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# MSM5298A

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## 68-DOT COMMON DRIVER

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### GENERAL DESCRIPTION

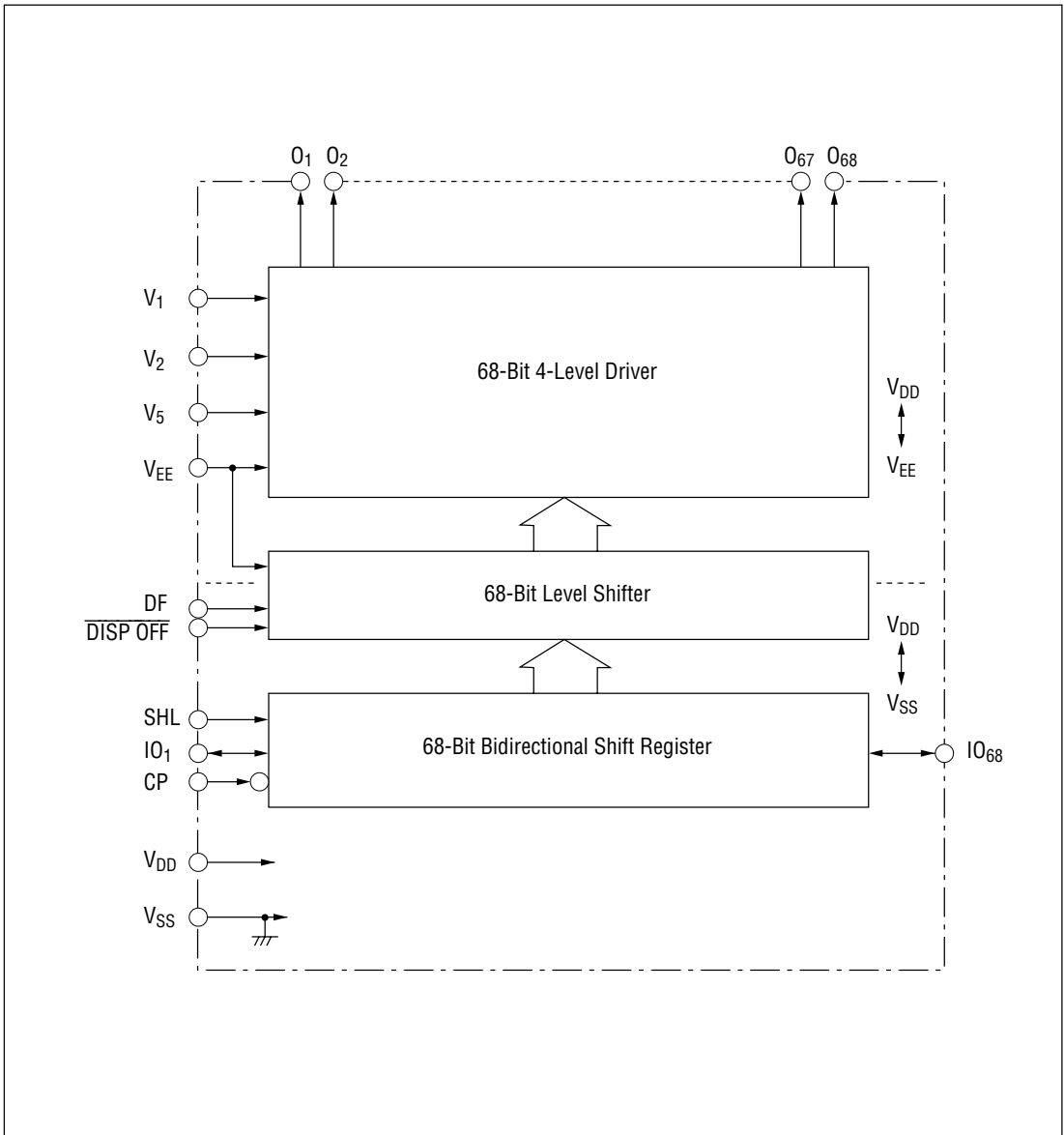
The MSM5298A is a dot matrix LCD common driver LSI which is fabricated using low power CMOS metal gate technology. This LSI consists of 68-bit bidirectional shift register, 68-bit level shifter and 68-bit 4-level driver.

This LSI has 68 output pins to be connected to the LCD. By connecting two or more MSM5298As in series, this LSI is applicable to a wide LCD panel.

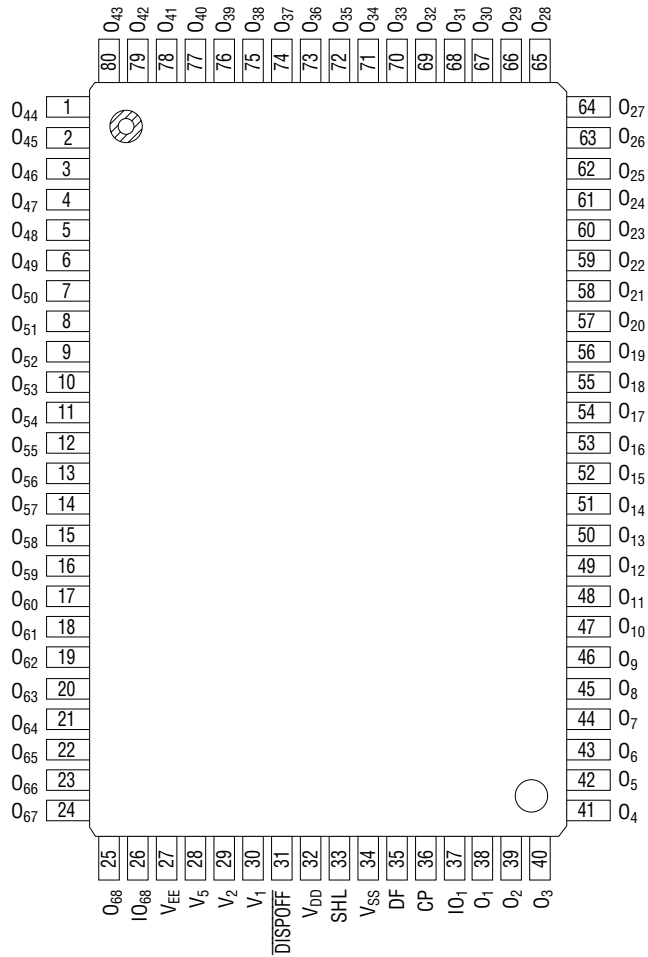
### FEATURES

- Supply voltage : 4.5 to 5.5V
- LCD driving voltage : 8 to 28V
- Applicable LCD duty : 1/64 to 1/256
- Applicable segment driver : MSM5299A (80 outputs), MSM5299C (80 outputs)
- Package options:
  - 80-pin plastic QFP (QFP80-P-1420-0.80-K) (Product name : MSM5298AGS-K)
  - 80-pin plastic QFP (QFP80-P-1420-0.80-BK) (Product name : MSM5298AGS-BK)

**BLOCK DIAGRAM**



**PIN CONFIGURATION (TOP VIEW)**



**80-Pin Plastic QFP**

Note: The abbreviated part number "M5298A" is imprinted on the package surface.

**ABSOLUTE MAXIMUM RATINGS**

(V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V <sub>DD</sub>	T <sub>a</sub> = 25°C	-0.3 to +6	V
Supply Voltage (2)	V <sub>LCD</sub>	T <sub>a</sub> = 25°C, V <sub>DD</sub> -V <sub>EE</sub> *1	0 to +30	V
Input Voltage	V <sub>I</sub>	T <sub>a</sub> = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Storage Temperature	T <sub>STG</sub>	—	-55 to +150	°C

\*1 V<sub>DD</sub> ≥ V<sub>1</sub> > V<sub>2</sub> > V<sub>5</sub> > V<sub>EE</sub>

**RECOMMENDED OPERATING CONDITIONS**

(V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	Range	Unit
Supply Voltage (1)	V <sub>DD</sub>	—	4.5 to 5.5	V
Supply Voltage (2)	V <sub>LCD</sub>	V <sub>DD</sub> -V <sub>EE</sub> *1	8 to 28	V
Operating Temperature	T <sub>op</sub>	—	-20 to +85	°C

\*1 V<sub>DD</sub> ≥ V<sub>1</sub> > V<sub>2</sub> > V<sub>5</sub> > V<sub>EE</sub>

**ELECTRICAL CHARACTERISTICS**

**DC Characteristics**

(V<sub>DD</sub> = 5V ± 10%, T<sub>a</sub> = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V <sub>IH</sub> *1	—	0.8V <sub>DD</sub>	—	V <sub>DD</sub>	V
"L" Input Voltage	V <sub>IL</sub> *1	—	V <sub>SS</sub>	—	0.2V <sub>DD</sub>	V
"H" Input Current	I <sub>IH</sub> *1	V <sub>I</sub> = V <sub>DD</sub> , V <sub>DD</sub> = 5.5V	—	—	1	μA
"L" Input Current	I <sub>IL</sub> *1	V <sub>I</sub> = 0V, V <sub>DD</sub> = 5.5V	—	—	-1	μA
"H" Output Voltage	V <sub>OH</sub> *2	I <sub>O</sub> = -0.4mA, V <sub>DD</sub> = 4.5V	V <sub>DD</sub> - 0.4	—	—	V
"L" Output Voltage	V <sub>OL</sub> *2	I <sub>O</sub> = 0.4mA, V <sub>DD</sub> = 4.5V	—	—	0.4	V
ON Resistance	R <sub>ON</sub> *4	V <sub>DD</sub> - V <sub>EE</sub> = 23V, V <sub>DD</sub> = 4.5V  V <sub>N</sub> - V <sub>O</sub>   = 0.25V *3	—	1.5	3	kΩ
Supply Current	I <sub>DD</sub>	f <sub>CP</sub> = 14kHz, V <sub>DD</sub> = 5.5V V <sub>DD</sub> - V <sub>EE</sub> = 23V, No load	—	—	100	μA
Input Capacitance	C <sub>I</sub>	f = 1MHz	—	5	—	pF

\*1 Applicable to CP, IO<sub>1</sub>, IO<sub>68</sub>, SHL, DF, DISP OFF.

\*2 Applicable to IO<sub>1</sub>, IO<sub>68</sub>.

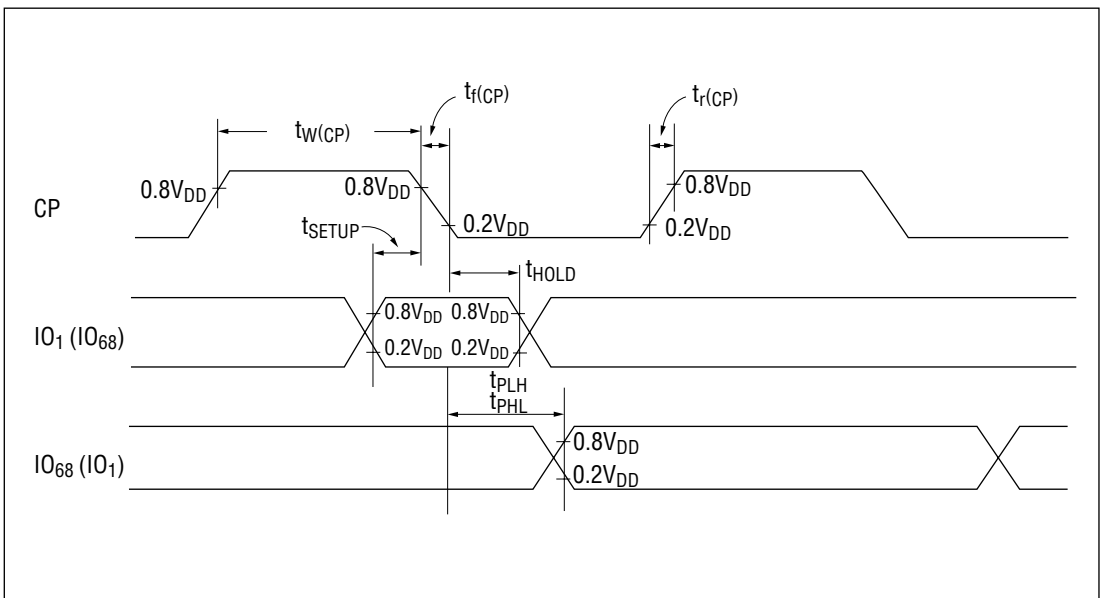
\*3 V<sub>N</sub> = V<sub>DD</sub> to V<sub>EE</sub>, V<sub>2</sub> =  $\frac{1}{15}$  (V<sub>DD</sub> - V<sub>EE</sub>), V<sub>5</sub> =  $\frac{14}{15}$  (V<sub>DD</sub> - V<sub>EE</sub>), V<sub>DD</sub> = V<sub>1</sub>

\*4 Applicable to O<sub>1</sub> to O<sub>68</sub>.

Switching Characteristics

( $V_{DD} = 5V \pm 10\%$ ,  $T_a = -20$  to  $+85^\circ C$ ,  $C_L = 15pF$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" , "L" Propagation Delay Time	$t_{PLH}$ $t_{PHL}$	—	—	—	250	ns
Clock Frequency	$f_{CP}$	—	—	—	1	MHz
Clock Pulse Width	$t_{W(CP)}$	—	125	—	—	ns
Data Setup Time $IO_1(IO_{68}) \rightarrow CP$	$t_{SETUP}$	—	100	—	—	ns
Data Hold Time $CP \rightarrow IO_1(IO_{68})$	$t_{HOLD}$	—	100	—	—	ns
Clock Pulse Rise/Fall Time	$t_r(CP)$ $t_f(CP)$	—	—	—	50	ns



## FUNCTIONAL DESCRIPTION

### Pin Functional Description

- IO<sub>1</sub>, IO<sub>68</sub>, SHL**

IO<sub>1</sub> and IO<sub>68</sub> are 68-bit bidirectional shift register input/output pins. The shifting direction is selected by the SHL pin. Refer to the table below.

SHL	Shifting direction	IO <sub>1</sub> /IO <sub>68</sub>	Input/output	Description
L	O <sub>1</sub> → O <sub>68</sub>	IO <sub>1</sub>	Input	The scanning data from the LCD controller LSI is input into IO <sub>1</sub> synchronized with the clock pulse.* 1
		IO <sub>68</sub>	Output	Shift register contents output pin. The data which is input into IO <sub>1</sub> is output from IO <sub>68</sub> with 68 bit's delay, synchronized with the clock pulse.
H	O <sub>68</sub> → O <sub>1</sub>	IO <sub>68</sub>	Input	The scanning data from the LCD controller LSI is input into IO <sub>68</sub> synchronized with the clock pulse.* 1
		IO <sub>1</sub>	Output	Shift register contents output pin. The data which is input into IO <sub>68</sub> is output from IO <sub>1</sub> with 68 bit's delay, synchronized with the clock pulse.

\*1 The combination of the scanning data, IO<sub>1</sub> or IO<sub>68</sub>, and the LCD driving output, O<sub>1</sub> to O<sub>68</sub>, is shown in the table below.

IO <sub>1</sub> , IO <sub>68</sub>	LCD driving output
"H"	Select level (V <sub>1</sub> , V <sub>EE</sub> )
"L"	Non-select level (V <sub>2</sub> , V <sub>5</sub> )

- CP**

Clock pulse input pin for 68-bit bidirectional shift register. The data is shifted to 68-bit bidirectional shift register at the falling edge of the clock pulse.

- DF**

Alternate signal input pin for LCD driving.

- V<sub>DD</sub>, V<sub>SS</sub>**

Supply voltage pins. V<sub>DD</sub> should be 4.5 to 5.5V. V<sub>SS</sub> is a ground pin. (V<sub>SS</sub> = 0V).

- DISP OFF**

Control input pin for display data output level (O<sub>1</sub> to O<sub>68</sub>). V<sub>1</sub> level is output from O<sub>1</sub> to O<sub>68</sub> pin during "L" level input. Refer to Truth Table.

- **V<sub>1</sub>, V<sub>2</sub>, V<sub>5</sub>, V<sub>EE</sub>**  
Bias supply voltage pins to drive the LCD. The V<sub>1</sub> pin can be separated from the V<sub>DD</sub> pin.
- **O<sub>1</sub> - O<sub>68</sub>**  
Display data output pins which correspond to each bit of the 68-bit bidirectional shift register. One of the four levels, V<sub>1</sub>, V<sub>2</sub>, V<sub>5</sub> and V<sub>EE</sub>, is selected based on the combination of the latched data level and DF signal. (Refer to Truth Table.)  
Connect these outputs to the common side of the LCD panel.

**Truth Table**

DF	Shift register data	$\overline{\text{DISP OFF}}$	Driver output level (O <sub>1</sub> to O <sub>68</sub> )
L	L	H	V <sub>2</sub>
L	H	H	V <sub>EE</sub>
H	L	H	V <sub>5</sub>
H	H	H	V <sub>1</sub>
X	X	L	V <sub>1</sub>

X : Don't care

**NOTES ON USE (when turning the power ON or OFF)**

The LCD drivers of this IC require a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC.

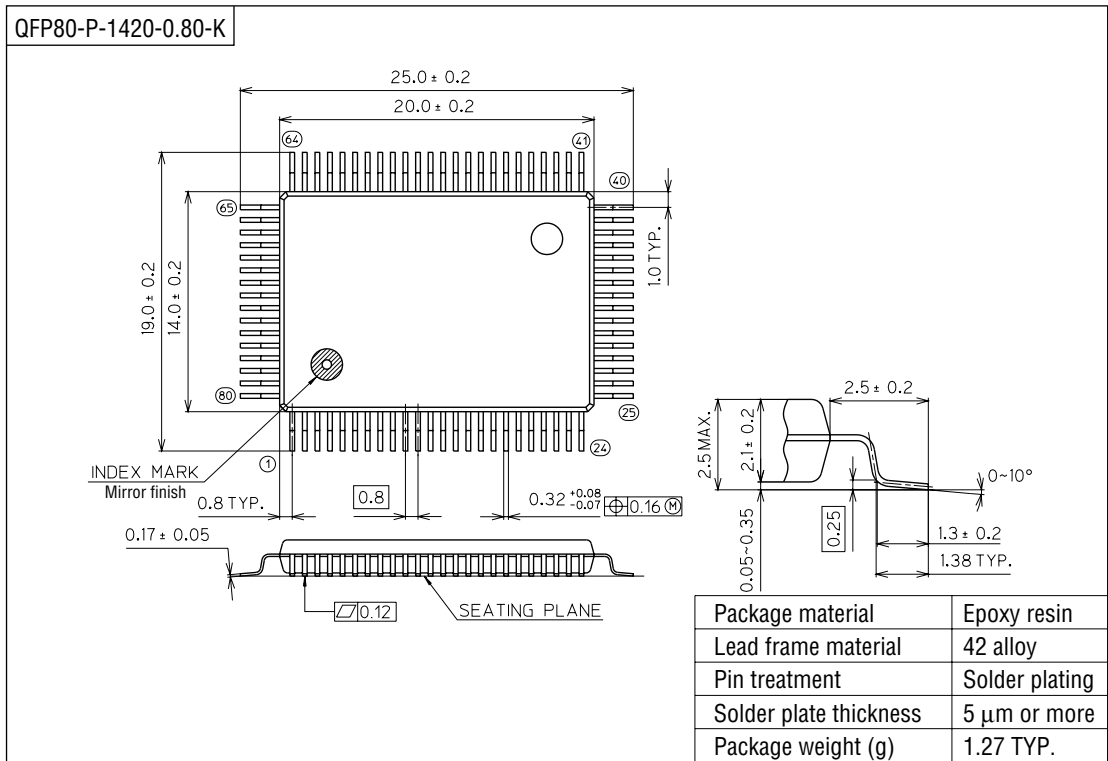
Be sure to follow the sequence below when turning the power ON or OFF.

Power ON : Logic circuits ON → LCD drivers ON, or both ON at a time

Power OFF : LCD drivers OFF → logic circuits OFF, or both OFF at a time

**PACKAGE DIMENSIONS**

(Unit : mm)

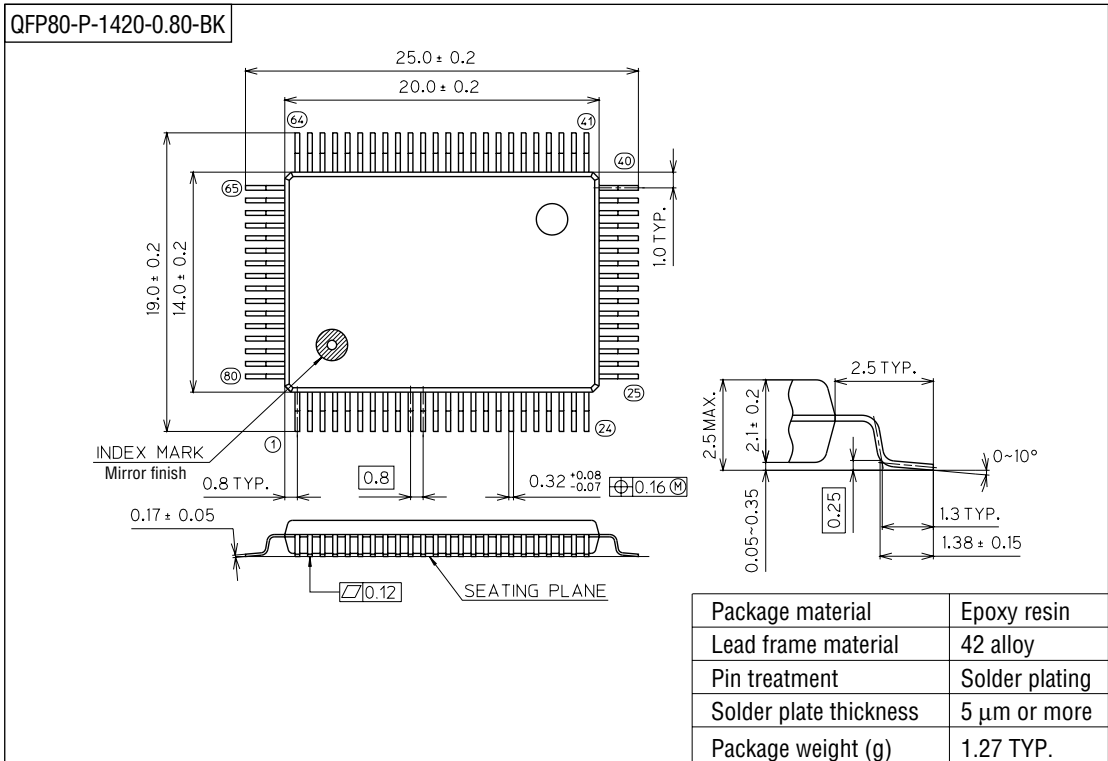


**Notes for Mounting the Surface Mount Type Package**

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).



(Unit : mm)



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