NIPPON PRECISION CIRCUITS INC.

QS7779PM/CM

3D Stereo Enhancement and 3D Virtual Stereo Surround
with Dolby Pro Logic and Mixed DVD (AC-3) Decoder

OVERVIEW

The QS7779PM/CM is an audio processor IC which implements a decoder for stereo matrix encoded source materials such as the Dolby Surround Pro Logic and mixed DVD (AC–3) with surround virtualization using QSound™ technology developed and licensed by QSound Labs, Inc. This chip produces enhanced stereo sound for a stereo input signal and if the input signal contains matrix encoded surround sound, the chip decodes it and produces 3D virtualized surround sounds with two speakers.

FEATURES

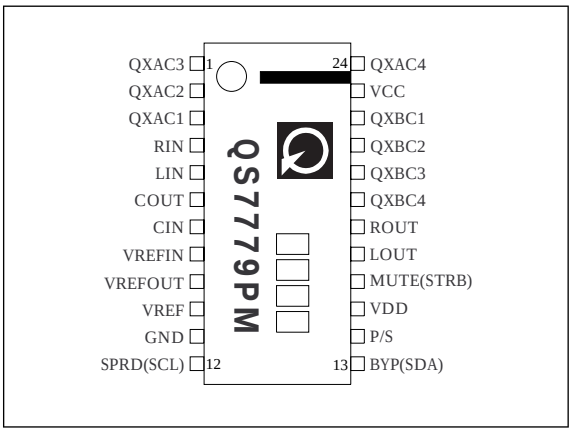
- Capable of decoding Dolby Surround materials such as Dolby Pro Logic or other matrix surround encoded materials (DVD/AC–3)
- Virtualized surround sound with two speakers
- 3D stereo sound enhancement
- Two enhanced levels
- Parallel and serial digital interface for mode control
  - QS7779CM for I^2C 2 control pins serial interface (Data, Clock)
  - QS7779PM for three-wire serial interface (Data, Clock and Strobe)
- Supply voltage (analog): 5 to 13V
  Supply voltage (digital): 4.5 to 5.5V
- 24-pin SSOP packaging

APPLICATIONS

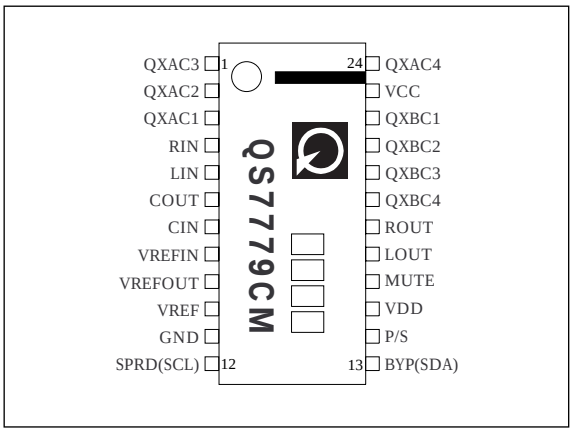
- DVD, Laser disk player
- Audio systems including TV, Radio and VCR
- Computer-based multimedia products, including sound cards and powered loudspeakers

PINOUT (Top view)

QS7779PM



QS7779CM



Using these products does not require any Dolby certifications.

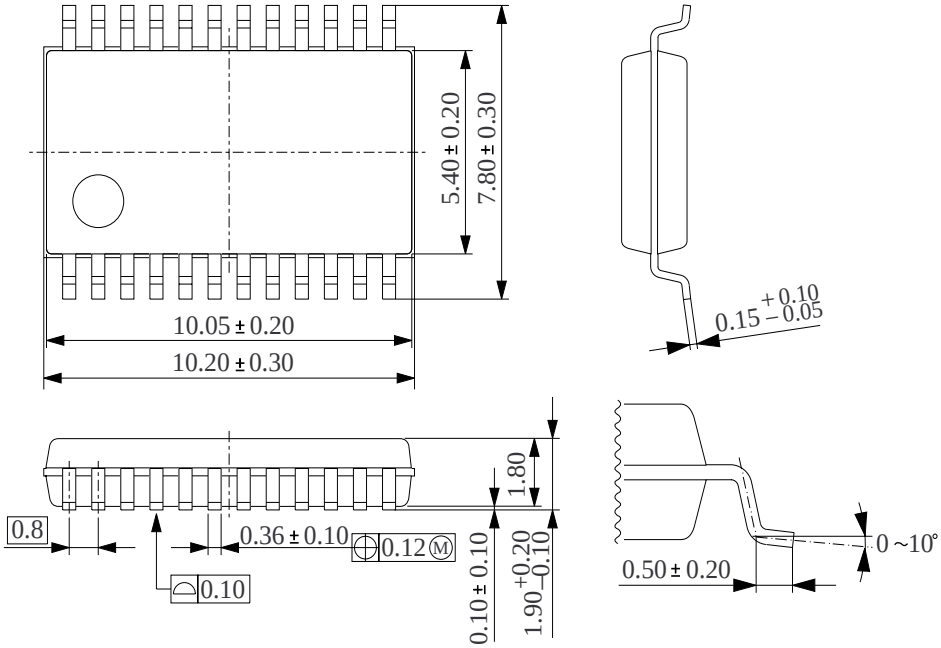
ORDERING INFORMATION

Device	Package
QS7779PM	24-pin SSOP
QS7779CM	24-pin SSOP

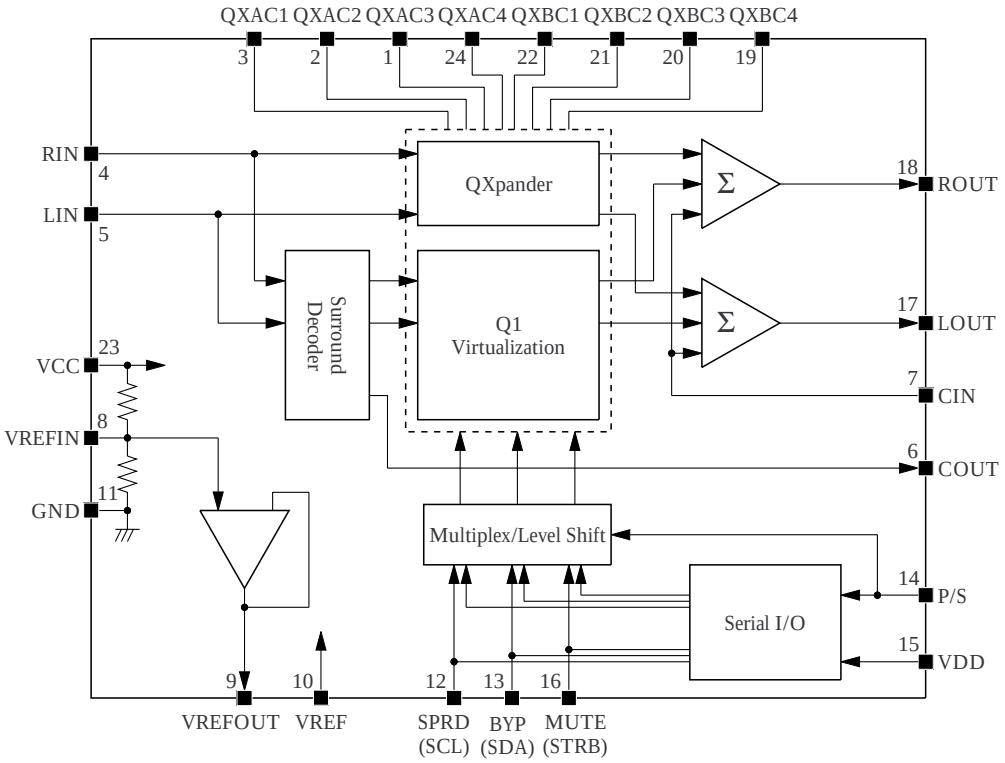
I^2C bus is a registered trademark of Philips Electronics N.V.
Dolby and the double-D symbol are registered trademarks of Dolby Laboratories Licensing Corporation.

PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name		I/O	Description
	Parallel	Serial		
1	QXAC3		I	Capacitor 3 for QEXPANDER filter A
2	QXAC2		I	Capacitor 2 for QEXPANDER filter A
3	QXAC1		I	Capacitor 1 for QEXPANDER filter A
4	RIN		I	Right channel signal input
5	LIN		I	Left channel signal input
6	COUT		O	Decoded center signal output
7	CIN		I	Center signal input for summing with the right and the left signal outputs
8	VREFIN		O	Internally generated reference voltage (V_{CC}/2)
9	VREFOUT		O	Buffered reference voltage (V_{CC}/2)
10	VREF		I	Signal reference input
11	GND		–	Ground 0V
12	SPRD	–	I	Enhancement control (H: spread maximum, L: spread minimum)
	–	SCL[1]	I	Serial data shift clock
13	BYP	–	I	Bypass control (H: Bypass on, L: Qsurround on)
	–	SDA[2]	I/O	Serial data input. ACK data output for I^2C (QS7779CM)
14	P/S		I	Interface mode control (H: parallel I/O, L: serial I/O)
15	VDD		–	Digital power supply DC4.5 to 5.5V
16	MUTE	–	I	Output mute control (H: mute on, L: mute off)
	–	STRB	I	Serial data strobe (not applicable to I^2C of QS7779CM)
17	LOUT		O	Left signal output
18	ROUT		O	Right signal output
19	QXBC4		I	Capacitor 4 for QEXPANDER filter B
20	QXBC3		I	Capacitor 3 for QEXPANDER filter B
21	QXBC2		I	Capacitor 2 for QEXPANDER filter B
22	QXBC1		I	Capacitor 1 for QEXPANDER filter B
23	VCC		–	Analog power supply DC5 to 13V
24	QXAC4		I	Capacitor 4 for QEXPANDER filter A

1. QS7779CM:CMOS input. No protective diode between the terminal and VDD.
   QS7779PM:CMOS input. Protective diode is in between the terminal and VDD.
2. QS7779CM:Nch open drain terminal. No protective diode between terminal and VDD.
   QS7779PM:CMOS input. Protective diode is in between the terminal and VDD.

SPECIFICATIONS

Absolute Maximum Ratings

GND = 0V

Parameter	Symbol	Rating	Unit
Supply voltage (analog)	V_{CC}	– 0.3 to 15	V
Supply voltage (digital)	V_{DD}	– 0.3 to 7	V
Input voltage (analog)	V_{IANA}	– 0.3 to V_{CC} + 0.3	V
Input voltage (digital)	V_{IDIG}	– 0.3 to V_{DD} + 0.3	V
I^2C input voltage (SDA, SCL)	V_{IOPEN}	10	V
Power dissipation	P_D	250	mW
Storage temperature	T_{stg}	– 40 to 125	°C
Soldering temperature	T_{SLD}	255	°C
Soldering time	t_{SLD}	10	sec

Recommended Operating Conditions

GND = 0V

Parameter	Symbol	Limits	Unit
Supply voltage (analog)	V_{CC}	5 to 13	V
Supply voltage (digital)	V_{DD}	4.5 to 5.5	V
Operating temperature	T_{OPR}	– 20 to 70	°C

DC Electrical Characteristics

V_{CC} = 9V, V_{DD} = 5V, GND = 0V, Ta = 25 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit
			min	typ	max	
LIN, RIN analog input impedance	Z_{AIN1}		16	20	24	kΩ
CIN analog input impedance	Z_{AIN2}		4	5	6	kΩ
Reference voltage out	V_{REFOUT}		–	$V_{CC}/2$	–	V
HIGH-level input voltage	V_{IH}		$0.7 \times V_{DD}$	–	–	V
LOW-level input voltage	V_{IL}		–	–	$0.3 \times V_{DD}$	V
Input leakage current	I_{LEAK}		– 3	–	3	µA
SDA, SCL input leakage current (I^2C input pin)	I_{LOPEN}	V_{IN} = 10V	– 3	–	3	µA
SDA LOW-level output voltage	V_{OL}	Acknowledge signal out I_{OL} = 3mA	0	–	0.4	V
Supply voltage (analog)	V_{CC}		5	–	13	V
Supply voltage (digital)	V_{DD}		4.5	–	5.5	V
Current consumption (analog)	I_{CC}		–	5	6.5	mA
Current consumption (digital)	I_{DD}		–	0.3	0.5	mA
Standby current (analog)	I_{CCSAVE}		–	0.1	0.2	mA

Noise/THD Characteristics

V_{CC} = 9V, V_{DD} = 5V, GND = 0V, Ta = 25 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit
			min	typ	max	
Noise voltage	N_{BYP}	BYP = HIGH (Bypass mode), A-wgt, LOUT, ROUT	–	10	20	μV_{RMS}
Noise voltage	N_{QS}	BYP = LOW (Qsurround mode), SPRD = HIGH, A-wgt, LOUT, ROUT	–	20	40	μV_{RMS}
THD	THD_{QS}	LIN = RIN = $1V_{RMS}$, BYP = LOW (Qsurround mode), SPRD = HIGH, f = 1kHz	–	–	0.1	%

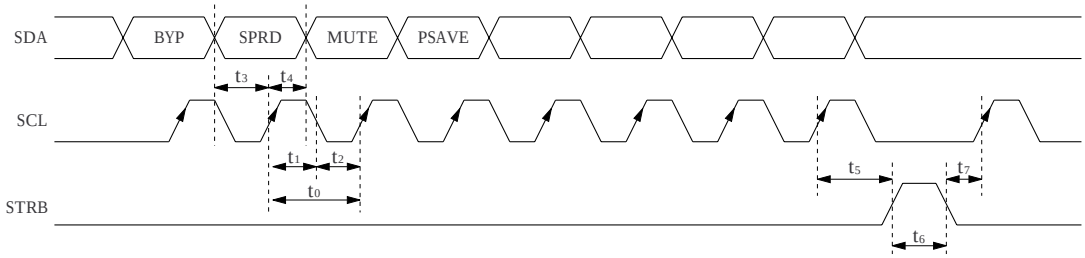
AC Electrical Characteristics

V_{CC} = 9V, V_{DD} = 5V, GND = 0V, Ta = 25 °C unless otherwise noted.

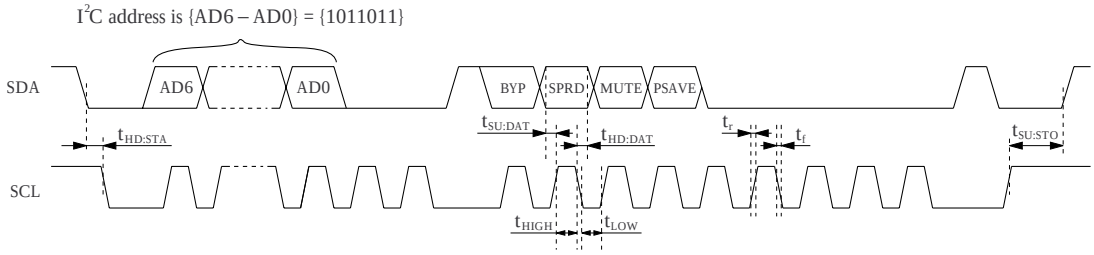
Parameter	Symbol	Condition	Limits			Unit
			min	typ	max	
Maximum input voltage 1	V_{FIN1}	LIN = RIN, BYP = LOW, SPRD = HIGH, f = 1kHz	1.4	–	–	V_{RMS}
Maximum input voltage 2	V_{FIN2}	LIN = – RIN, BYP = LOW, SPRD = HIGH, f = 1kHz	0.5	–	–	V_{RMS}
Bypass gain	G_{BYP}	BYP = HIGH, f = 1kHz, LIN to LOUT, RIN to ROUT	– 2	0	2	dB
Forward gain	G_F	SPRD = HIGH, BYP = LOW, f = 1kHz, LIN to LOUT, RIN to ROUT	6.6	8.6	10.6	dB
Crosstalk gain	G_{XF}	SPRD = HIGH, BYP = LOW, f = 1kHz, LIN to ROUT, RIN to LOUT	0.5	2.5	4.5	dB
SCL clock pulse cycle	t_0	PM version	100	–	–	ns
SCL HIGH-level clock pulse width	t_1	PM version	40	–	–	ns
SCL LOW-level clock pulse width	t_2	PM version	40	–	–	ns
SDA set-up time	t_3	PM version	15	–	–	ns
SDA hold time	t_4	PM version	30	–	–	ns
STRB set-up time	t_5	PM version	50	–	–	ns
STRB clock pulse width	t_6	PM version	100	–	–	ns
STRB hold time	t_7	PM version	50	–	–	ns
SCL hold time (I^2C)	$t_{HD:STA}$	CM version	4.0	–	–	µs
SCL set-up time (I^2C)	$t_{SU:STO}$	CM version	4.0	–	–	µs
SDA hold time (I^2C)	$t_{HD:DAT}$	CM version	5.0	–	–	µs
SDA set-up time (I^2C)	$t_{SU:DAT}$	CM version	250	–	–	ns
SCL HIGH-level clock pulse width (I^2C)	t_{HIGH}	CM version	4.0	–	–	µs
SCL LOW-level clock pulse width (I^2C)	t_{LOW}	CM version	4.7	–	–	µs
SCL rise time (I^2C)	t_r	CM version	–	–	1000	ns
SCL fall time (I^2C)	t_f	CM version	–	–	300	ns

Serial Interface

Three-wire serial interface (for QS7779PM)



I²C serial interface (for QS7779CM)



FUNCTIONAL DESCRIPTION

Operating Mode

This chip can be set to a desired operating mode by control pins for the parallel interface (P/S pin sets to HIGH) or control bits for the serial interface (P/S pin sets to LOW). The control pins or bits configurations are shown in the following table.

Mode No.	Control Pins/Bits				Operation (Output signal)		Description
	BYP	SPRD	MUTE	PSAVE	LOUT	ROUT	
1	1	×	0	0	LIN	RIN	Bypass mode
2	0	0	0	0	QX(LIN)	QX(RIN)	Stereo enhanced and virtual surround mode with lower enhanced level
3	0	1	0	0	QX+(LIN)	QX+(RIN)	Stereo enhanced and virtual surround mode with higher enhanced level
4	×	×	1	0	–	–	Mute mode
5	×	×	1	1	–	–	Power save mode. This function is available with serial interface only

Note1. ×: Don't care.
Note2. MUTE = 1 when PSAVE = 1

Mode description

Mode No.	Operating description
1	Bypass mode. Outputs the stereo signal as it is input.
2	Stereo Enhanced and virtual surround mode with lower enhanced level. The Dolby Surround Pro Logic signal (Lt, Rt) input. Available Surround Effect with two speakers by Qsurround technology. Virtual location of each signal is; The Front signal: Virtually outside of the speakers. The Rear signal: Virtually behind the listeners.
3	Stereo Enhanced and virtual surround mode with higher enhanced level. The Dolby Surround Pro Logic signal (Lt, Rt) input. Available Surround Effect with two speakers by Qsurround technology. This mode outputs the signals much more spread sound than Mode 2.
4	Mute mode. No signal at output pins.
5	Power save mode. This function is available with serial interface only.

Center signal output

CIN and COUT are used to emphasize the center signal.

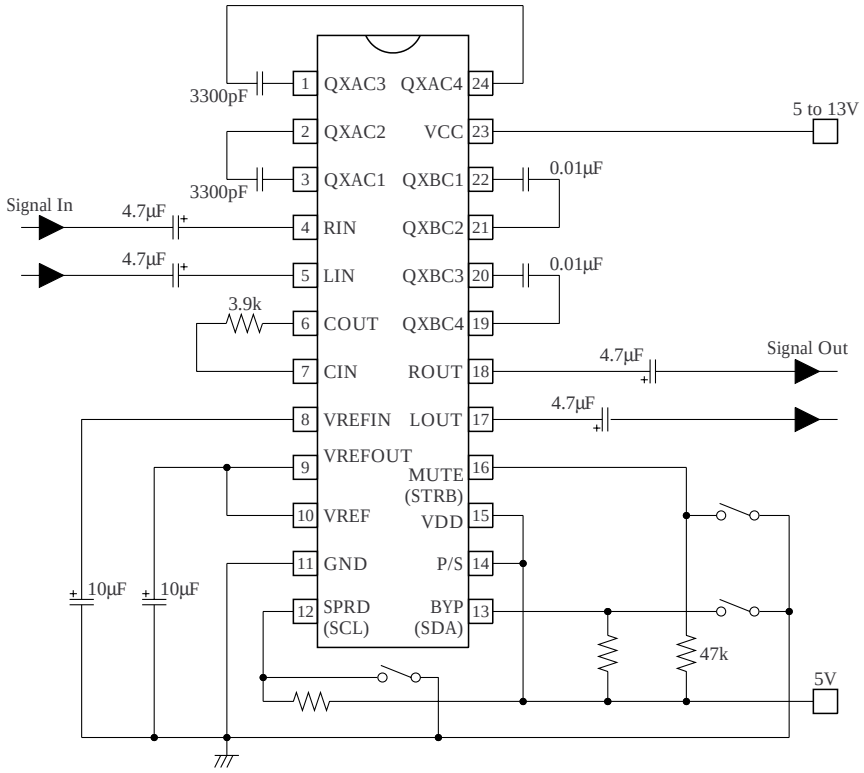
Pin	Description
CIN	Outputs the doubled signal to ROUT and LOUT always.
COUT	Outputs the half level of signal ((RIN+LIN)/2).

How to use CIN and COUT.

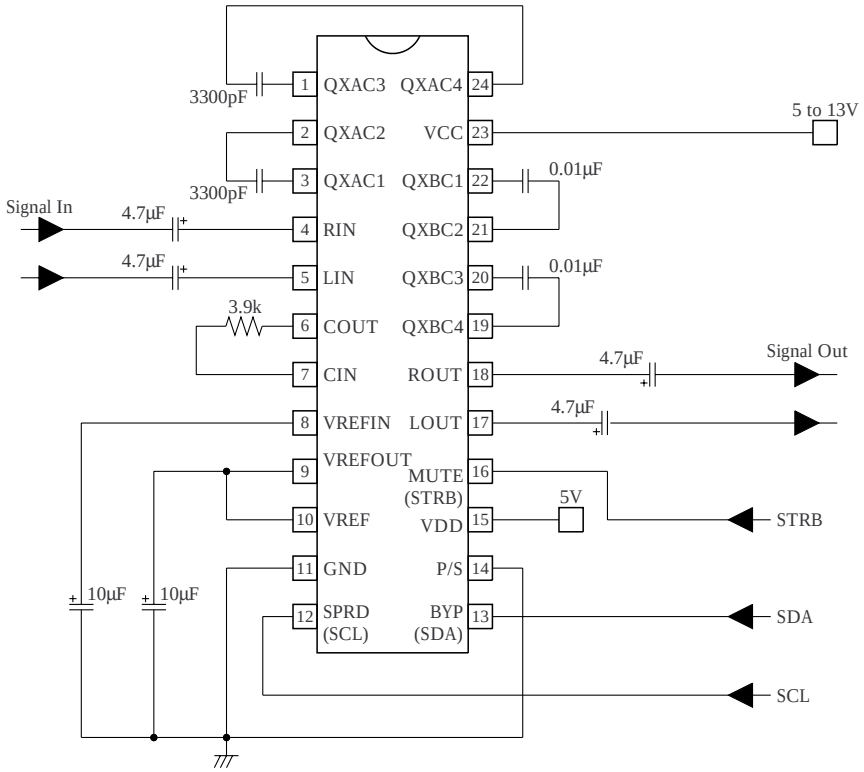
- Connect CIN and COUT with a resistor to make the center signal emphasized.
- Input resistance for CIN is 5kΩ. For example, connecting a 5kΩ resistor between CIN and COUT makes output of (RIN+LIN)/2 to ROUT and LOUT.
- Directly connecting CIN and COUT makes ROUT and LOUT output (RIN+LIN).

TYPICAL APPLICATION CIRCUIT

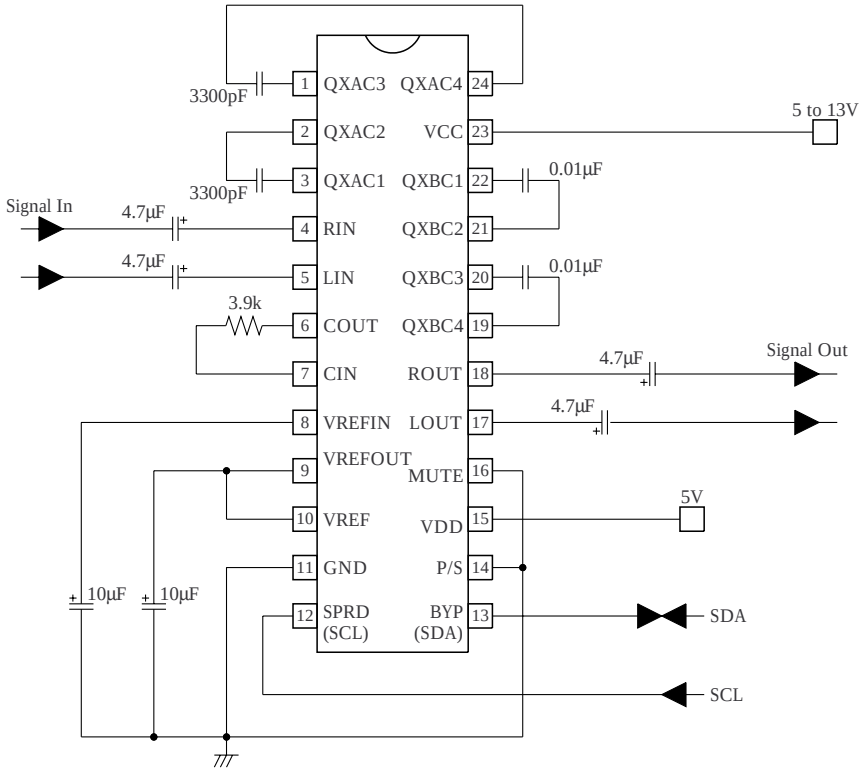
QS7779PM/CM with parallel interface



QS7779PM with serial interface



QS7779CM with serial interface



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