

FEATURES

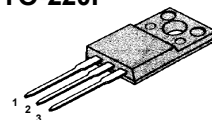
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25 μ A (Max.) @ $V_{DS} = 900V$
- Low $R_{DS(ON)}$: 4.679 Ω (Typ.)

$$BV_{DSS} = 900 V$$

$$R_{DS(on)} = 6.2 \Omega$$

$$I_D = 2 A$$

TO-220F



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	900	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	2	A
	Continuous Drain Current ($T_C=100^\circ C$)	1.3	
I_{DM}	Drain Current-Pulsed ①	12	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	286	mJ
I_{AR}	Avalanche Current ①	2	A
E_{AR}	Repetitive Avalanche Energy ①	3.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.5	V/ns
P_D	Total Power Dissipation ($T_C=25^\circ C$)	35	W
	Linear Derating Factor	0.28	
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	3.57	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV _{DSS}	Drain-Source Breakdown Voltage	900	--	--	V	V _{GS} =0V, I _D =250μA
ΔBV/ΔT _J	Breakdown Voltage Temp. Coeff.	--	1.13	--	V/°C	I _D =250μA See Fig 7
V _{GS(th)}	Gate Threshold Voltage	2.0	--	3.5	V	V _{DS} =5V, I _D =250μA
I _{GSS}	Gate-Source Leakage, Forward	--	--	100	nA	V _{GS} =30V
	Gate-Source Leakage, Reverse	--	--	-100		V _{GS} =-30V
I _{DSS}	Drain-to-Source Leakage Current	--	--	25	μA	V _{DS} =900V
		--	--	250		V _{DS} =720V, T _C =125°C
R _{DS(on)}	Static Drain-Source On-State Resistance	--	--	6.2	Ω	V _{GS} =10V, I _D =1A ④
g _{fs}	Forward Transconductance	--	1.78	--	S	V _{DS} =50V, I _D =1A ④
C _{ISS}	Input Capacitance	--	590	770	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz See Fig 5
C _{OSS}	Output Capacitance	--	55	65		
C _{RSS}	Reverse Transfer Capacitance	--	22	28		
t _{d(on)}	Turn-On Delay Time	--	16	40	ns	V _{DD} =450V, I _D =3A, R _G =16Ω See Fig 13 ④ ⑤
t _r	Rise Time	--	26	60		
t _{d(off)}	Turn-Off Delay Time	--	47	105		
t _f	Fall Time	--	24	60		
Q _g	Total Gate Charge	--	28	37	nC	V _{DS} =720V, V _{GS} =10V, I _D =3A See Fig 6 & Fig 12 ④ ⑤
Q _{gs}	Gate-Source Charge	--	5.5	--		
Q _{gd}	Gate-Drain(米勒?) Charge	--	11.9	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I _S	Continuous Source Current	--	--	2	A	Integral reverse pn-diode in the MOSFET
I _{SM}	Pulsed-Source Current ①	--	--	12		
V _{SD}	Diode Forward Voltage ④	--	--	1.4	V	T _J =25°C, I _S =2A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	380	--	ns	T _J =25°C, I _F =3A
Q _{rr}	Reverse Recovery Charge	--	1.9	--	μC	di _F /dt=100A/μs ④

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=135mH, I_{AS}=2A, V_{DD}=50V, R_G=27Ω, Starting T_J=25°C
- ③ I_{SD}≤3A, di/dt≤90A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25°C
- ④ Pulse Test : Pulse Width = 250μs, Duty Cycle ≤ 2%
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

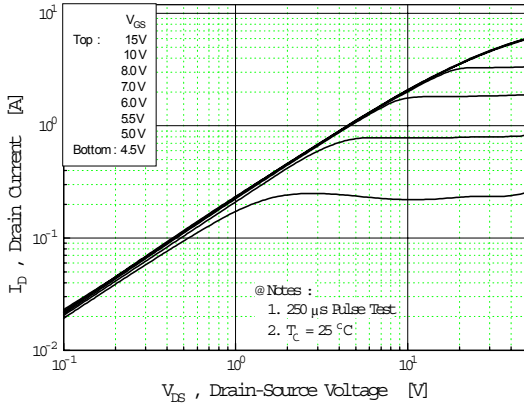


Fig 2. Transfer Characteristics

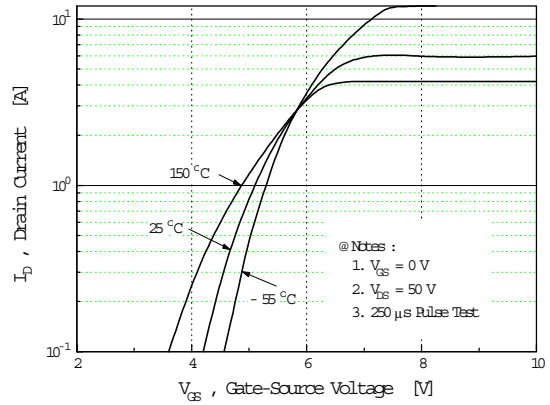


Fig 3. On-Resistance vs. Drain Current

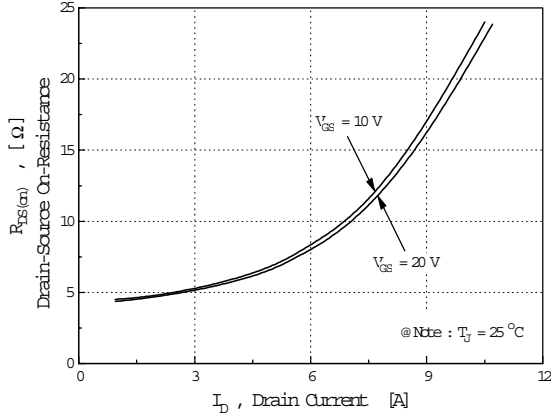


Fig 4. Source-Drain Diode Forward Voltage

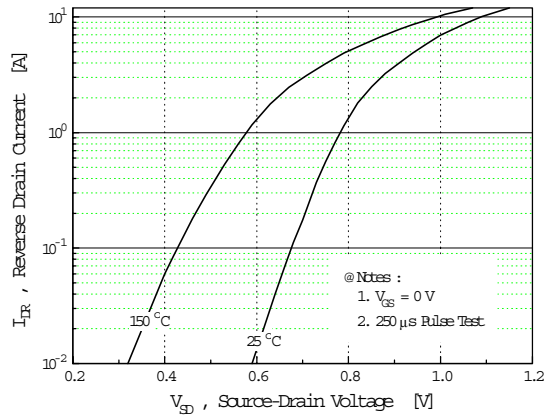


Fig 5. Capacitance vs. Drain-Source Voltage

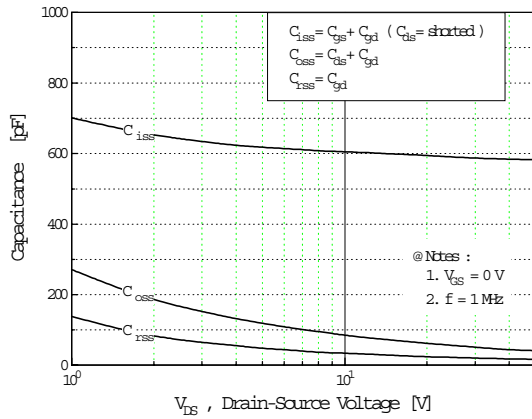


Fig 6. Gate Charge vs. Gate-Source Voltage

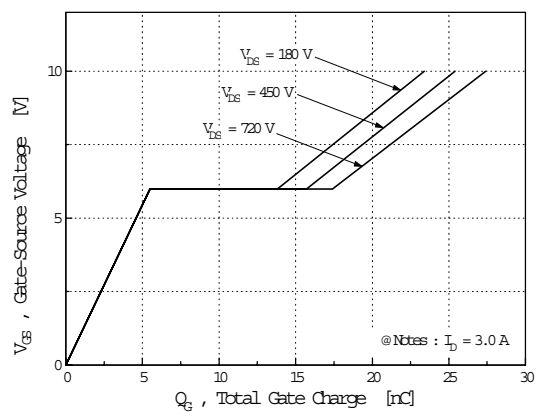


Fig 7. Breakdown Voltage vs. Temperature

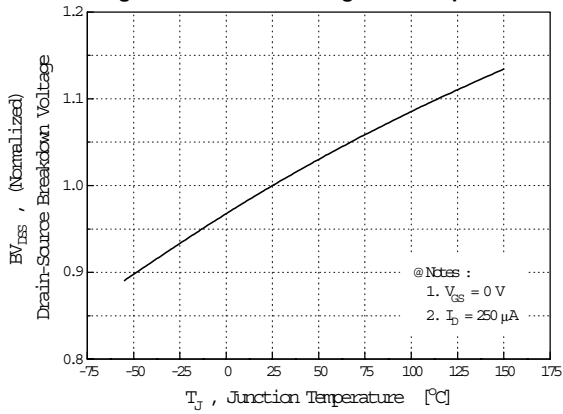


Fig 8. On-Resistance vs. Temperature

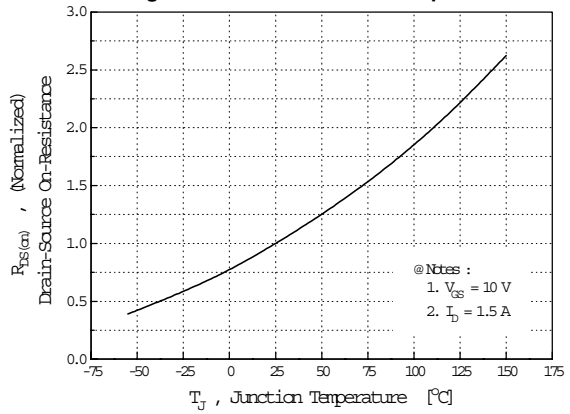


Fig 9. Max. Safe Operating Area

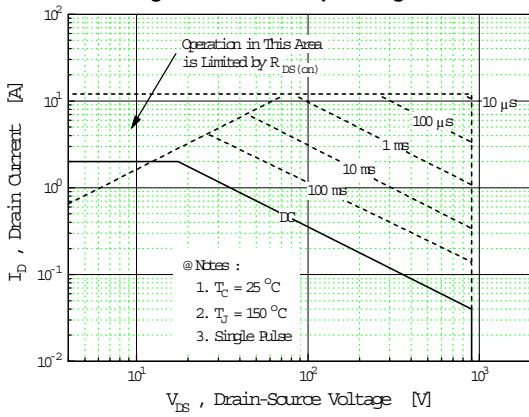


Fig 10. Max. Drain Current vs. Case Temperature

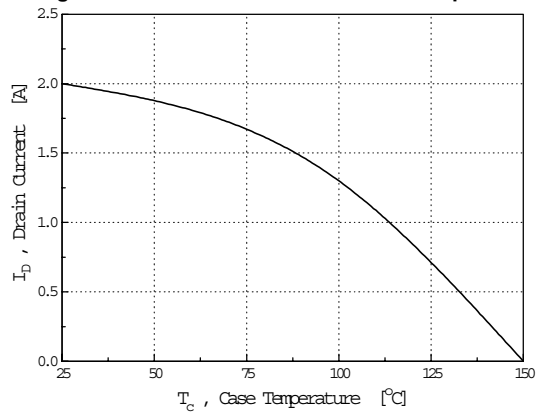


Fig 11. Thermal Response

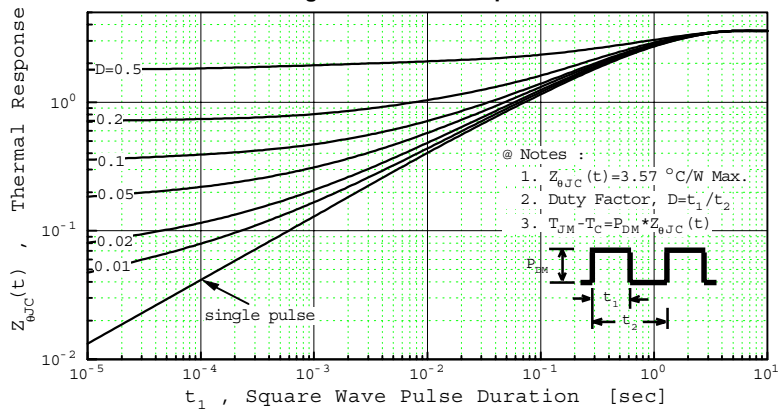


Fig 12. Gate Charge Test Circuit & Waveform

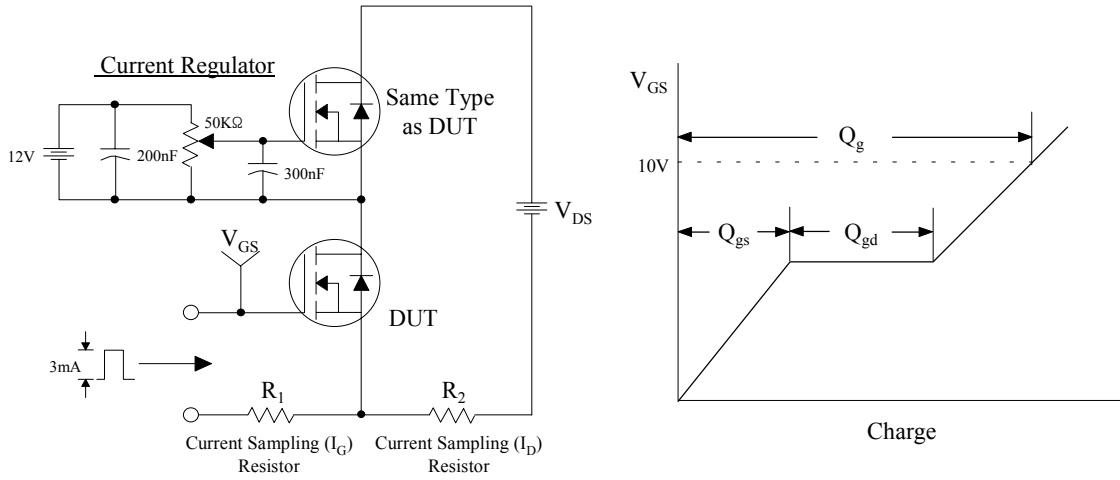


Fig 13. Resistive Switching Test Circuit & Waveforms

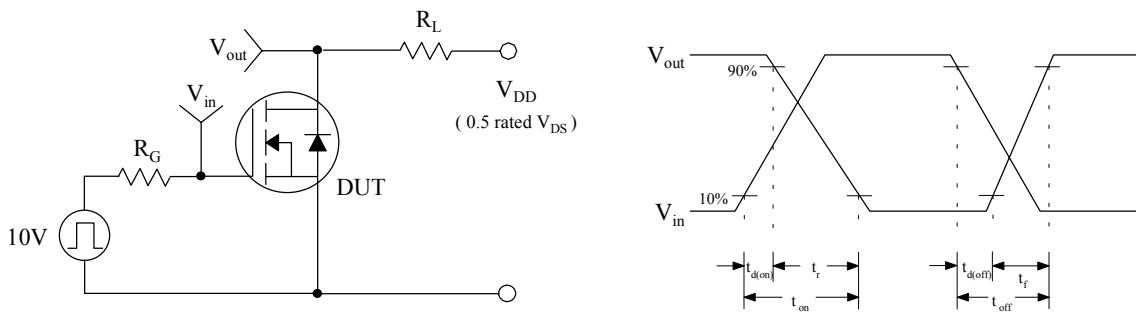


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

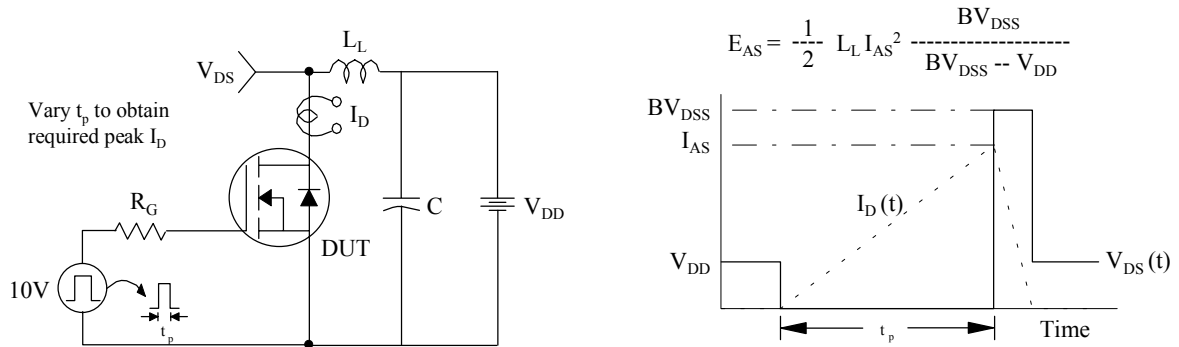


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

