

Features

- Low ON-state resistance.
- Ultrahigh-speed switching.
- Micaless package facilitating mounting.

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

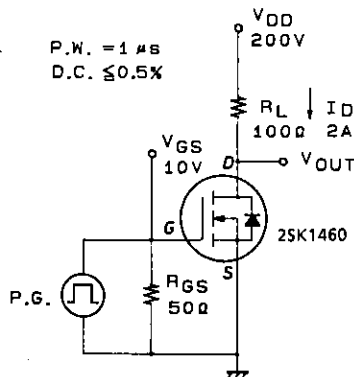
			unit
Drain-to-Source Voltage	V_{DSS}	900	V
Gate-to-Source Voltage	V_{GSS}	± 30	V
Drain Current(DC)	I_D	3.5	A
Drain Current(Pulse)	I_{DP}	$PW \leq 10\mu\text{s}, \text{duty cycle} \leq 1\%$	7 A
Allowable Power Dissipation	P_D	2.0	W
		$T_c = 25^\circ\text{C}$	40 W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics at $T_a = 25^\circ\text{C}$

			min	typ	max	unit
D-S Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 1\text{mA}, V_{GS} = 0$	900			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 900\text{V}, V_{GS} = 0$			1.0	mA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 30\text{V}, V_{DS} = 0$			± 100	nA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 10\text{V}, I_D = 1\text{mA}$	2.0		3.0	V
Forward Transfer Admittance	$ Y_{fs} $	$V_{DS} = 20\text{V}, I_D = 2\text{A}$	1.0	2.0		S
Static Drain-to-Source ON-State Resistance	$R_{DS(on)}$	$I_D = 2\text{A}, V_{GS} = 10\text{V}$		2.8	3.6	Ω
Input Capacitance	C_{iss}	$V_{DS} = 20\text{V}, f = 1\text{MHz}$		700		pF
Output Capacitance	C_{oss}	$V_{DS} = 20\text{V}, f = 1\text{MHz}$		300		pF
Reverse Transfer Capacitance	C_{rss}	$V_{DS} = 20\text{V}, f = 1\text{MHz}$		170		pF
Turn-ON Delay Time	$t_{d(on)}$	$I_D = 2\text{A}, V_{GS} = 10\text{V}$ $V_{DD} = 200\text{V}, R_{GS} = 50\Omega$		15		ns
Rise Time	t_r			35		ns
Turn-OFF Delay Time	$t_{d(off)}$			200		ns
Fall Time	t_f			65		ns
Diode Forward Voltage	V_{SD}	$I_S = 3.5\text{A}, V_{GS} = 0$			1.8	V

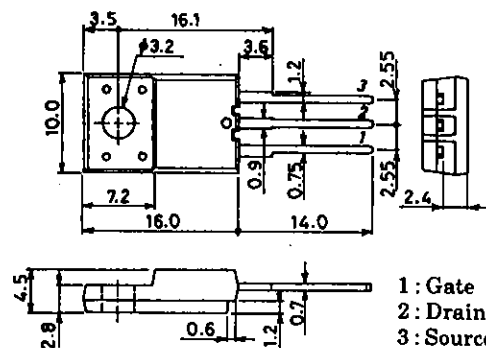
(Note) Be careful in handling the 2SK1460 because it has no protection diode between gate and source.

Switching Time Test Circuit



Package Dimensions 2078B

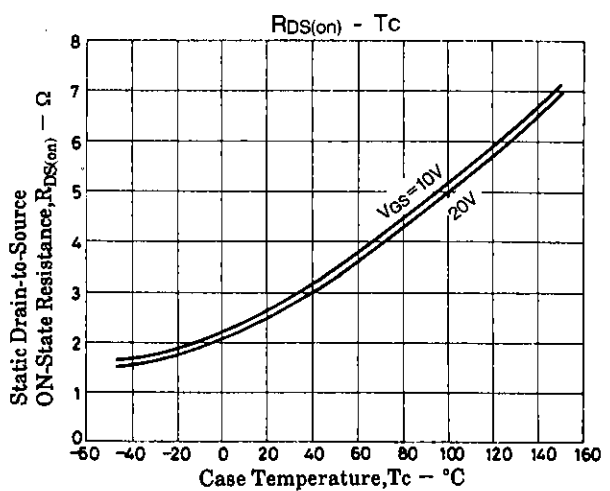
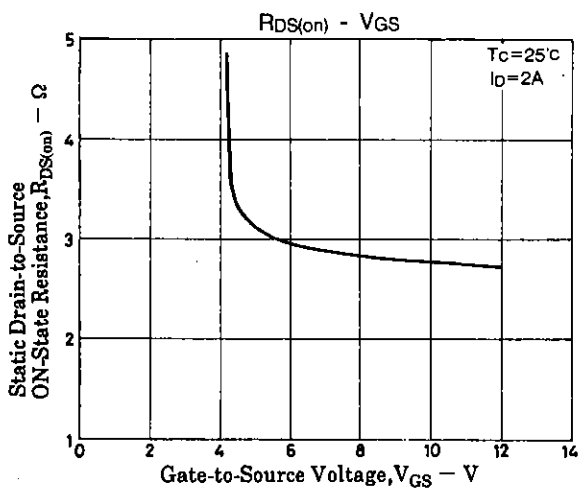
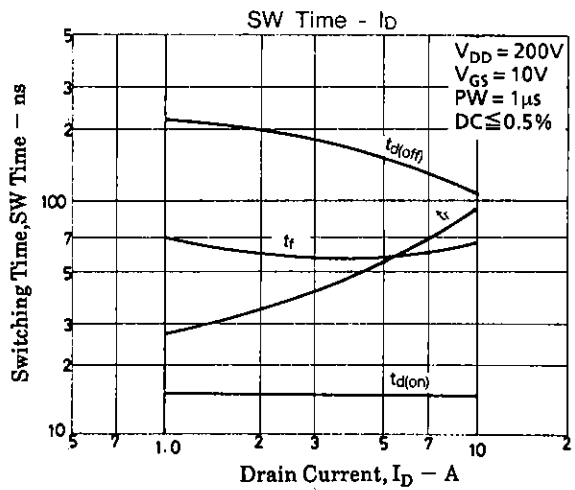
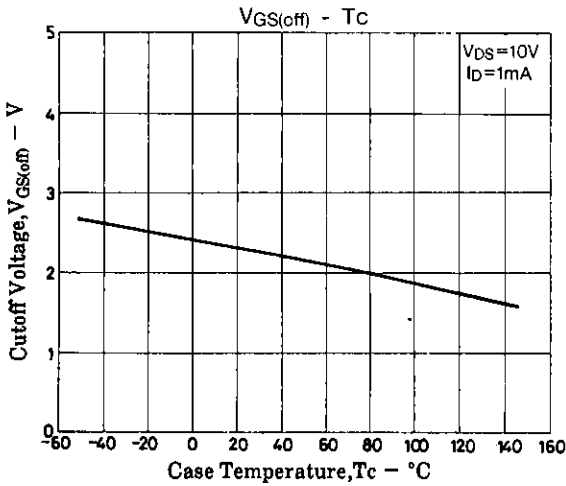
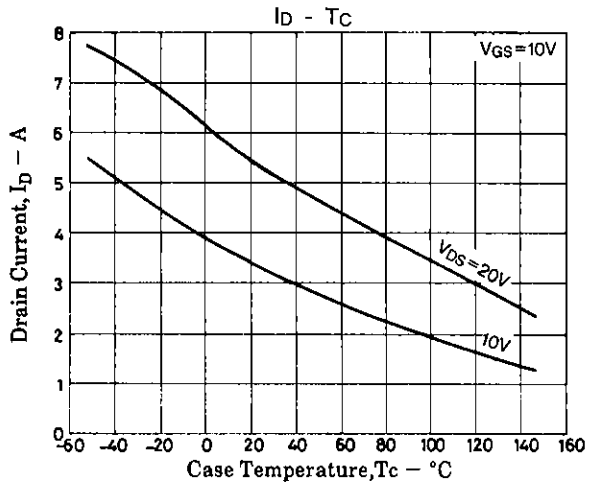
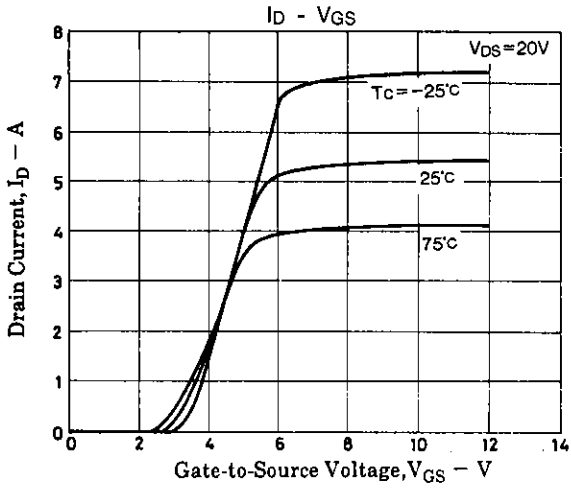
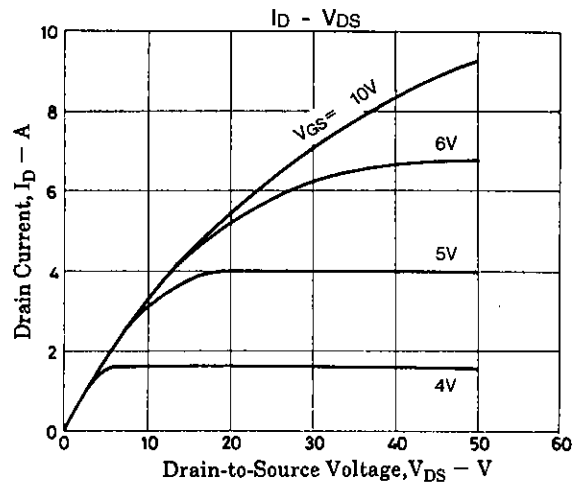
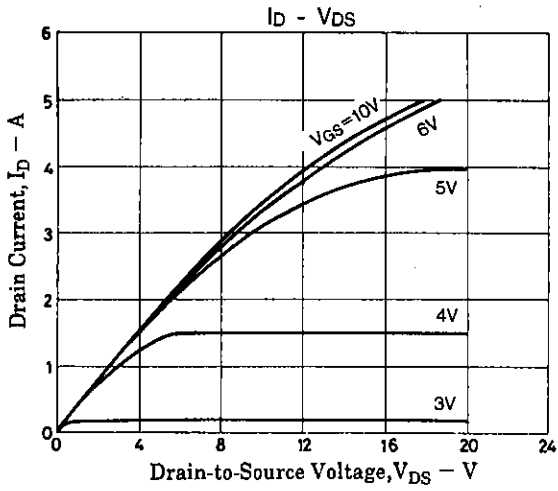
(unit : mm)

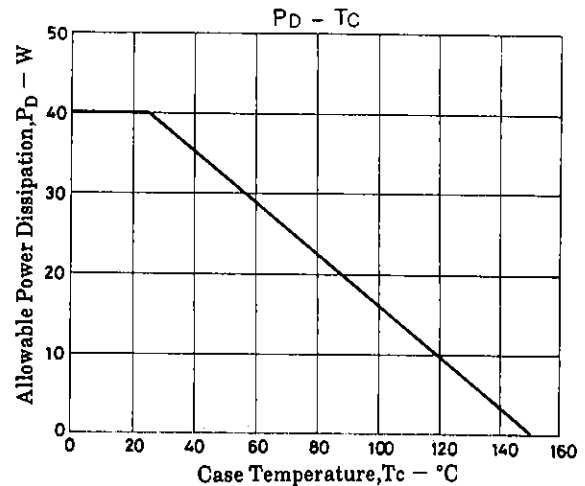
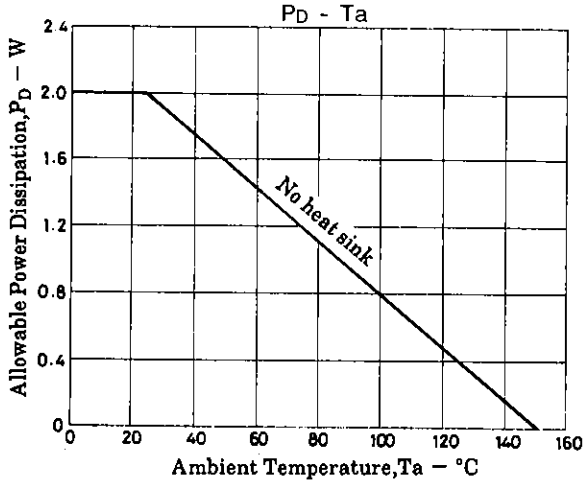
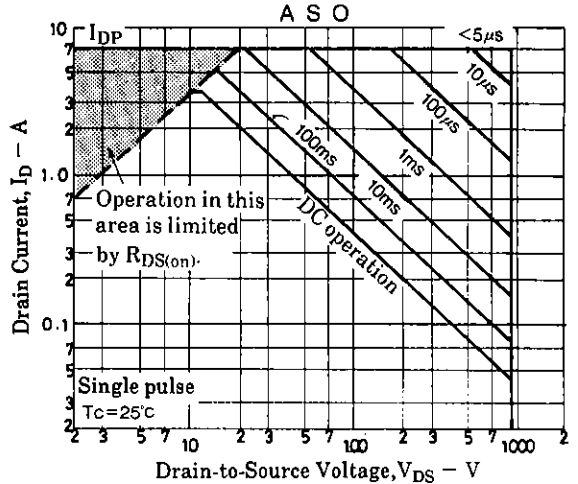
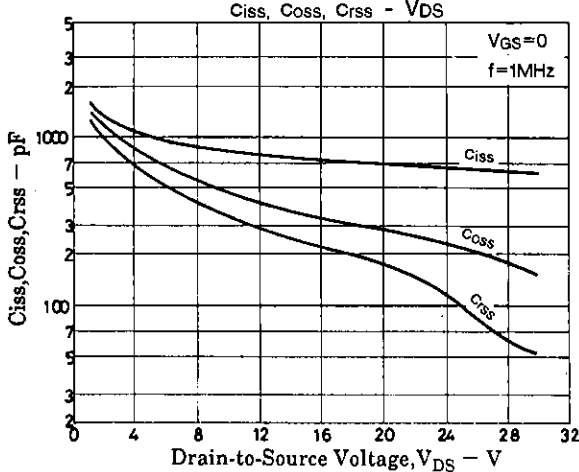
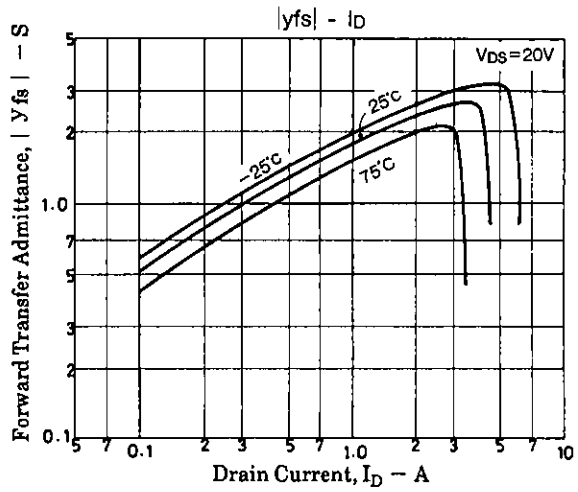
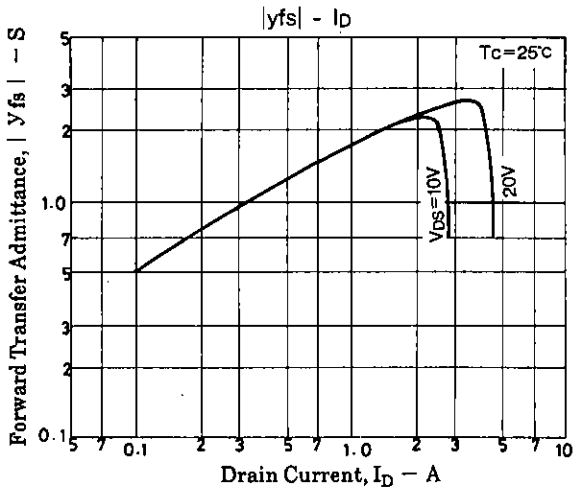


1 : Gate
2 : Drain
3 : Source

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