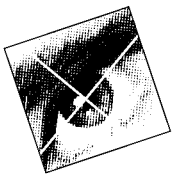


CIRCUIT DESCRIPTION

Pin Descriptions

This chapter begins with a table describing each pin and its function (Table 1), followed by a pinout diagram (Figure 1) and a detailed functional block diagram (Figure 2).

Table 1. Pin Descriptions *(1 of 2)*

Pin Name	I/O	Pin No.	Description
CLK	I	25	Pixel clock input (TTL compatible). A clock frequency 2 times the luminance sample rate should be applied
VSYNC*	I/O	28	Vertical synchronization input/output (TTL compatible). VSYNC* is registered by the rising edge of CLK.
HSYNC*	I/O	29	Horizontal synchronization input/output (TTL compatible). HSYNC* is registered by the rising edge of CLK.
P[7:0]	I	17–24	YCrCb pixel inputs (TTL compatible). P[7:0] is registered on the rising edge of CLK. A higher index corresponds to a greater significance.
MODE[3:0]	I	13–16	Mode configuration inputs (TTL compatible). Described in Mode Selection section.
MASTER	I	12	Timing mode input (TTL compatible). MASTER is registered on the rising edge of CLK. A logical zero configures the device to accept synchronization signals of the HSYNC* and VSYNC* pins; a logical one allows the device to output sync signals on these pins.
CBSWAP	I	11	Pixel sequence configuration input (TTL compatible). Set this pin to a logical zero for the normal pixel sequence. A logical one swaps the Cr and Cb samples.
SVIDEO	I	10	SVIDEO select input (TTL compatible). A logical one configures the device to output Y and C on the DAC outputs. A logical zero configures the device to output composite video on both DAC outputs.
SLEEP	I	9	Power-down control input (TTL compatible). A logical one configures the device for power-down mode. A logical zero configures the device for normal operation. This pin may be connected directly to VAA or GND.

Table 1. Pin Descriptions *(2 of 2)*

Pin Name	I/O	Pin No.	Description
FSADJUST	I	1	Full scale adjust control pin. A resistor connected between this pin and GND controls the full-scale output current on the analog outputs. For standard operation, use the nominal RSET values shown under Recommended Operating Conditions.
COMP	I	2	Compensation pin. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Typically 3.4 V with nominal RSET and typical VDD (5.0 V).
VREF_OUT	O	4	Voltage reference output. This pin can only be used to drive the VREF_IN pin. A 0.1 µf ceramic capacitor must be used to decouple this input to GND, as shown in Figure 19 in the PC Board Layout section. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VRDAC	I	5	DAC current switch reference input. VREF_OUT must be connected directly to this pin.
VBIAS	O	6	DAC bias voltage. Potential normally .7 V less than COMP.
CVBS/C	O	7	Composite video output. Chrominance is output if the SVIDEO pin is high.
CVBS/Y	O	32	Composite video output. Luminance (with blanking and sync) is output if the SVIDEO pin is high.
VAA	–	3	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
VDD	–	27	Digital Power
GND	–	26	Digital Ground
AGND	–	8, 30, 31	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Figure 1. Bt852 32-pin TQFP Pinout Diagram

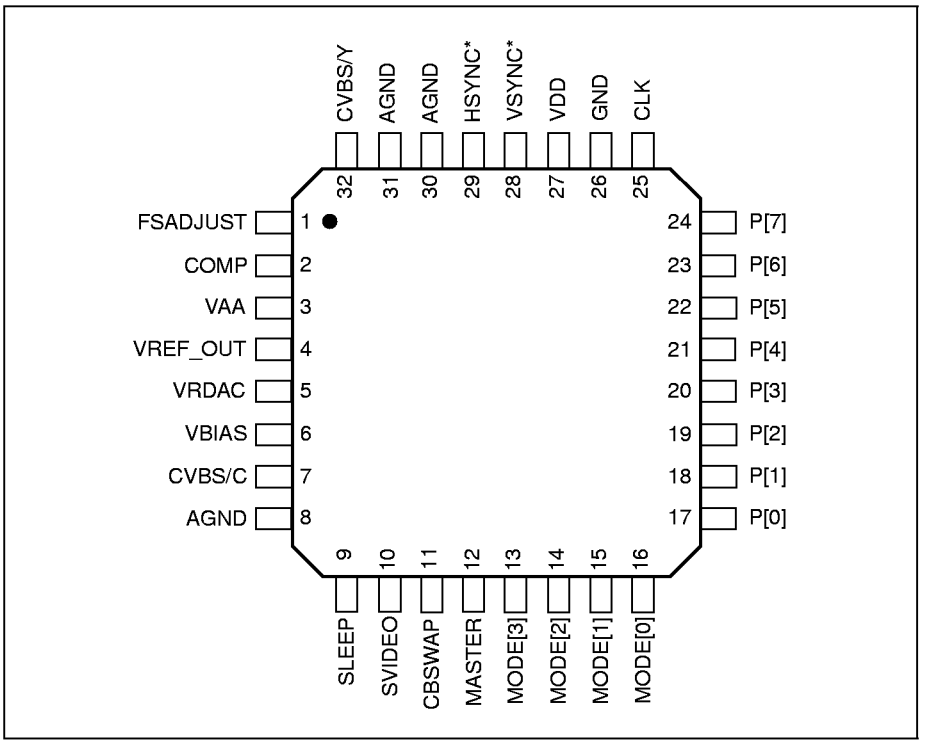
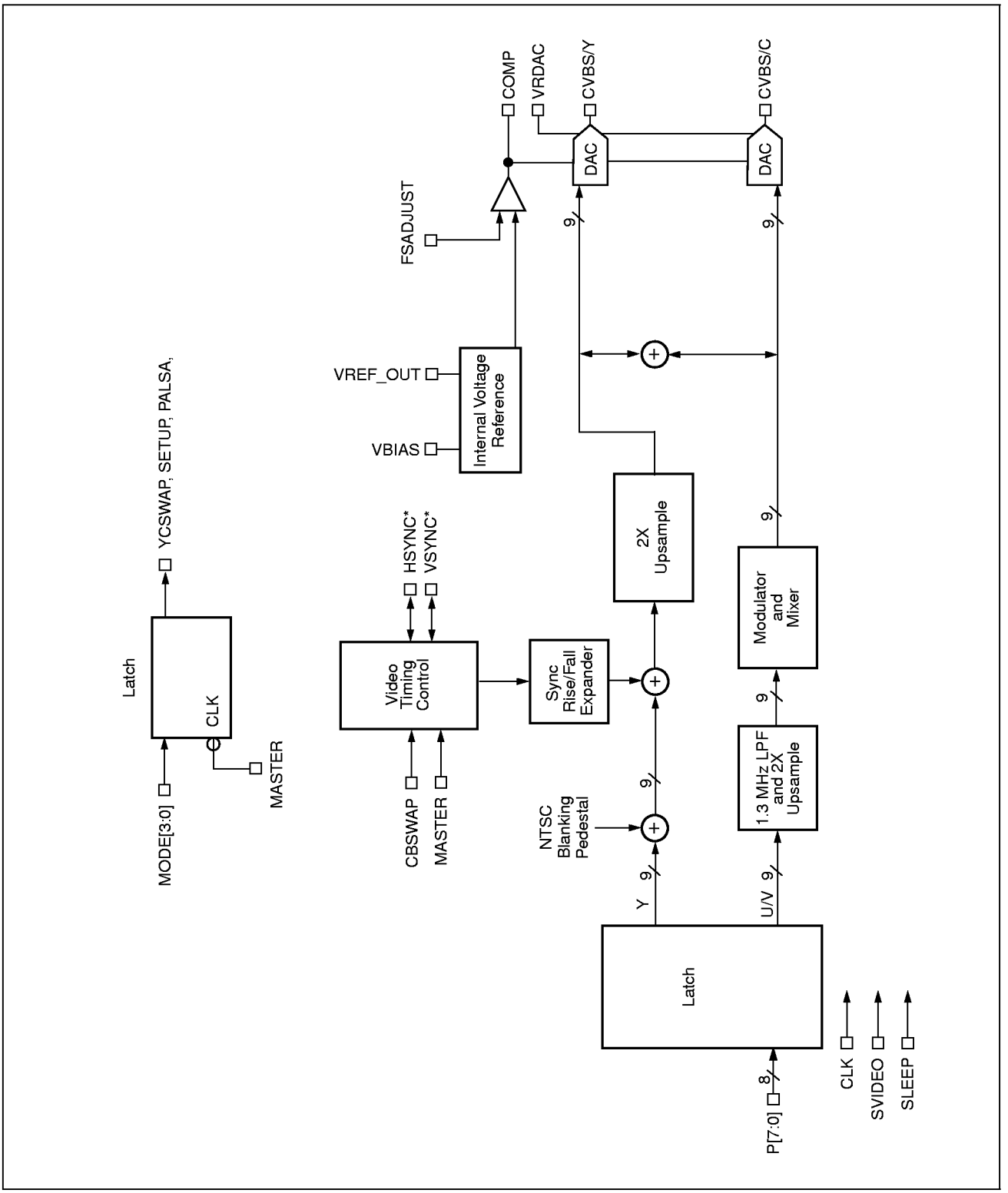


Figure 2. Detailed Block Diagram



Mode Selection

Master mode is selected when MASTER = 1, slave mode is selected when MASTER = 0. Four pins, MODE[3:0], drive seven different configuration registers. The most common operating modes can be selected with these pins while in master mode. In slave mode, the common operating modes are automatically determined from the timing of the incoming HSYNC* and VSYNC* signals.

NOTE: The term "common operating mode" refers to North American NTSC and Western European PAL

Table 2 illustrates the multi-functionality of the mode pins during master and slave mode. To access the more exotic video formats, slave mode is preferred since the necessary registers are always accessible.

If master mode is needed, the less common modes can still be programmed by first registering the modes as a slave, and then switching to a master. During power-up, the MODE[3:0] pins configure the master registers; i.e., EFIELD, PAL625, INTERLACED, and SQUARE are written. Also, during power-up, the slave registers are reset to zero, i.e., YCSWAP, SETUP, and PALSA.

Table 2. Mode Selection

Mode	Pin Description			
	MODE[3]	**MODE[2]**	**MODE[1]**	**MODE[0]**
Slave	YCSWAP	SETUP	PALSA	Reserved
Master	EFIELD	PAL625	INTERLACED	SQUARE
Note: In slave mode, MODE[3:0] must be kept at a logical zero.				

Table 3. Configuration Register Settings

Configuration Register	Slave Mode (MASTER = 0)	Master Mode (MASTER = 1)
EFIELD	NA	Mode 3
PAL625	Determined by HSYNC and VSYNC	Mode 2
INTERLACED	Determined by HSYNC and VSYNC	Mode 1
SQUARE	Determined by HSYNC and VSYNC	Mode 0
YCSWAP	Mode 3	Latched Mode 3
SETUP	Mode 2	Latched Mode 2
PALSA	Mode 1	Latched Mode 1

Listed below are eight internal signals which determine the output video.

EFIELD — EFIELD is used when configured as a master. When EFIELD is set low, the normal vsync* signal is output on the VSYNC* pin (low for 3 lines or 2.5 lines for NTSC or PAL). When EFIELD is set high, Field ID information is output on the VSYNC* pin (VSYNC* is low for Field 1, and high for Field 2).

PAL625 — PAL625 is used when configured as a master. When PAL625 is set low, 525-line operation is selected; when PAL625 is set high, 625-line operation is selected. This mode is set by automatic detection when configured as a slave.

INTERLACED — INTERLACED is used when configured as a master. When INTERLACED is set low, noninterlaced operation is selected; when INTERLACED is set high, 2:1 interlaced operation is enabled. This mode is set by automatic detection when configured as a slave.

SQUARE — SQUARE is used when configured as a master. When SQUARE is set low, 4:3 aspect ratio timing is assumed per CCIR601; when SQUARE is set high, square pixel timing is selected. This mode is set by automatic detection when configured as a slave.

YCSWAP — YCSWAP should normally be set to zero. When configured as a slave, this bit can be set high to swap the luma and chroma samples, thus altering the pixel sequence with respect to the incoming HSYNC* timing reference.

SETUP — SETUP is normally low for the common video modes. The setup and scaling function is toggled when this bit is high. This register is referenced in the "Pixel Input Ranges" section. When SETUP is low, the 7.5 IRE setup is enabled for NTSC and PAL-M with scaling amplified for a 92.5% black-to-white range; other PAL formats have setup disabled with normal 100% scaling. When SETUP is high, the 7.5 IRE setup is disabled for NTSC and PAL-M with 100% black-to-white range scaling; other PAL formats have setup enabled with amplified scaling.

PALSA — PALSA is normally low for the common video modes. South American video standards can be enabled by setting this bit high. For 525-line operation (selected in master mode or detected in slave mode), the PALSA register enables PAL-M for Brazil; in 625-line operation, the PALSA register enables PAL-N-combination for Argentina.

Tables 4a and 4b display valid output video formats in both master and slave modes as a function of the MASTER and MODE[3:0] pins.

Table 4a. Bt852 (Master Mode) Output Video Format Setting

MASTER	MODE[3:0]	Output Format	F_V	F_H	F_{SC}	F_{CLK}	Typical Market
⌐↑	x000	(Normal Setup)					
		CCIR601 NTSC					(North America, Central America, Taiwan)
1	x000	Noninterlaced	60.05	15734.26	3579575	27,000,000	
1	x010	Interlaced	59.94	15734.26	3579545	27,000,000	
		Square NTSC					
1	x001	Noninterlaced	60.05	15734.26	3579575	24,545,454	
1	x011	Interlaced	59.94	15734.26	3579545	24,545,454	
⌐↑	x100	(Special Setup)					
		CCIR601 NTSC					Japan
1	x000	Noninterlaced	60.05	15734.26	3579575	27,000,000	
1	x010	Interlaced	59.94	15734.26	3579545	27,000,000	
		Square NTSC					
1	x001	Noninterlaced	60.05	15734.26	3579575	24,545,454	
1	x011	Interlaced	59.94	15734.26	3579545	24,545,454	
⌐↑	x000	(Normal Setup)					
		CCIR601 PAL BDGHI					(Europe, SE Asia)
1	x100	Noninterlaced	50.08	15625	4433619	27,000,000	
1	x110	Interlaced	50.00	15625	4433619	27,000,000	
		Square PAL BDGHI					
1	x101	Noninterlaced	50.08	15625	4433619	14,750,000	
1	x111	Interlaced	50.00	15625	4433619	14,750,000	
⌐↑	x010	(Normal Setup, SA)					
		CCIR601 PAL -M					Brazil
1	x000	Noninterlaced	60.05	15734.26	3575611	27,000,000	
1	x010	Interlaced	59.94	15734.26	3575611	27,000,000	
		Square PAL-M					
1	x001	Noninterlaced	60.05	15734.26	3575611	24,545,454	
1	x011	Interlaced	59.94	15734.26	3575611	24,545,454	
		CCIR601 PAL -NC					Argentina
1	x100	Noninterlaced	50.08	15625	3582056	27,000,000	
1	x110	Interlaced	50.00	15625	3582056	27,000,000	
		Square PAL-NC					
1	x101	Noninterlaced	50.08	15625	3582056	29,500,000	
1	x111	Interlaced	50.00	15625	3582056	29,500,000	
⌐↑	x110	(Special Setup, SA)					
		CCIR601 PAL -N					(Uruguay, Jamaica, [2.5 H VSYNC])
1	x100	Noninterlaced	50.08	15625	4,433,619	27,000,000	
1	x110	Interlaced	50.00	15625	4,433,619	27,000,000	
		Square PAL-N					
1	x101	Noninterlaced	50.08	15625	4,433,619	29,500,000	
1	x111	Interlaced	50.00	15625	4,433,619	29,500,000	

Table 4b. Bt852 (Slave Mode) Output Video Format Setting

MASTER	MODE[3:0]	Output Format	F_V	F_H	F_{SC}	F_{CLK}	Typical Market
		CCIR601 NTSC					(North America, Central America, Taiwan)
0	x000	Noninterlaced	60.05	15734.26	3579575	27,000,000	
0	x000	Interlaced	59.94	15734.26	3579545	27,000,000	
		Square NTSC					
0	x000	Noninterlaced	60.05	15734.26	3579575	24,545,454	
0	x000	Interlaced	59.94	15734.26	3579545	24,545,454	
		CCIR601 NTSC					Japan
0	x100	Noninterlaced	60.05	15734.26	3579575	27,000,000	
0	x100	Interlaced	59.94	15734.26	3579545	27,000,000	
		Square NTSC					
0	x100	Noninterlaced	60.05	15734.26	3579575	24,545,454	
0	x100	Interlaced	59.94	15734.26	3579545	24,545,454	
		CCIR601 PAL BDGHI					(Europe, SE Asia)
0	x000	Noninterlaced	50.08	15625	4433619	27,000,000	
0	x000	Interlaced	50.00	15625	4433619	27,000,000	
		Square PAL BDGHI					
0	x000	Noninterlaced	50.08	15625	4433619	14,750,000	
0	x000	Interlaced	50.00	15625	4433619	14,750,000	
		CCIR601 PAL -M					Brazil
0	x010	Noninterlaced	60.05	15734.26	3575611	27,000,000	
0	x010	Interlaced	59.94	15734.26	3575611	27,000,000	
		Square PAL-M					
0	x010	Noninterlaced	60.05	15734.26	3575611	24,545,454	
0	x010	Interlaced	59.94	15734.26	3575611	24,545,454	
		CCIR601 PAL -N_c					Argentina
0	x010	Noninterlaced	50.08	15625	3582056	27,000,000	
0	x010	Interlaced	50.00	15625	3582056	27,000,000	
		Square PAL-N_c					
0	x010	Noninterlaced	50.08	15625	3582056	29,500,000	
0	x010	Interlaced	50.00	15625	3582056	29,500,000	
		CCIR601 PAL -N					(Uruguay, Jamaica, [2.5 H VSYNC])
0	x100	Noninterlaced	50.08	15625	4,433,619	27,000,000	
0	x100	Interlaced	50.00	15625	4,433,619	27,000,000	
		Square PAL-N					
0	x100	Noninterlaced	50.08	15625	4,433,619	29,500,000	
0	x100	Interlaced	50.00	15625	4,433,619	29,500,000	

Note: The output video format is determined by the MODE[3:0] pins in conjunction with the HSYNC* and VSYNC* signal timing.

Clock Timing

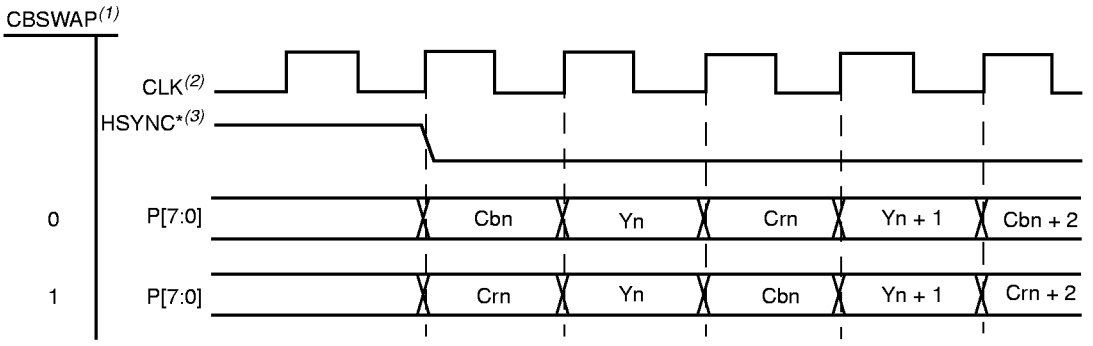
A clock signal with a frequency twice the luminance sampling rate must be present at the CLK pin. All setup and hold timing specifications are measured with respect to the rising edge of this signal.

Pixel Input Timing

Pixel Sequence

Multiplexed Y, Cb, and Cr data is input through the P[7:0] inputs. By default, the input sequence for active video pixels must be Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, etc., in accordance with CCIR-656. This pattern begins during the first CLK period after the falling edge of HSYNC* (regardless of the setting of SLAVE/MASTER mode). The order of Cb and Cr can be reversed by setting the CBSWAP pin. Figure 3 illustrates the timing. If the pixel stream input to the Bt852 is off by one CLK period, the Bt852 can lock to the pixel stream by setting the YCSWAP register. This would solve the problem of having the Y and Cr/Cb pixels swapped.

Figure 3. Pixel Sequence



Notes: (1). CBSWAP is pin 11.
(2). Pixel transitions must occur observing setup and hold timing about the rising edge of CLK.
(3). Pixel sequence will begin with Cbn at 4 x m clock periods following the falling edge of HSYNC*, where m is an integer.

Video Timing

The width of the analog horizontal sync pulses and the start and end of color burst is automatically calculated and inserted for each mode according to CCIR-624-4. Color burst is disabled on appropriate scan lines. Serration and equalization pulses are generated on appropriate scan lines. In addition, rise and fall times of sync, and the burst envelope are internally controlled. Video timing figures follow the text in this section.

Sync and Burst Timing

Table 5 lists the resolutions and clock rates for the various modes of operation. Table 6 lists the horizontal counter values for the end of horizontal sync, start of color burst, end of color burst, front porch, back porch, and the first active pixel for the various modes of operation. The front porch is the interval before the next expected falling HSYNC* when outputs are automatically blanked.

The horizontal sync width is measured between the 50% points of the falling and rising edges of horizontal sync.

The start of color burst is measured between the 50% point of the falling edge of horizontal sync and the first 50% point of the color burst amplitude (nominally +20 IRE for NTSC/PAL–M and 150 mV for PAL–B, D, G, H, I, N, N_c above the blanking level).

The end of color burst is measured between the 50% point of the falling edge of horizontal sync and the last 50% point of the color burst envelope (nominally +20 IRE for NTSC/PAL–M and 150 mV for PAL–B, D, G, H, I, N, N_c above the blanking level).

NOTE: PAL-N_c refers to "Combination N," the PAL format used in Argentina.

Table 5. Field Resolutions and Clock Rates for Various Modes of Operation

Operating Mode	Active Luminance Resolution (pixels)			Total Resolution (pixels)			Luminance Pixel Frequency (MHz)
	Horizontal	Vertical		Horizontal	Vertical		
	Porch = 0	Non Interlaced Field	Interlaced Frame		Non Interlaced	Interlaced	
NTSC/PAL–M CCIR601	711	241	482	858 ± 1	262 ± 1/4	262.5 ± 1/4	13.5000
PAL–B, D, G, H, I, N, Nc CCIR601	702	287	575	864 ± 1	312 ± 1/4	312.5 ± 1/4	13.5000
NTSC/PAL–M Square Pixel	647	241	482	780 ± 1	262 ± 1/4	262.5 ± 1/4	12.2727
PAL–B, D, G, H, I, N, Nc Square Pixel	767	287	575	944 ± 1	312 ± 1/4	312.5 ± 1/4	14.7500

Notes: 1. Tolerances apply to slave mode. Cumulative errors over color frame interval may result in subcarrier glitches.
2. Due to upsampling filter response, pixels near the boundary of the active definition will be reduced in amplitude due to averaging with the blank level.

Table 6. Horizontal Counter Values for Various Video Timings

Operating Mode	Horizontal Counter Value											
	Equalization Pulse Width		Horizontal/Serration Pulse Width		Start of Burst		Duration of Burst		Back Porch		Front Porch(1)	
	2*TCLK	µs	HCNT	µs	HCNT	µs	HCNT	µs	HCNT	µs	HCNT	µs
NTSC CCIR601	32	2.37	63	4.67	72	5.33	34	2.52	127	9.41	20	1.48
PAL–M CCIR601	32	2.37	63	4.67	78	5.78	34	2.52	127	9.41	20	1.48
NTSC Square	29	2.36	58	4.73	65	5.30	31	2.53	115	9.37	18	1.47
PAL–M Square	29	2.36	58	4.73	71	5.79	31	2.53	115	9.37	18	1.47
PAL-B CCIR601	32	2.37	63	4.67	76	5.63	30	2.22	142	10.52	20	1.48
PAL–N_C CCIR601	32	2.37	63	4.67	76	5.63	34	2.52	142	10.52	20	1.48
PAL–B Square	35	2.37	69	4.68	83	5.63	33	2.24	155	10.51	22	1.49
PAL-N_C Square(2)	35	2.37	69	4.68	83	5.63	37	2.51	155	10.51	22	1.49

Notes: (1). In slave mode, since Front Porch timing is triggered by the previous HSYNC pulse, any deviation from nominal line length can affect the front porch duration.
(2). PAL-N_C refers to the PAL format used in Argentina (Combination N).
3. HCNT refers to the number of luminance pixel periods; with respect to the CLK pin, there are twice as many CLK periods as HCNT periods.
4. Odd counts at porch transitions indicate invalid chroma framing

Master Mode

Horizontal sync (HSYNC* and vertical sync (VSYNC*) are generated from internal timing and optional software bits. HSYNC*, HSYNCO*, VSYNC*, and VSYNCO* are output following the rising edge of CLK.

The horizontal counter is incremented on every other rising edge of CLK. After reaching the appropriate value (determined by the mode of operation), it is reset to one, indicating the start of a new line. HSYNC* falls six CLK edges later.

The vertical counter is incremented at the start of each new line. After reaching the appropriate value, determined by the mode of operation (see Table X), it is reset to one, indicating the start of a new field (interlaced operation) or frame (non-interlaced operation). VSYNC* is asserted for 3 or 2.5 scan lines for 262/525 line and 312/625 line, respectively.

Slave Mode

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are inputs that are registered on the rising edge of CLOCK. The horizontal counter is incremented on the rising edge of CLOCK. Two clock cycles after falling edge of HSYNC*, the counter is reset to one, indicating the start of a new line. The vertical counter is incremented on the falling edge of HSYNC*. A falling edge of VSYNC* resets it to one, indicating the start of a new field (interlaced operation) or frame (noninterlaced operation).

A falling edge of VSYNC* occurring within ±1/4 of a scan line from the falling edge of HSYNC* cycle time (line time) indicates the beginning of Field 1. A falling edge of VSYNC* occurring within ±1/4 scan line from the mid point of the line indicates the beginning of Field 2. Referring to Figures 4–6b, start of VSYNC occurs on the falling HSYNC* at the beginning of the next expected Field 2.

The operating mode (NTSC/PAL, interlaced/noninterlaced, Square Pixel/CCIR-601) can be programmed with the MODE[4:0] bits when the SETMODE bit is set high. Alternatively, when SETMODE is low, the mode is automatically detected in slave mode. For example, 525-line operation is assumed, 625-line operation is detected by the number of HSYNC* edges between VSYNC* edges. Interlaced operation is detected by observing the sequence of Field 1 or Field 2; if the field timing (Field 1 follows Field 1, Field 2 follows Field 2) is repeated, then noninterlaced mode is assumed. The frequency of operation (square pixels or CCIR-601) for both PAL and NTSC is detected by counting the number of clocks per line. The pixel rate is assumed to be 13.5 MHz unless the exact horizontal count for square pixels, ±1 count, is detected in between two successive falling edges of HSYNC*.

NOTE: Square pixel 625-line operation with this sequence requires one frame to stabilize.

Burst Blanking

For interlaced NTSC, color burst information is automatically disabled on scan lines 1–9 and 264–272, inclusive. (SMPTE line numbering convention.)

For interlaced PAL-M, color burst information is automatically disabled on scan lines 1–11 and 263–273, inclusive. (SMPTE line numbering convention.)

For interlaced PAL-B, D, G, H, I, N, N_c, color burst information is automatically disabled on scan lines 1–6, 310–318, and 623–625, inclusive, for fields 1, 2, 5, and 6. During fields 3, 4, 7, and 8, color burst information is disabled on scan lines 1–5, 311–319, and 622–625, inclusive.

For noninterlaced NTSC, color burst information is automatically disabled on scan lines 1–6 and 261–262, inclusive.

For noninterlaced PAL-M, color burst information is automatically disabled on scan lines 1–8 and 260–262, inclusive.

For noninterlaced PAL-B, D, G, H, I, N, N_c, color burst information is automatically disabled on scan lines 1–6 and 310–312, inclusive. See Figures 4–9.

Vertical Blanking Intervals

For interlaced NTSC/PAL-M, scan lines 1–9 and 263–272, inclusive, are always blanked. There is no setup on scan lines 10–21 and 273–284 inclusive. All displayed lines in the vertical blanking interval (10–21 and 273–284 for interlaced NTSC/PAL-M; 7–13 and 320–335 for interlaced PAL-B, D, G, H, I, N, N_c) are forced to blank.

For interlaced PAL-B, D, G, H, I, N, N_c, scan lines 1–6, 311–318, and 624–625, inclusive, during fields 1, 2, 5, and 6, are always blanked. During fields 3, 4, 7, and 8, scan lines 1–5, 311–319, and 624–625, inclusive, are always blanked.

For noninterlaced NTSC/PAL-M, scan lines 261–6, inclusive, are always blanked. For noninterlaced PAL-B, D, G, H, I, N, N_c, scan lines 1–6 and 311–312, inclusive, are always blanked (CCIR624 line numbering).

Digital Processing

Once the input data is converted into internal YUV format, the UV components are low-pass filtered with a filter response shown in Figure 10a (linearly scalable by clock frequency). The Y and filtered UV components are upsampled to CLK frequency by a digital filter whose response is shown in Figures 11a and 11b.

Subcarrier Generation

To maintain a synchronous subcarrier relative to HSYNC*, the subcarrier phase is reset every frame for NTSC and every 8 fields for PAL. The SCA phase is non-zero and depends upon the clock frequency and the video format.

For a perfect clock input, the burst frequency is 4.43361875 MHz for PAL-B, D, G, H, I, N, 3.57561149 MHz for PAL-M, 3.58205625 MHz for PAL-N_c (Argentina), 3.579545 MHz for NTSC interlaced, and 3.579575 MHz for NTSC noninterlaced.

Noninterlaced Operation

When in noninterlaced master mode, the Bt852 always displays Field 1, meaning that the falling edges of HSYNC* and VSYNC* will be output coincidentally.

A 30 Hz offset will be added to the color subcarrier frequency while in NTSC mode so that the color subcarrier phase will be inverted from field to field. Subcarrier phase is reset to zero upon rising SLEEP and every four fields for NTSC or eight fields for PAL.

Transition from interlaced to noninterlaced in master mode occurs during Field 1 to prevent synchronization disturbance. In slave mode, transition occurs after a subsequent falling edge of VSYNC*.

NOTE: Consumer VCRs can record noninterlaced video with minor noise artifacts, but special effects (e.g., scan > 2x) may not function properly.

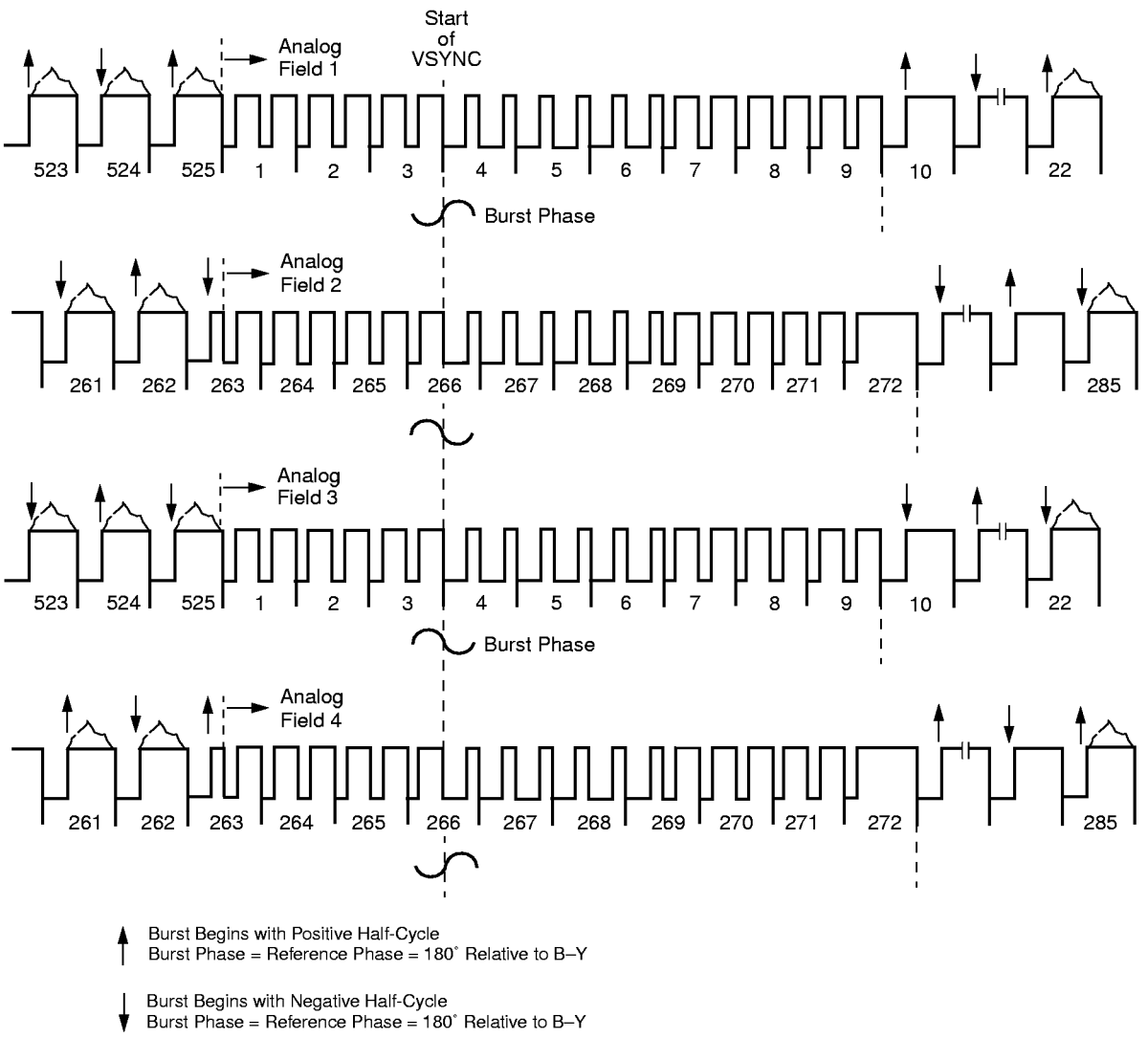
Power-Down Mode

In power-down mode (SLEEP pin set to 1), the internal clock is stopped, an internal reset is forced and the DACs are powered down. When returned high, the device starts from a reset state (horizontal and vertical counters = 0, which is the start

of VSYNC in Field 1). This mode should be set when the Bt852 may be subjected to clock frequencies outside its functional range.

If Master = 1, the HSYNC* and VSYNC* pins remain driven to the value previously output before SLEEP was activated and power down current is dependent on loading on the HSYNC* and VSYNC* pins.

Figure 4. Interlaced 525-Line (NTSC) Video Timing



Note: SMPTE line numbering convention rather than CCIR-624 is used.

Figure 5. Interlaced 525-Line (PAL-M) Video Timing

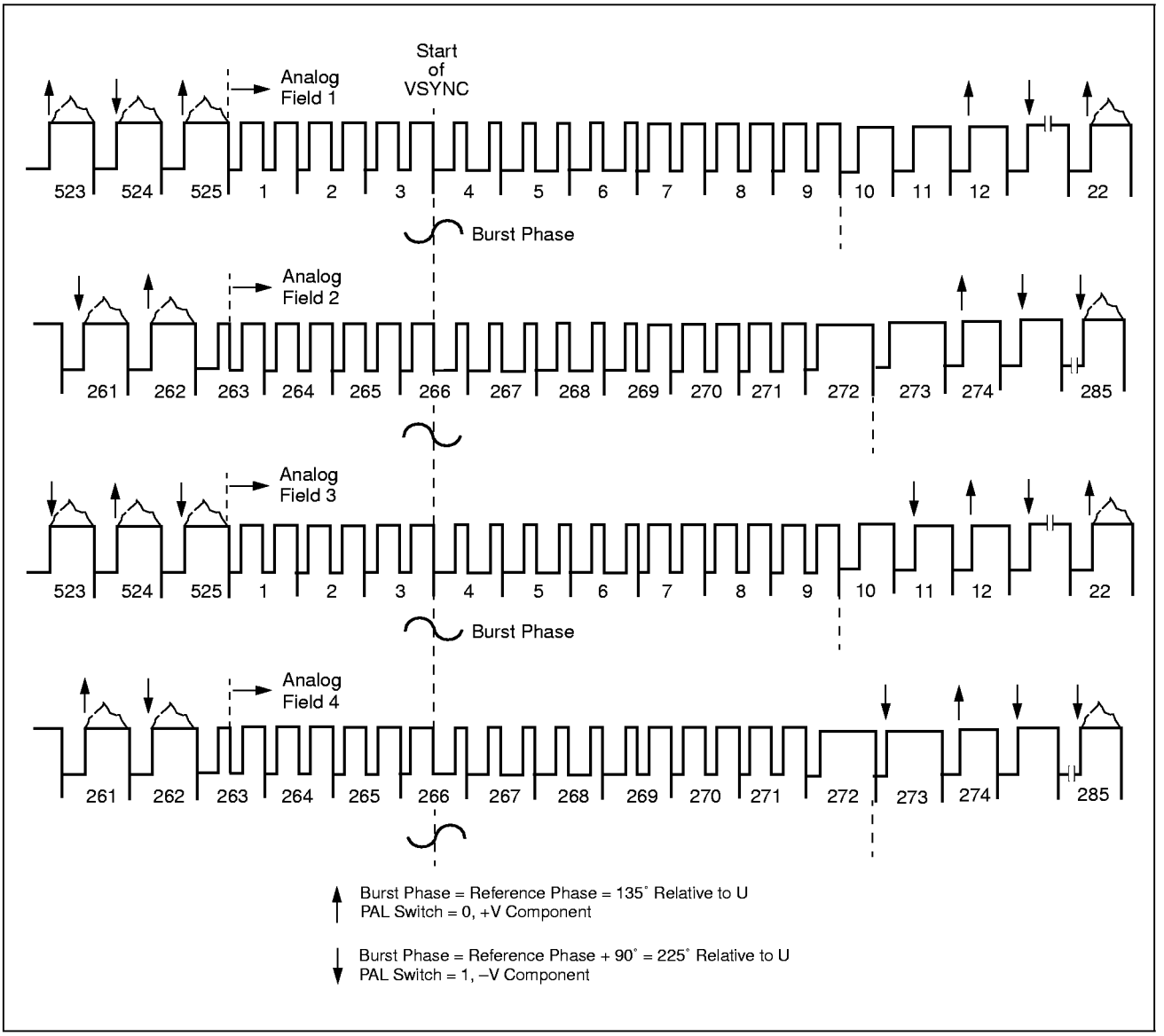


Figure 6a. Interlaced 625-Line (PAL-B, D, G, H, I, N, N_c) Video Timing (Fields 1–4)

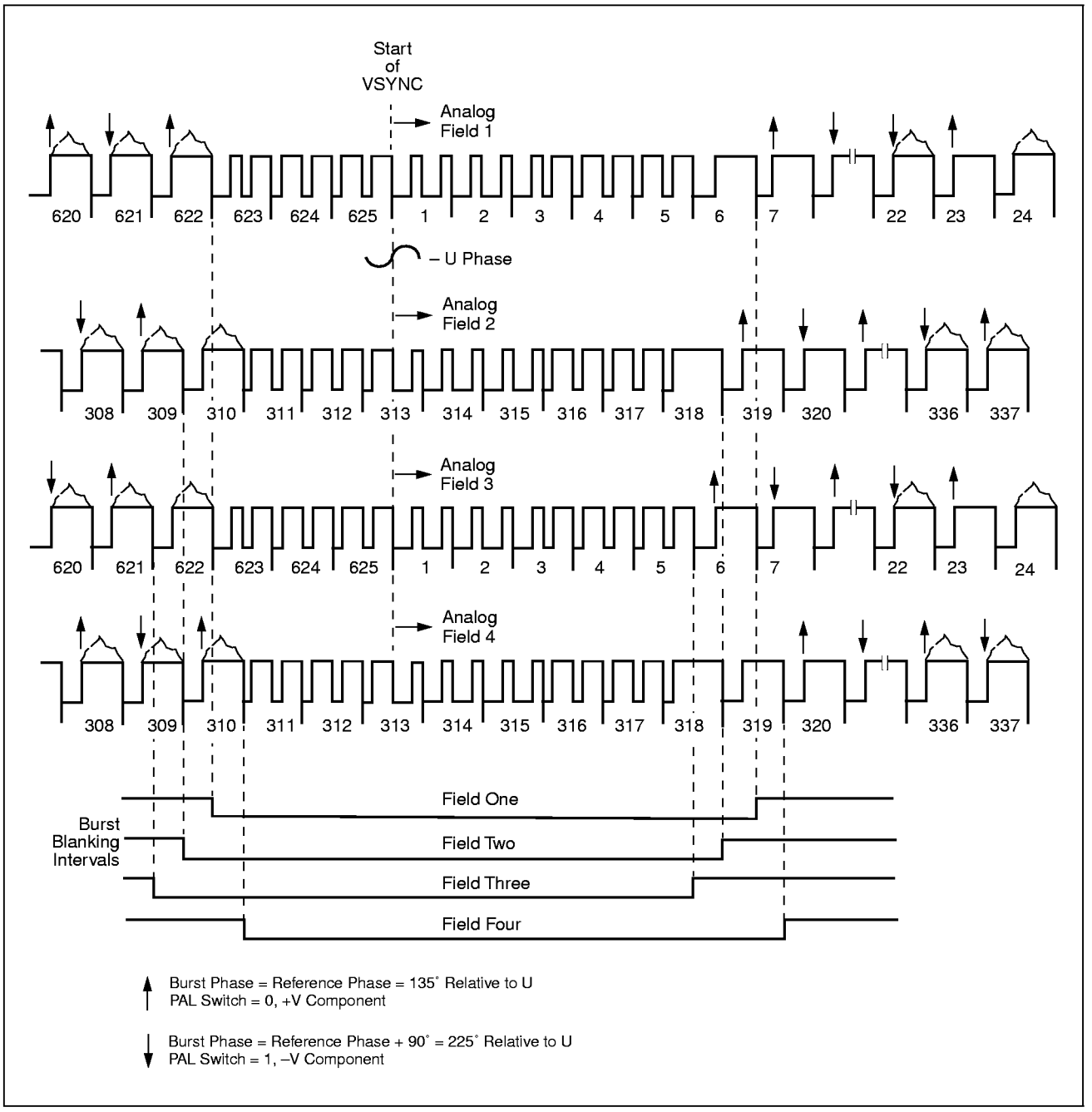


Figure 6b. Interlaced 625-Line (PAL-B, D, G, H, I, N, N_c) Video Timing (Fields 5–8)

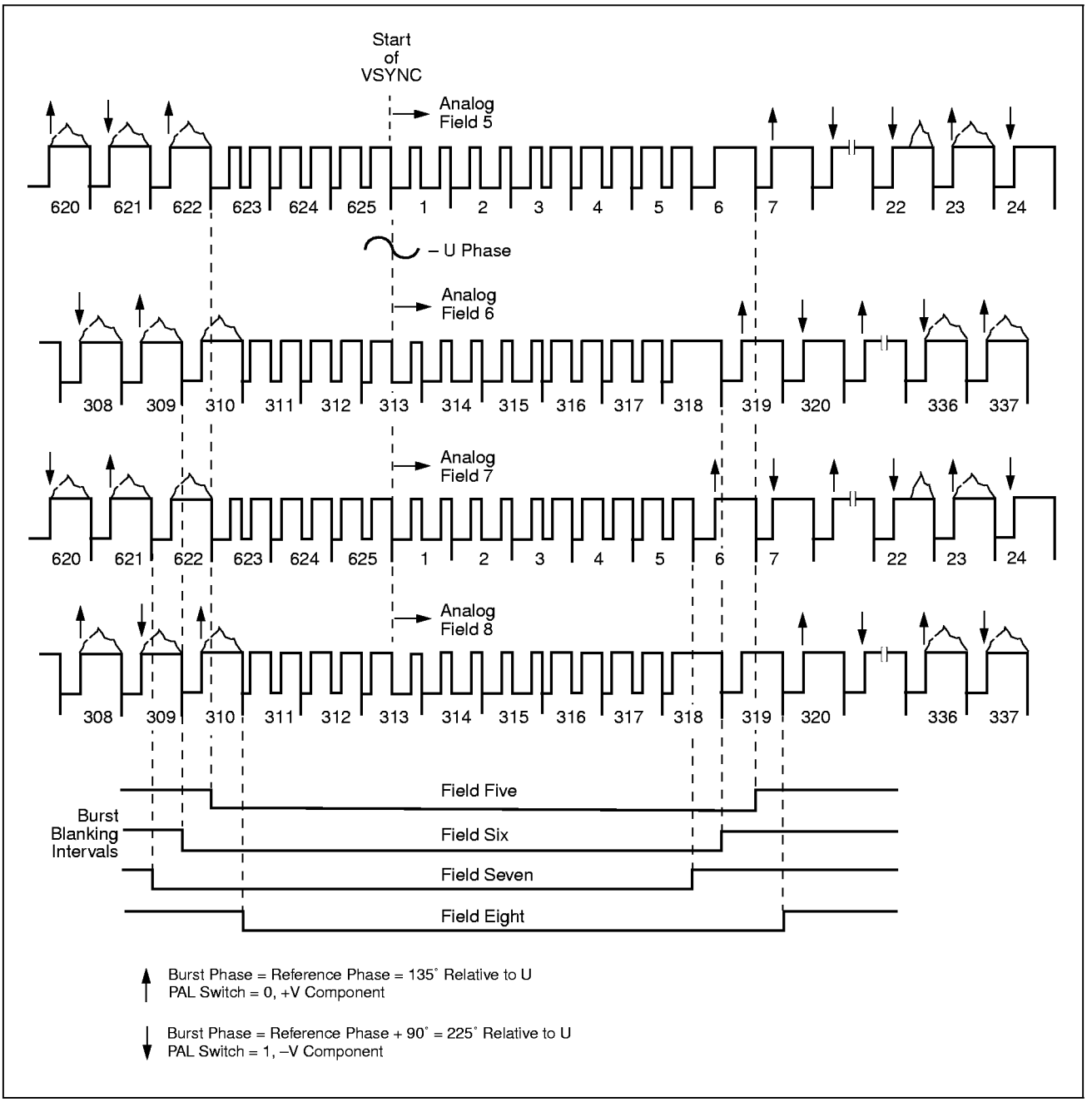
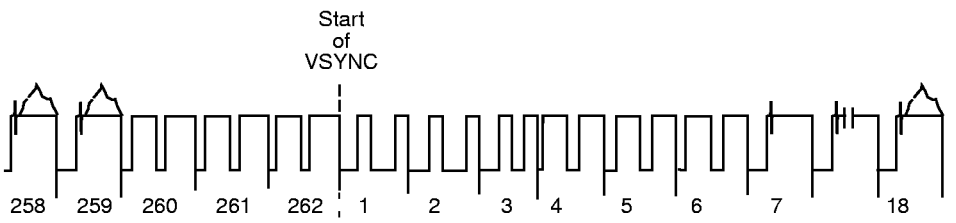
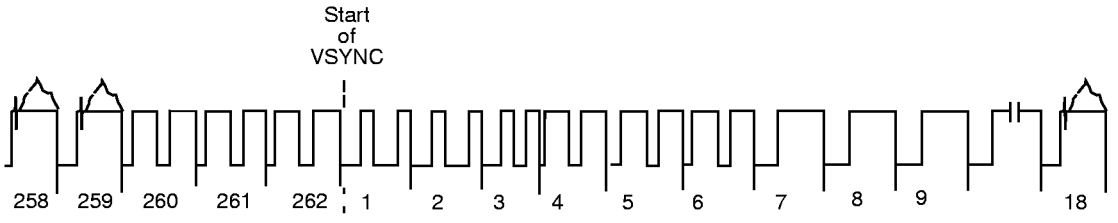


Figure 7. Noninterlaced 262-Line (NTSC) Video Timing



Note: CCIR 624 line numbering convention.

Figure 8. Noninterlaced 262-Line (PAL-M) Video Timing



Note: CCIR 624 line numbering convention.

Figure 9. Noninterlaced 312-Line (PAL-B, D, G, H, I, N, N_C) Video Timing

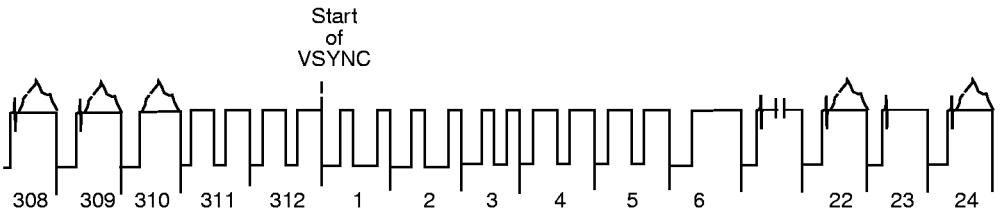


Figure 10a. Three-Stage Chrominance Filter

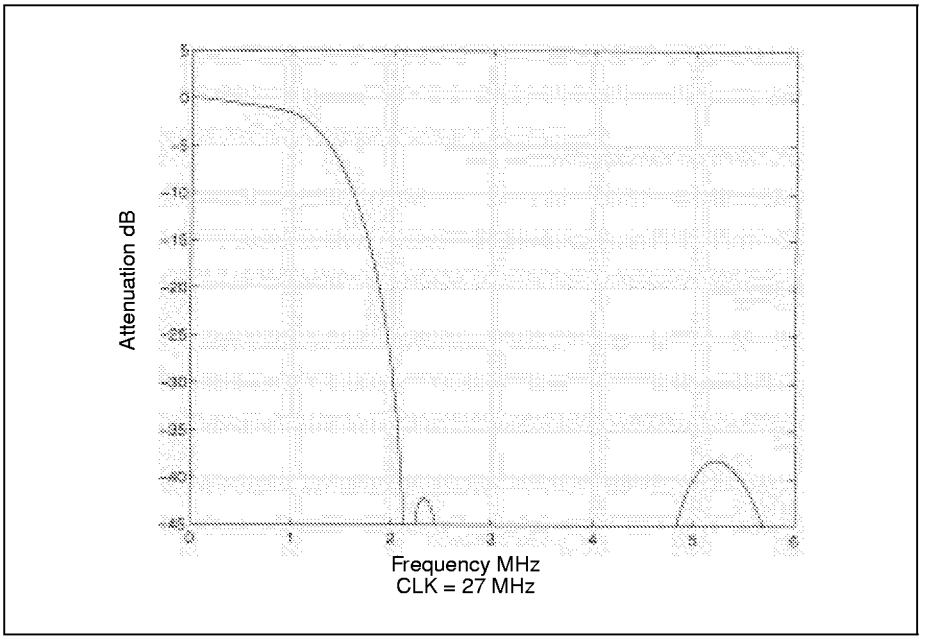


Figure 10b. Three-Stage Chrominance Filter (Passband)

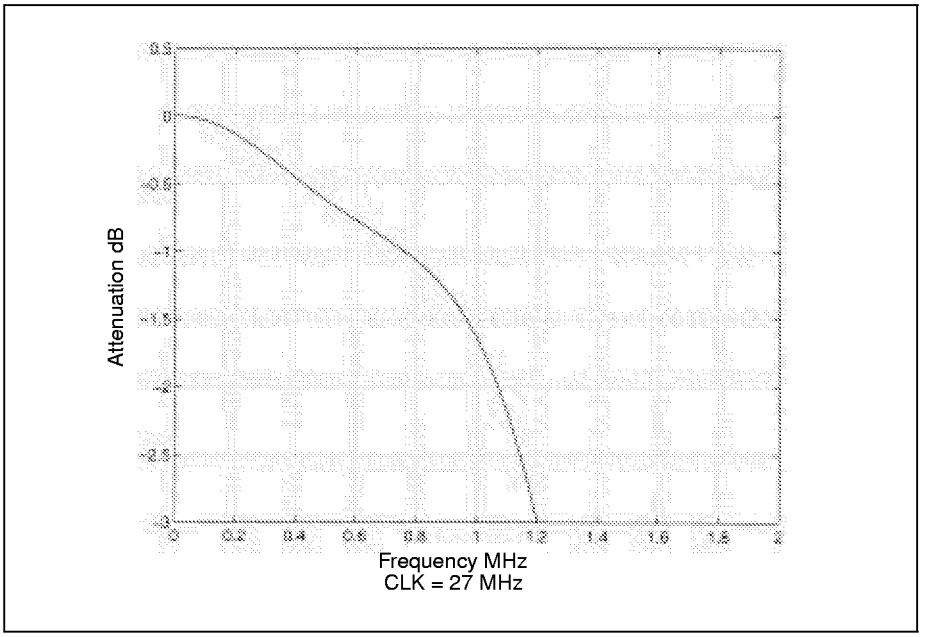


Figure 11a. Luminance 2X Upsampling Filter Response

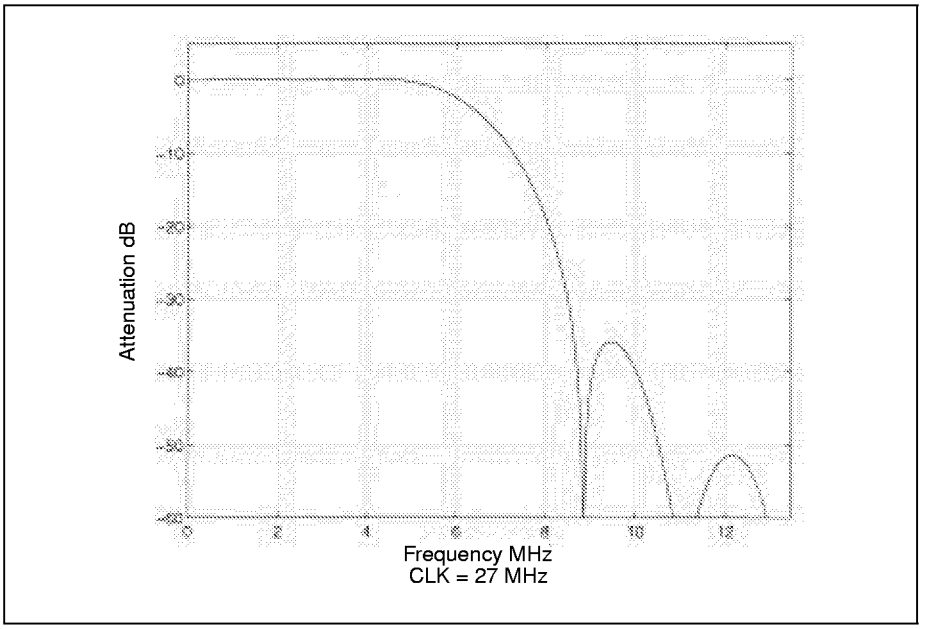


Figure 11b. Luminance 2X Upsampling Filter Response (Passband)

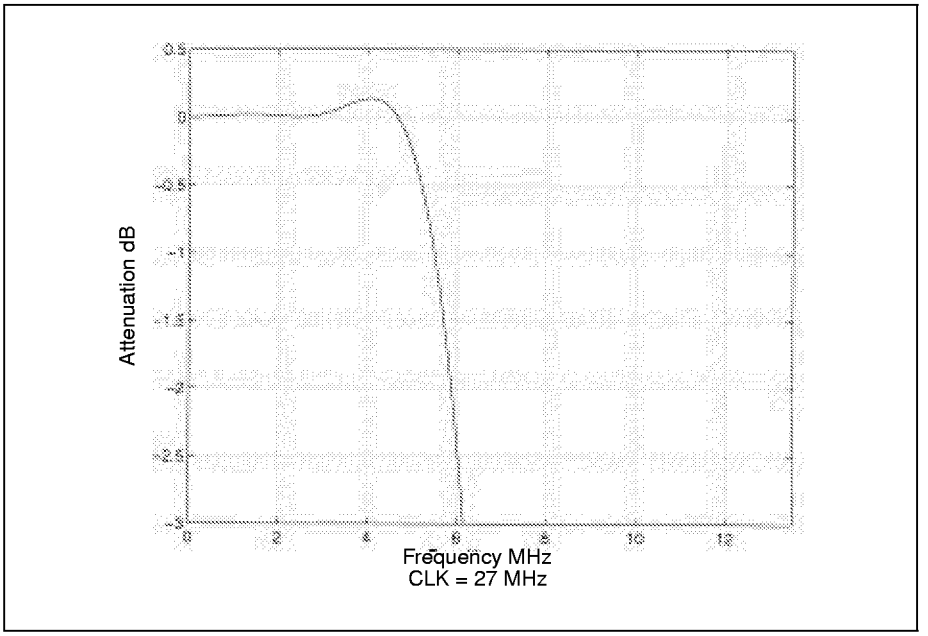


Figure 12a. DAC Sinx/x Response

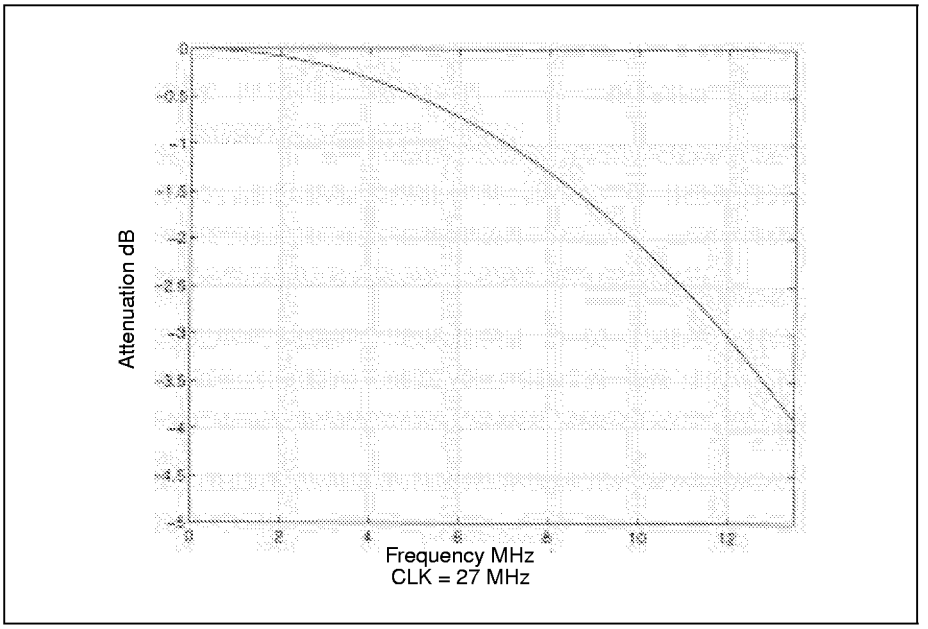
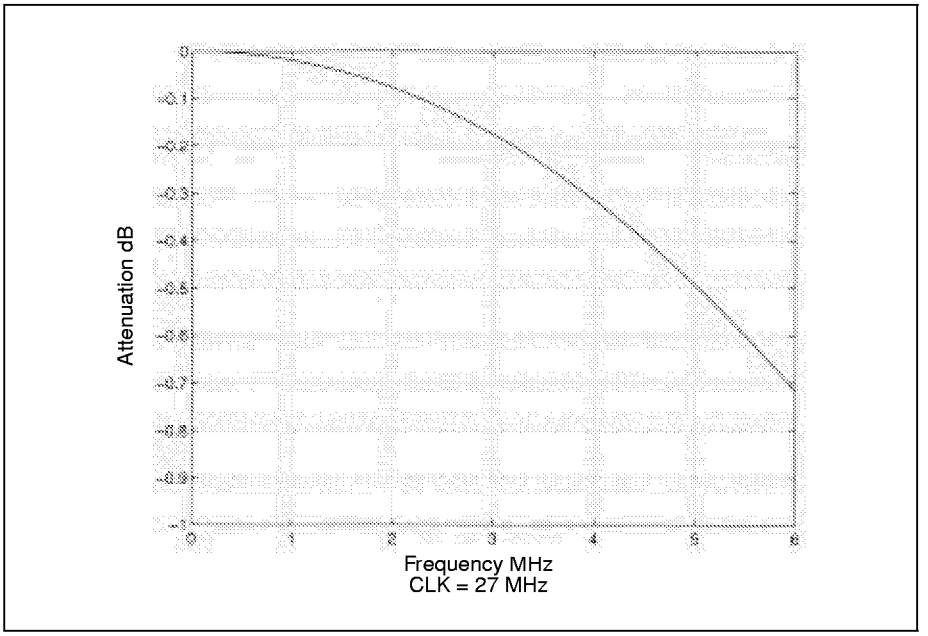


Figure 12b. DAC Sinx/x Response (Passband)



Pixel Input Ranges and Colorspace Conversion

YC Inputs (4:2:2 YCrCb)

Y has a nominal range of 16–235; Cb and Cr have a nominal range of 16–240, with 128 equal to zero. Values of 0 and 255 are interpreted as 1 and 254, respectively. Y values of 1–15 and 236–254, and CrCb values of 1–15 and 241–254, are interpreted as valid linear values.

Alternatively, register bit SETUP will alter luma scaling and disable or enable the 7.5 IRE setup. When the SETUP register is enabled, PAL-B, D, G, H, I, N, N_c video can be generated using NTSC/PAL-M blanking levels and 7.5 IRE setup, and NTSC/PAL-M pixel scaling is performed (Y range of 16–235 represents 7.5–100 IRE); or, NTSC/PAL-M video can be generated using PAL-B, D, G, H, I, N, N_c scaling (Y range of 16-235 represents 0–100 IRE) without the 7.5 IRE setup. NTSC/PAL-M mode with setup disabled has 2% less black-to-white range than NTSC/PAL-M mode with setup enabled.

Table 7 provides the correct YCrCb codes to produce 100/x/75/x color bars.

Table 7. Color Bar Table

Color	Y Value	Cr Value	Cb Value
White	EB	80	80
Yellow	A2	8E	2C
Cyan	83	2C	9C
Green	70	3A	48
Magenta	54	C6	B8
Red	41	D4	64
Blue	23	72	D4
Black	10	80	80

DAC Coding

White is represented by a DAC code of 400. For PAL-B, D, G, H, I, N, N_c, the standard blanking level is represented by a DAC code of 120. For NTSC/PAL-M, with setup enabled (SETUP bit = 0), the standard blanking level is represented by a DAC code of 114, 1 IRE is equivalent to a DAC code of 2.857. For NTSC/PAL-M with setup disabled (SETUP bit = 1), the standard blanking level is represented by a DAC code of 112, 1 IRE is equivalent to a DAC code of 2.800.

Outputs

All digital-to-analog converters are designed to drive standard video levels into an equivalent 37.5 Ω load. Unused outputs should be connected directly to ground to minimize supply switching currents. Either two composite video outputs or Y/C S-Video outputs are available (selectable by the SVIDEO pin). If the SLEEP pin is high, the DACs are essentially turned off and only the leakage current is present. The D/A converter values for 100% saturation, 100% amplitude color bars are shown in Figures 13–18.

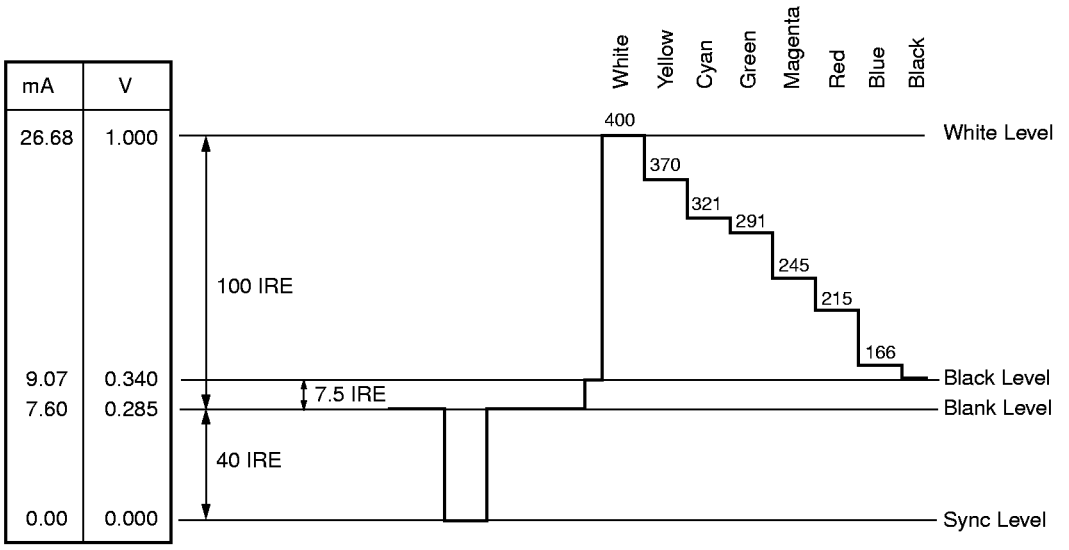
Composite and Luminance (CVBS/Y) Analog Output

When SVIDEO is a logical zero, digital composite video information drives the 9-bit D/A converter that generates the CVBS output. When SVIDEO is a logical one, digital luminance information drives the DAC that generates the analog Y video output (Figures 13, 14, 17, and 18, and Tables 8, 9, 12, and 13.

Composite and Chrominance (CVBS/C) Analog Output

When SVIDEO is a logical zero, digital composite video information drives the 9-bit D/A converter that generates the CVBS output. When SVIDEO is a logical one, digital chrominance information drives the 9-bit D/A converter that generates the analog C video output (Figures 15–18, and Tables 10–13).

Figure 13. 525-Line (NTSC/PAL-M) Y (Luminance) Video Output Waveform



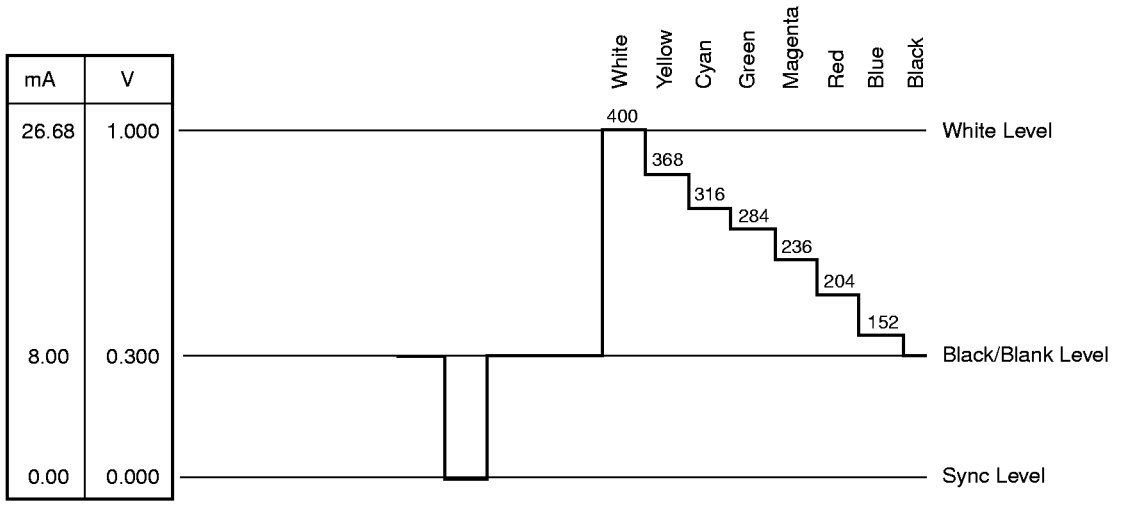
Note: Typical with 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and SETUP = 0. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Table 8. 525-Line (NTSC/PAL-M) Y (Luminance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval
White	26.68	400	0
Black	9.07	136	0
Blank	7.60	114	0
Sync	0	0	1

Note: Typical with 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and SETUP = 0. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Figure 14. 625-Line (PAL-B, D, G, H, I, N, N_C) Y (Luminance) Video Output Waveform



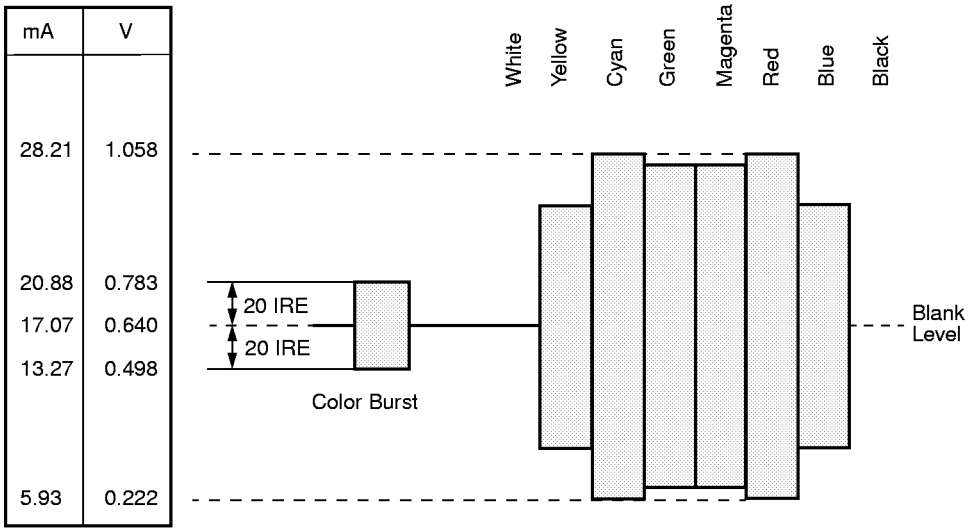
Note: Typical with 37.5 Ω load, VRDAC = VREF_OUT, SETUP = 0, and nominal RSET. CCIR-624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Table 9. 625-Line (PAL-B, D, G, H, I, N, N_C) Y (Luminance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval
White	26.68	400	0
Black	8.00	120	0
Blank	8.00	120	0
Sync	0	0	1

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, SETUP = 0, and nominal RSET. CCIR-624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Figure 15. 525-Line (NTSC/PAL-M) C (Chrominance) Video Output Waveform



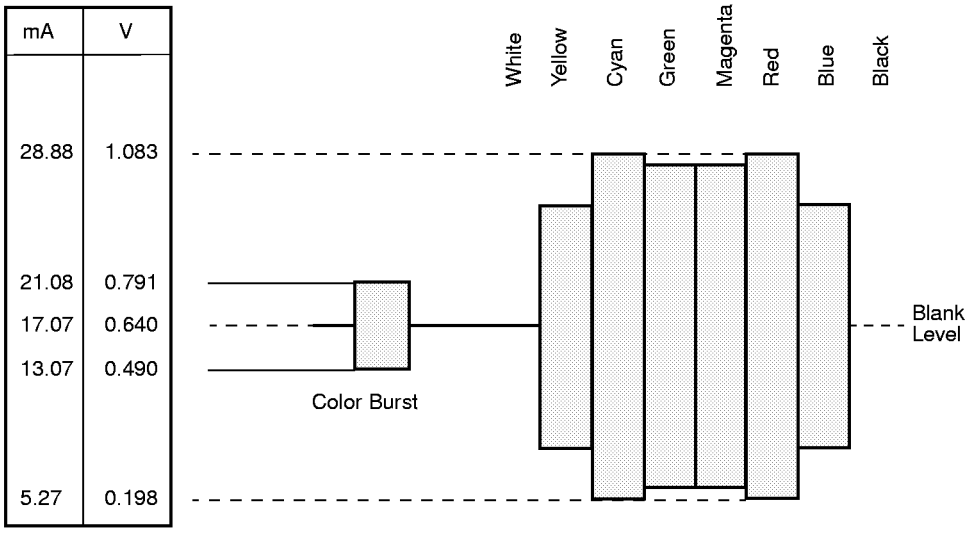
Note: Typical with 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and SETUP = 0. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown. Figures depict peak DAC values, and do not reflect sinx/x loss.

Table 10. 525-Line (NTSC/PAL-M) C (Chrominance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval
Peak Chroma (High)	28.21	423	x
Burst (High)	20.88	313	x
Blank	17.07	256	x
Burst (Low)	13.27	199	x
Peak Chroma (Low)	5.93	89	x

Note: Typical with 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and SETUP = 0. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Figure 16. 625-Line (PAL-B, D, G, H, I, N, N_C) C (Chrominance) Video Output Waveform



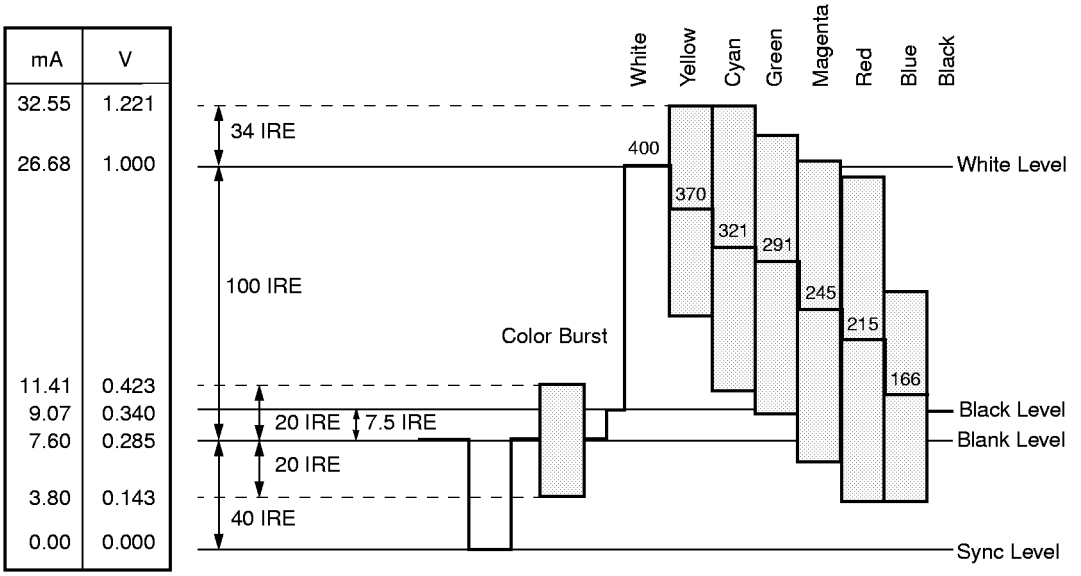
Note: Typical with 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and SETUP = 0. CCIR-624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown. Figures depict peak DAC values, and do not reflect sinx/x loss.

Table 11. 625-Line (PAL-B, D, G, H, I, N, N_C) C (Chrominance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval
Peak Chroma (High)	28.88	433	x
Burst (High)	21.08	316	x
Blank	17.07	256	x
Burst (Low)	13.07	196	x
Peak Chroma (Low)	5.27	79	x

Note: Typical with 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and SETUP = 0. CCIR-624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Figure 17. Composite 525-Line (NTSC/PAL-M) Video Output Waveform



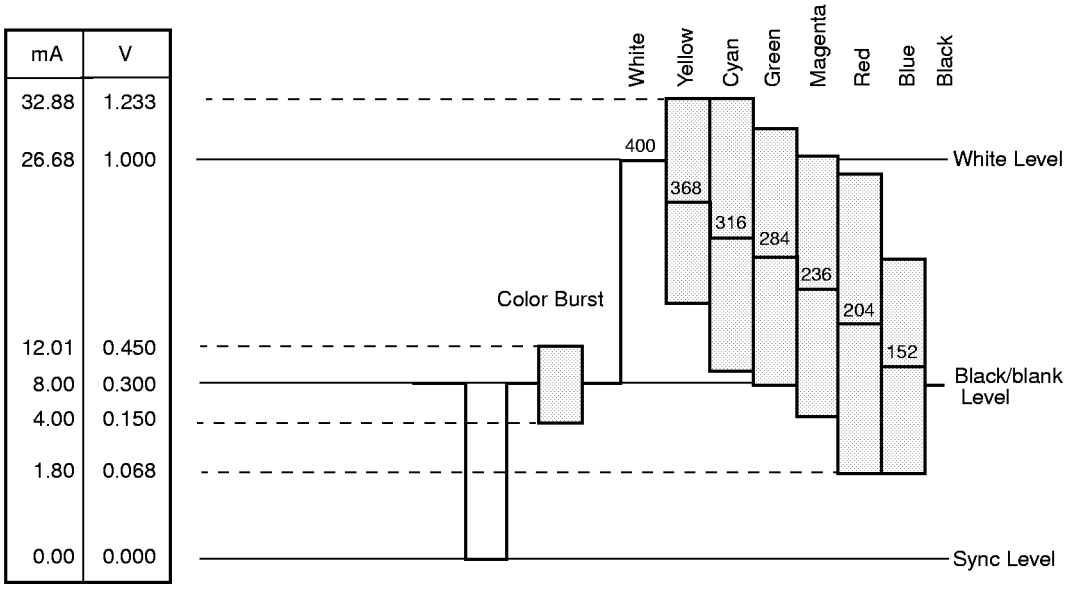
Note: Typical with 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and SETUP = 0. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown. Figures depict peak DAC values, and do not reflect sinx/x loss.

Table 12. Composite 525-Line (NTSC/PAL-M) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval
Peak Chroma (High)	32.55	488	0
White	26.68	400	0
Burst (High)	11.41	171	0
Black	9.07	136	0
Blank	7.60	114	0
Burst (Low)	3.80	57	0
Peak Chroma (Low)	3.20	48	0
Sync	0	0	1

Note: Typical with 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, setup and SETUP = 0. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Figure 18. Composite 625-Line (PAL-B, D, G, H, I, N, N_c) Video Output Waveform

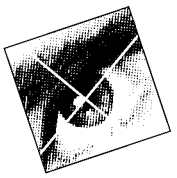


Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, and SETUP = 0. CCIR-624 levels are assumed. 100% amplitude, 100% saturation (100/0/100/0) color bars are shown. Figures depict peak DAC values, and do not reflect sinx/x loss.

Table 13. Composite 625-Line (PAL-B, D, G, H, I, N, N_c) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval
Peak Chroma (High)	32.88	493	0
White	26.68	400	0
Burst (High)	12.01	180	0
Black	8.00	120	0
Blank	8.00	120	0
Burst (Low)	4.00	60	0
Peak Chroma (Low)	1.80	27	0
Sync	0	0	1

Note: Typical with 37.5 Ω load, VRDAC= VREF_OUT, nominal RSET, and SETUP = 0. CCIR-624 levels are assumed. 100% amplitude, 100% saturation (100/0/100/0) color bars are shown.



PC BOARD CONSIDERATIONS

For optimum performance of the Bt852, proper CMOS layout techniques should be studied in the Bt451/457/458 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun.

The layout should be optimized for lowest noise on the power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for ground and power, respectively.

Component Placement

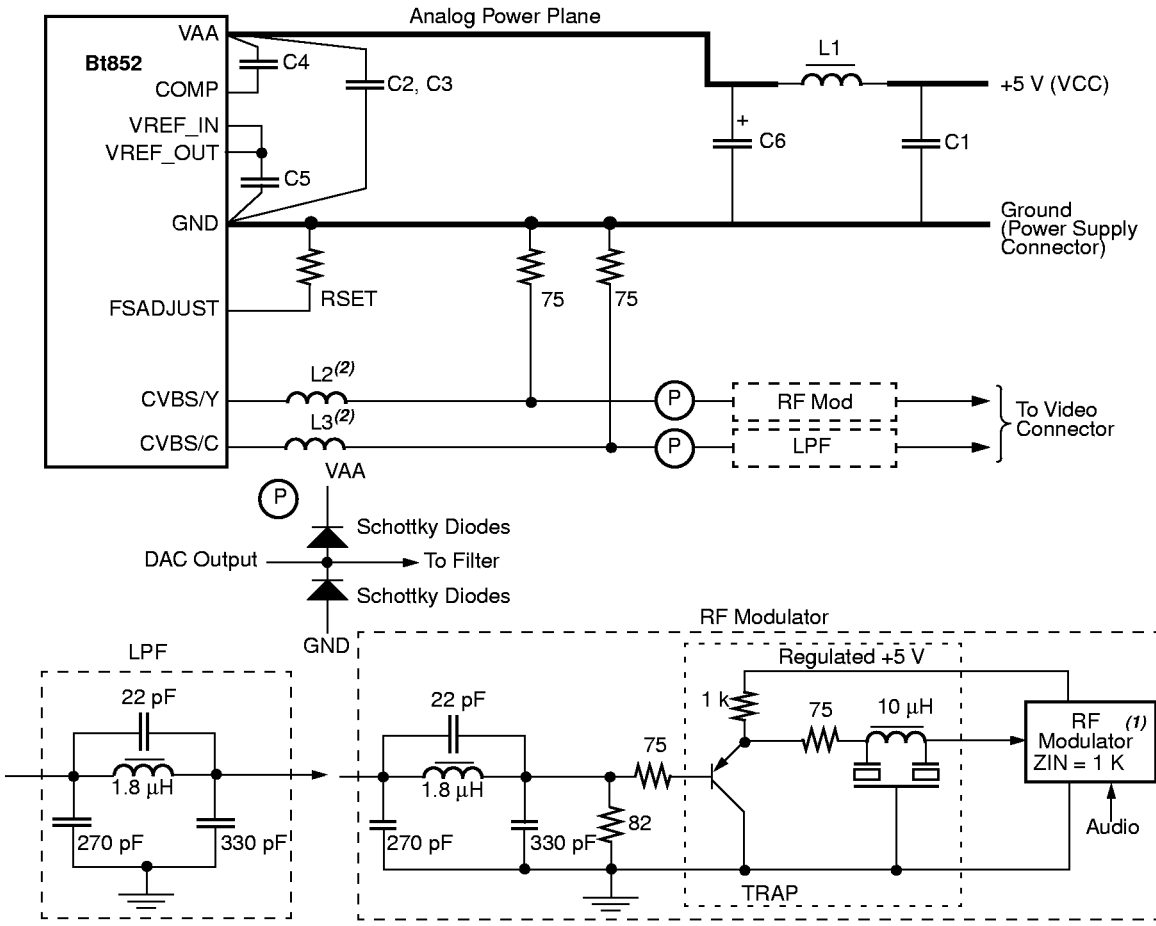
Components should be placed as close as possible to the associated pin. Whenever possible, components should be placed so traces can be connected point to point. The optimum layout enables the Bt852 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

For optimum performance, a common digital and analog ground plane is recommended. Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt852 power pins, VREF circuitry, and COMP decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 19, Table 14. This bead should be located within 3 inches of the Bt852. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2723021447, or TDK BF45-4001.

Figure 19. Typical Connection Diagram (Internal Voltage Reference)



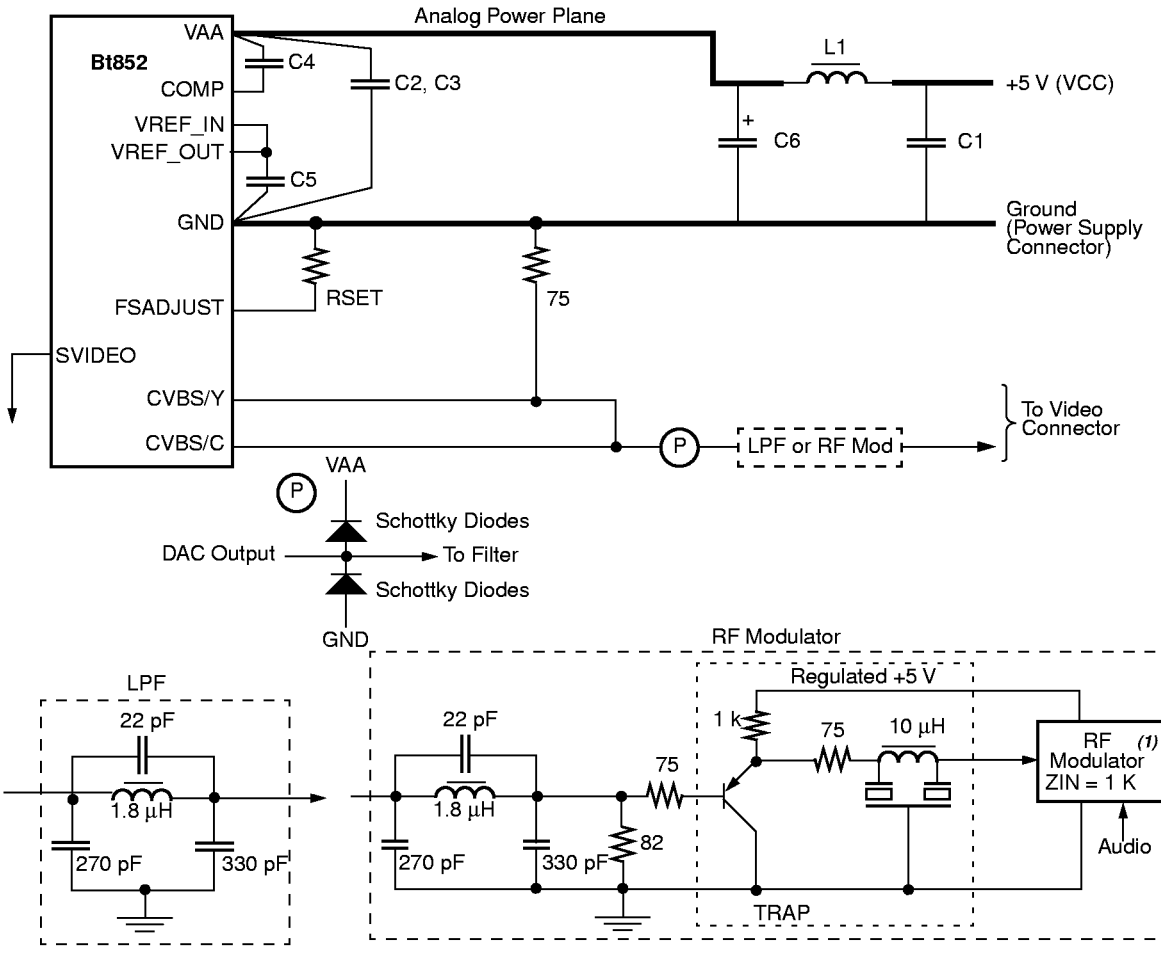
Notes: (1). Some modulators may require AC coupling capacitors (10 µF).
(2). Optional for chroma boost.
3. VREF must be connected to either VREF_OUT or VBIAS.

Table 14. Typical Parts List (Internal Voltage Reference)

Location	Description	Vendor Part Number
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	47 µF Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead - Surface Mount	Fair-Rite 2743021447
L2, L3	Ferrite Bead (z < 300 Ω @ 5 MHz)	ATC LCB0805, Taiyo Yuden BK2125LM182
RSET	1% Metal Film Resistor	Dale CMF-55C
TRAP	Ceramic Resonator	Murata TPSx.xMJ or MB2 (where x.x = sound carrier frequency in MHz)
	Schottky Diodes	BAT85 (BAT54F Dual) HP 5082-2305 (1N6263) Siemens BAT 64-04 (Dual)

Note: Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect Bt852 performance.

Figure 20. Optional Low Power Connection Diagram Single output/10° C Tc Reduction



Notes: (1). Some modulators may require AC coupling capacitors (10 µF).
2. VREF must be connected to either VREF_OUT or VBIAS.

Table 15. Typical Parts List (Internal Voltage Reference)

Location	Description	Vendor Part Number
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	47 µF Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead - Surface Mount	Fair-Rite 2743021447
L2, L3	Ferrite Bead	ATC LCB0805, Taiyo Yuden
RSET	1% Metal Film Resistor	Dale CMF-55C = 300 Ω
TRAP	Ceramic Resonator	Murata TPSx.xMJ or MB2 (where x.x = sound carrier frequency in MHz)
	Schottky Diodes	BAT85 (BAT54F Dual) HP 5082-2305 (1N6263) Siemens BAT 64-04 (Dual)

Table 15. Typical Parts List (Internal Voltage Reference)

Location	Description	Vendor Part Number
Note: Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect Bt852 performance.		

Decoupling

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply performance is obtained with a 0.1 µF ceramic capacitor decoupling each group of VDD pins to GND, and VAA pins to AGND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 47 µF capacitor shown in Figure 19 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 5% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to the closest VAA pin, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

VREF _OUT Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this pin to GND.

VBIAS Decoupling

A 0.1 µf ceramic capacitor should be used to decouple this pin to GND.

Signal Interconnect

Digital Signal Interconnect

The digital inputs to the Bt852 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one-fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt852 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should overlay the ground plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and AGND should be as close as possible to the Bt852 to minimize reflections. Unused DAC outputs should be connected to GND.

Applications Information

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage. Device damage can produce symptoms of catastrophic failure or erratic device behavior with leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided; they could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA and VDD pins are at the same potential, all GND and AGND pins are at the same potential, and that the VAA and VDD supply voltages are applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage.

Clock and Subcarrier Stability

The color subcarrier is derived directly from the CLK input, hence any jitter or frequency deviation of CLK will be transferred directly to the color subcarrier. Jitter within the valid CLK cycle interval will result in hue noise on the color subcarrier on the order of 1.3–1.6 degrees per nanosecond. Random hue noise can result in degradation in AM/PM noise ratio (typically around 40 dB for consumer media such as Videodiscs and VCRs). Periodic or coherent hue noise can result in differential phase error (which is limited to 10 degrees by FCC cable TV standards). Any frequency deviation of CLK from nominal will challenge the subcarrier tracking capability of the destination receiver. This may range from a few parts-per-million (ppm) for broadcast equipment to 100 ppm for industrial equipment to a few hundred ppm for consumer equipment. Greater subcarrier tracking range generally results in poorer subcarrier decoding dynamic range, so that receivers that tolerate jitter and wide subcarrier frequency deviation will introduce more noise in the decoded image. Crystal-based clock sources with maximum deviations of 100 ppm produce the best results for consumer and industrial applications, while temperature-compensated clock sources with tighter tolerances may be warranted for broadcast or more stringent PAL (e.g., type I) applications.

Some applications call for maintaining correct Subcarrier-Horizontal phasing (SC-H) for correct color framing, which requires subcarrier coherence within specified tolerances over a four-field interval for 525-line systems or 8 fields for 625-line systems. Any CLK interruption (even during vertical blanking interval) which results in mis-registration of the CLK input or nonstandard pixel counts per line can result in SC-H excursions outside the NTSC limit of ±40 degrees (reference EIA RS170A) or the PAL limit of ±20 degrees (reference EBU D23-1984).

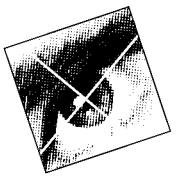
In slave mode, any deviation of the number CLK cycles between HSYNC* falling edges when in slave mode may result in automatic mode switching unless the SETMODE bit is set for the desired mode of operation.

Filtering RF Modulator Connection

The Bt852 internal upsampling filter alleviates external filtering requirements by moving significant sampling alias components above 19 MHz and reducing the sinx/x aperture loss up to the filters passband cutoff of 5.75 MHz. While typical chrominance subcarrier decoders can handle the Bt852 output signals without analog filtering, the higher frequency alias products pose some EMI concerns and may create troublesome images when introduced to an RF modulator. When the video is presented to an RF modulator, it should be free of energy in the region of the aural subcarrier (4.5 MHz for NTSC, 5.5–6.5 MHz for PAL), hence some additional frequency traps may be necessary when the video signal contains fundamental or harmonic energy (as from unfiltered character generators) in that region. Where better frequency response flatness is required, some peaking in the analog filter is appropriate to compensate for residual digital filter losses with sufficient margin to tolerate 10% reactive components.

A three-pole elliptic filter (1 inductor, 3 capacitors) with a 6.75 MHz passband can provide at least 45 dB attenuation (including sinx/x loss) of frequency components above 20 MHz and provide some flexibility for mild peaking or special traps. An inductor value with a self-resonant frequency above 80 MHz is chosen so that its intrinsic capacitance contributes less than 10% of the total effective circuit value. The inductor itself may induce 1% (0.1 dB) loss. Any additional ferrites introduced for EMI control should have less than 5 Ω impedance below 5 MHz to minimize additional losses. The capacitor to ground at the Bt852 output pin is compensated for the parasitic capacitance of the chip plus any protection diodes and lumped circuit traces (about 22 pF + 5 pF/diode). Some filter peaking can be accomplished by splitting the 75 Ω source impedance across the reactive PI filter network. However, this will also introduce some chrominance-luminance delay distortion in the range of 10–20 ns for a maximum of 0.5 dB boost at the subcarrier frequency.

The filter network feeding an RF modulator may include the aforementioned trap, which could take two forms depending on the depth of attenuation and type of resonator device employed. The trap circuit will affect luminance response flatness unless isolated from the low pass filter by an active buffer. Two stage traps may introduce significant chrominance delay, which may warrant inclusion of an active delay compensation stage or trade-off in trap attenuation, via lower coupling inductance. The RF modulator typically has a high input impedance (about 1 K ± 30%) and loose tolerance. Consequently, the amplitude variation at the modulator input will be greater, especially when the trap is properly terminated at the modulator input for maximum effect. Some modulators video or aural fidelity will degrade dramatically when overdriven, so the value of the effective termination (nominally 37.5 Ω) may need to be adjusted downward to maintain sufficient linearity (or depth of modulation margin) in the RF signal. When using a two section trap (e.g., when stereo, SAP, or AM aural carriers are generated), some impedance isolation (e.g., buffer) may be required before the trap to obtain flattest frequency response. See Figures 19 and 20. The degree of trap attenuation will affect chroma-luma delay inequality, so optimization of elements around the trap will achieve best performance compromise



PARAMETRIC INFORMATION

DC Electrical Parameters

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. See Table 16 for absolute maximum ratings and Table 17 for recommended operating conditions.

Table 16. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (Measured to GND)				7.0	V
Voltage on Any Signal Pin(1)		GND –0.5		VAA + 0.5	V
CVBS/Y/C Output Short Circuit Duration to Any Power Supply or Common	ISC		Indefinite		
Storage Temperature	TS	–65		+150	°C
Vapor Phase Soldering (1 Minute)	TVSOL			220	°C
Notes: (1). This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply or ground voltage by more than 0.5 V can cause destructive latchup.					

Table 17. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply (zero LFPM)	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		70	°C
DAC Output Load(1)	RL		37.5		Ω
Nominal RSET	RSET		150 Ω		
Notes: (1). DC component not to exceed 80 Ω.					

DC Characteristics

Recommended Operating Conditions, NTSC CCIR 601 operation, and CLK frequency = 27 MHz. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V. See Table 18. RSET = 150 Ω, RLOAD = 37.5 Ω, VRDAC = VREF_OUT.

Table 18. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Video D/A Resolution		9	9	9	Bits
Output Current-DAC Code 511 (Iout FS)			34.08		MA
Output Voltage-DAC Code 511			1.28		V
Video Level Error (I_{OUT})		–5		+5	%
Output Capacitance			22		pF
Digital Inputs (except those specified below)					
Input High Voltage	VIH	2.0		VAA +0.5	V
Input Low Voltage	VIL	GND –0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
CLK Input					
Input High Voltage	VIH	2.4		VAA +0.5	V
Input Low Voltage	VIL	GND –0.5		0.8	V
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
Output Capacitance	CDOUT		10		pF
VRDAC Input Current	IREF_IN		10		µA

AC Characteristics

Recommended Operating Conditions, NTSC CCIR 601 operation, and CLK frequency = 27.000 MHz. HSYNC* and VSYNC* output load ≤ 75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V. See Table 19. Video input and output timing is shown in Figure 21. RSET = 150 Ω, RLOAD = 37.5 Ω, VRDAC = VREFOUT (CVBS/C output).

Table 19. AC Characteristics *(1 of 2)*

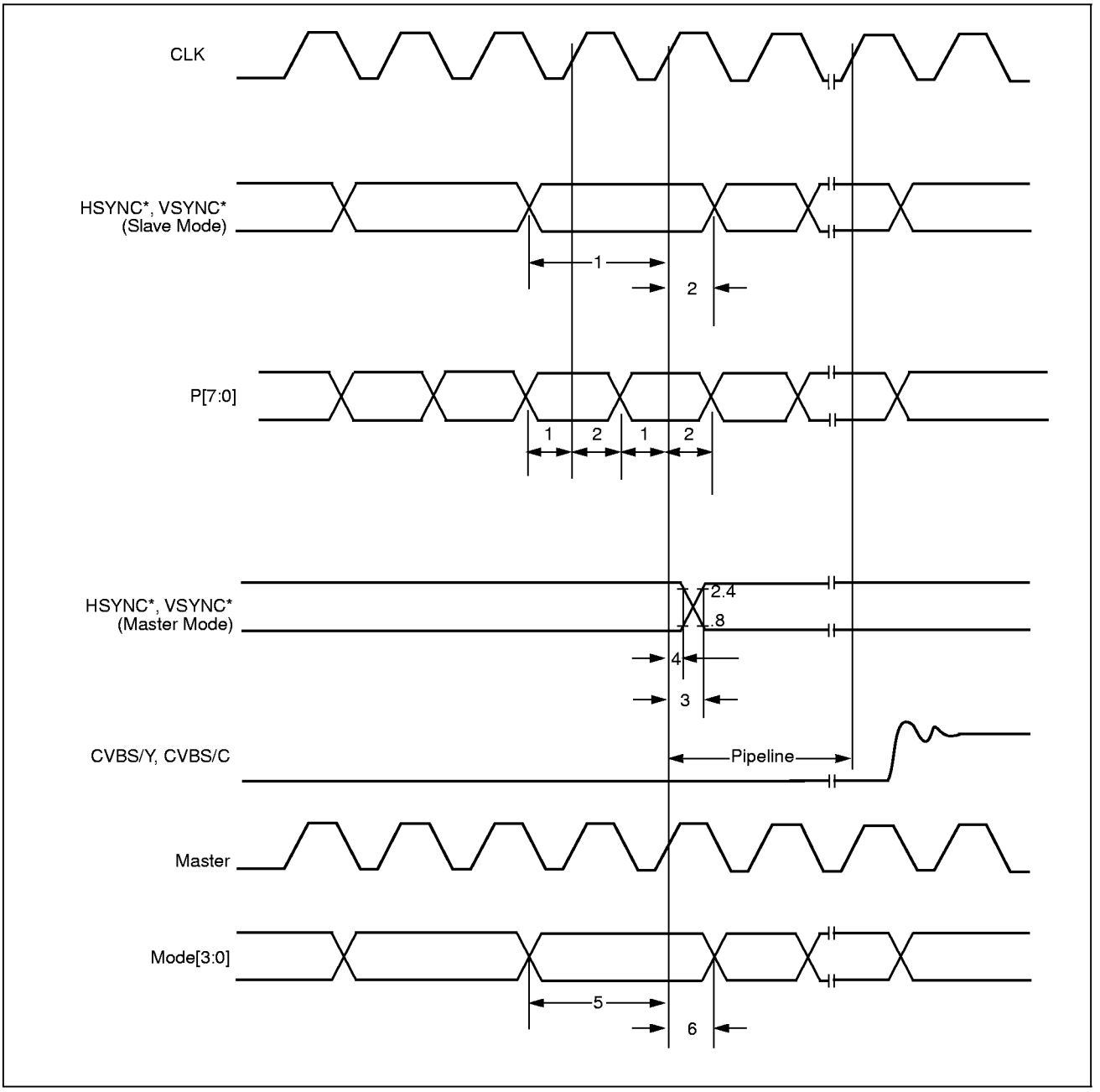
Parameter	EIA/TIA 250C Ref	Symbol	Min	Typ	Max	Units
Hue Accuracy(1, 2)				1.5	2.5	± °
Color Saturation Accuracy(1, 2)				1.5	2.3	± %
Chroma AM/PM Noise(2)	1 MHz Red Field			–62		dB rms
Differential Gain(3)	6.2.2.1			1.0		% p–p
Differential Phase(3)	6.2.2.2			1.0		° p–p
SNR (Unweighted 100 IRE Y Ramp Tilt Correct)(2)						
RMS	6.3.1			60		dB rms
Peak Periodic	6.3.2			56		dB p-p
100 IRE Multiburst(5)	6.1.1			–2		± IRE
Chroma/Luma Gain Ineq(2)	6.1.2.2			–5		± IRE
Chroma/Luma Delay Ineq(2)	6.1.2			0		ns
Short Time Distortion 100IRE/Pixel(3)	6.1.6			2.5		%
Luminance Nonlinearity(3)	6.2.1			2		%
Chroma/Luma Intermod(3)	6.2.3			0.1		± IRE
Chroma Nonlinear Gain(3)	6.2.4.1				1.0	± IRE
Chroma Nonlinear Phase(3)	6.2.4.2				1.0	± °
Pixel/Control Setup Time(4)		1	6			ns
Pixel/Control Hold Time(4)		2	3			ns
Control Output Delay Time(4)		3			17	ns
Control Output Hold Time(4)		4	2			ns
CLK Frequency			24.54	27	29.50	MHz

Table 19. AC Characteristics *(2 of 2)*

Parameter	EIA/TIA 250C Ref	Symbol	Min	Typ	Max	Units
CLK Pulse Width Low Time			8			ns
CLK Pulse Width High Time			8			ns
Mode[3:0] Setup Time		5	10			
Mode[3:0] Hold Time		6	5			
Pipeline Delay						
Input Pixels to Composite Video				49		CLK Periods
HSYNC* to Analog Output (Slave Mode)				48		CLK Periods
HSYNC* to Analog Output (Master Mode)				40		CLK Periods
VAA Supply Current				130	155	mA
Power-Down Mode Current(6)				3	10	mA

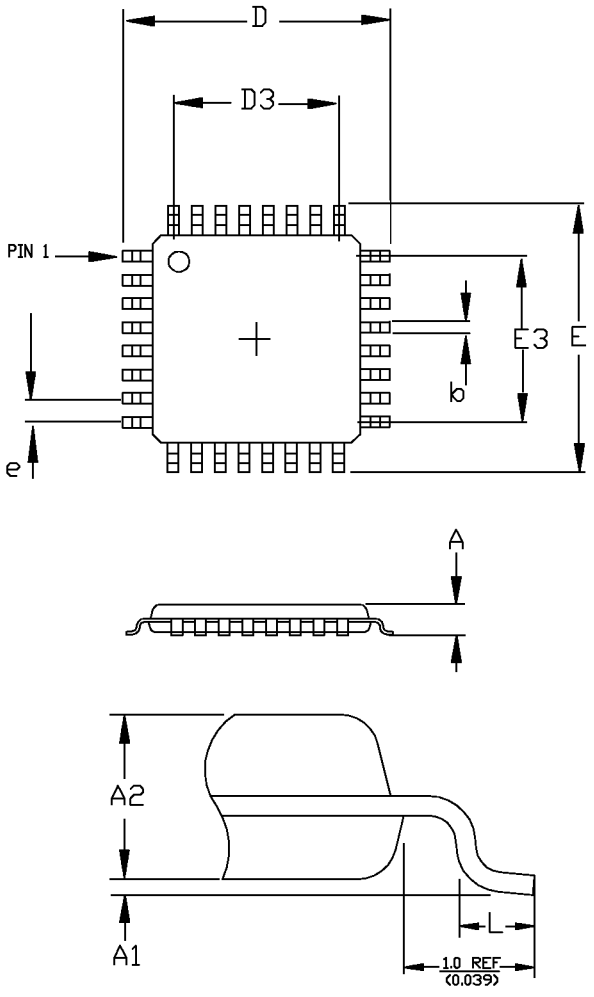
Notes: (1). 75/7.5/75/7.5 color bars normalized to burst.
(2). Guaranteed by characterization without postfilter or beads.
(3). Without post filter. Guaranteed by design.
(4). Control pins are defined as P[7:0], HSYNC*, VSYNC*, and SLEEP.
(5). With optional peaking beads but no filter.
(6). Without loading on the HSYNC* and VSYNC* pins.

Figure 21. 8-Bit YCrCb Video Input and Output Timing



Package Drawing

Figure 22. 32-Pin Thin Quad Flat Pack (TQFP)



SYMBOL	JEDEC VARIATION MO-136 BC		
	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.60
A_1	0.05	0.10	0.15
A_2	1.35	1.40	1.45
D		9.00 BSC.	
D_1		7.00 BSC.	
E		9.00 BSC.	
E_1		7.00 BSC.	
L	0.45	0.60	0.75
N		32	
e		0.80 BSC.	
b	0.30	0.37	0.45

Revision History

Revision	Change from Previous Revision
A	Initial Release
B	Revised Table 3 Pins 8, 30, 31 changed from GND to AGND. Pin 27 changed from VAA to VDD, Figure 3 revised. ELiminated Y[7:0] Figure 7, 8, and 9 revised. Eliminated RESET*. Figure 10 and 11 revised. CLOCK = 13.5 MHz changed to CLK = 27 MHz. Figure 18 updated. Table 13 revised. Added L2 description. VBIAS Coupling, page 29. Changed VAA reference to GND. Table 15. TBD replaced with 150 Ω. Table 17. VAA Supply Current changed from 200 to 120.
C	Signal VREF_IN removed, VRDAC added. 3 V supply voltage operation removed. Odd field changed to Field 1, Even field changed to Field 2. Pin description list modified to provide further signal clarification. Signals MODE[3:0] and VRDAC added to Detailed Block Diagram, VREF_IN removed. Slave Register M60Hz removed. Video output truth tables revised to provide further signal values information. Added Configuration Register Settings (Table 3), Bt852 (Master Mode) Output Video Format Setting (Table 4a), and Bt852 (Slave Mode) Output Video Format Setting (Table 4a). Added DAC sinx/x Response Figures 12a and 12b.