

128K x 8 HIGH-SPEED CMOS STATIC RAM 3.3V REVOLUTIONARY PINOUT

SEPTEMBER 2000

FEATURES

- High-speed access times:
8, 10, 12 and 15 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with \overline{CE} and \overline{OE} options
- \overline{CE} power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply
- Packages available:
 - 32-pin 300-mil SOJ
 - 32-pin 400-mil SOJ
 - 32-pin TSOP (Type II)

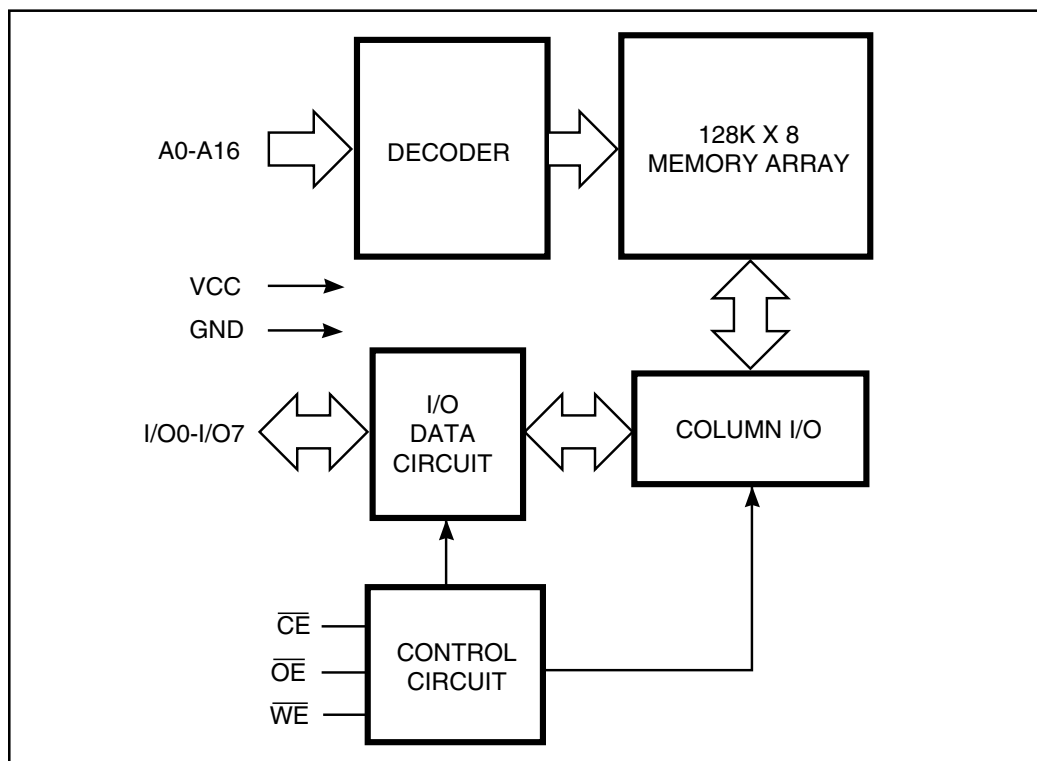
DESCRIPTION

The *ISSI* IS63LV1024 is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM in revolutionary pinout. The IS63LV1024 is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 μ W (typical) with CMOS input levels.

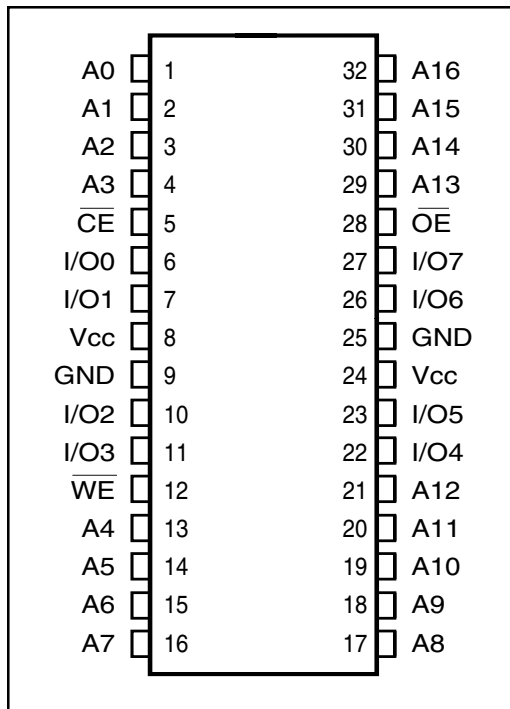
The IS63LV1024 operates from a single 3.3V power supply and all inputs are TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM

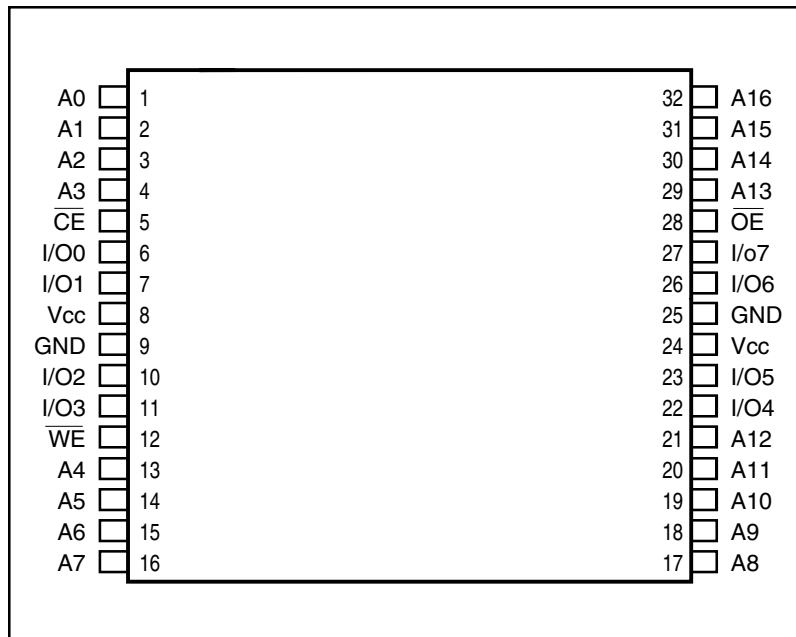


ISSI reserves the right to make changes to its products at any time without notice in order to improve design and supply the best possible product. We assume no responsibility for any errors which may appear in this publication. © Copyright 2000, Integrated Silicon Solution, Inc.

PIN CONFIGURATION 32-Pin SOJ



PIN CONFIGURATION 32-Pin TSOP (Type II) (T)



PIN DESCRIPTIONS

A0-A16	Address Inputs
\overline{CE}	Chip Enable Input
\overline{OE}	Output Enable Input
\overline{WE}	Write Enable Input
I/O0-I/O7	Bidirectional Ports
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	\overline{WE}	\overline{CE}	\overline{OE}	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	ISB1, ISB2
Output Disabled	H	L	H	High-Z	Icc1, Icc2
Read	H	L	L	DOUT	Icc1, Icc2
Write	L	L	X	DIN	Icc1, Icc2

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

IS63LV1024

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	3.3V ± 0.15V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4	—	V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	—	0.4	V	
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	V	
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V	
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	Com. Ind.	-1 5	1 5	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC} , Outputs Disabled	Com. Ind.	-1 -5	1 5	μA

Notes:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	-8 ns		-10 ns		-12 ns		-15 ns		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
I _{CC1}	V _{CC} Operating Supply Current	V _{CC} = Max., $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = Max.	Com.	—	160	—	150	—	130	—	120	mA
			Ind.	—	170	—	160	—	140	—	130	
I _{SB}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = Max	Com.	—	55	—	45	—	40	—	35	mA
			Ind.	—	55	—	45	—	40	—	35	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	25	—	25	—	25	—	25	mA
			Ind.	—	30	—	30	—	30	—	30	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., $\overline{CE} \leq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com.	—	5	—	5	—	5	—	5	mA
			Ind.	—	10	—	10	—	10	—	10	

Notes:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{I/O}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-8 ns		-10 ns		-12 ns		-15 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	8	—	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	—	15	ns
t_{OHA}	Output Hold Time	2	—	2	—	3	—	3	—	ns
t_{ACE}	\overline{CE} Access Time	—	8	—	10	—	12	—	15	ns
t_{DOE}	\overline{OE} Access Time	—	4	—	5	—	6	—	7	ns
$t_{LZOE}^{(2)}$	\overline{OE} to Low-Z Output	0	—	0	—	0	—	0	—	ns
$t_{HZOE}^{(2)}$	\overline{OE} to High-Z Output	0	4	0	5	0	6	0	7	ns
$t_{LZCE}^{(2)}$	\overline{CE} to Low-Z Output	3	—	3	—	3	—	3	—	ns
$t_{HZCE}^{(2)}$	\overline{CE} to High-Z Output	0	4	0	5	0	6	0	7	ns
t_{PU}	\overline{CE} to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}	\overline{CE} to Power Down Time	—	8	—	10	—	12	—	15	ns

Notes:

- Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and C1 output loading specified in Figure 1.
- Tested with the C2 load in Figure 1. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1a and 1b

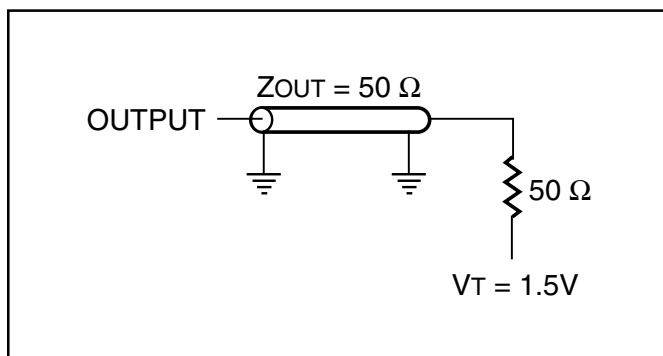
AC TEST LOADS

Figure 1

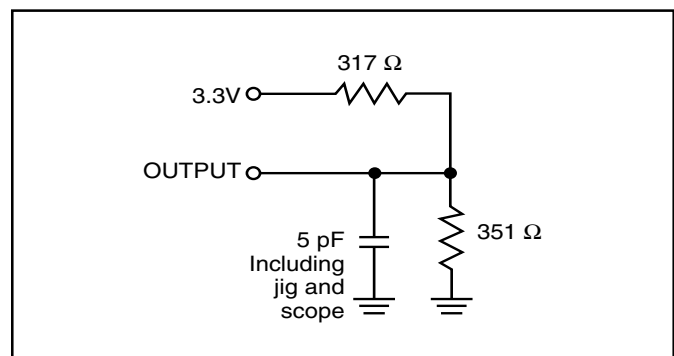
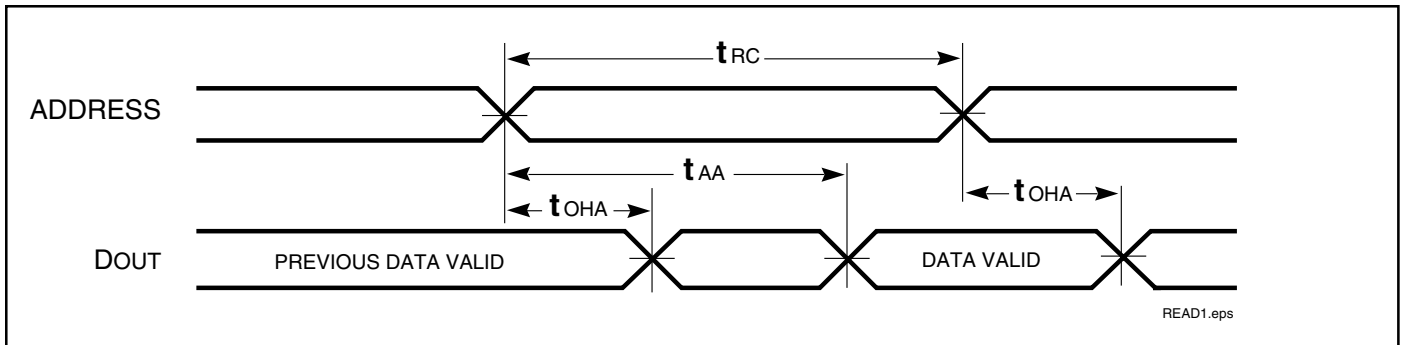


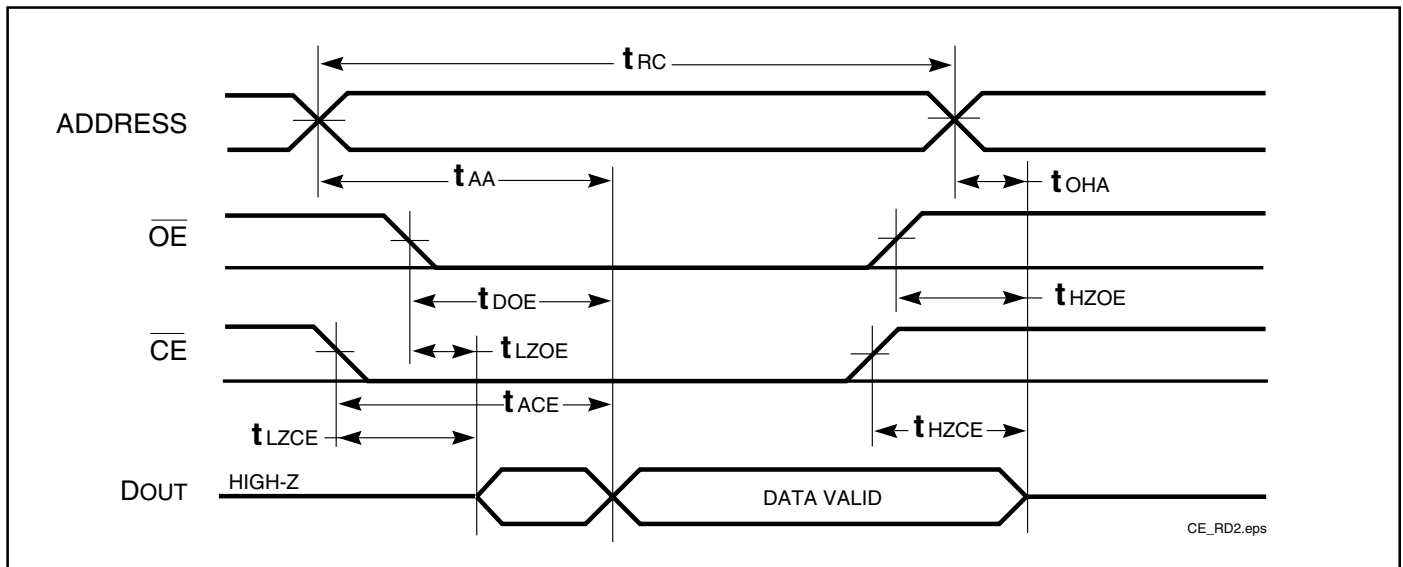
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)



READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transitions.

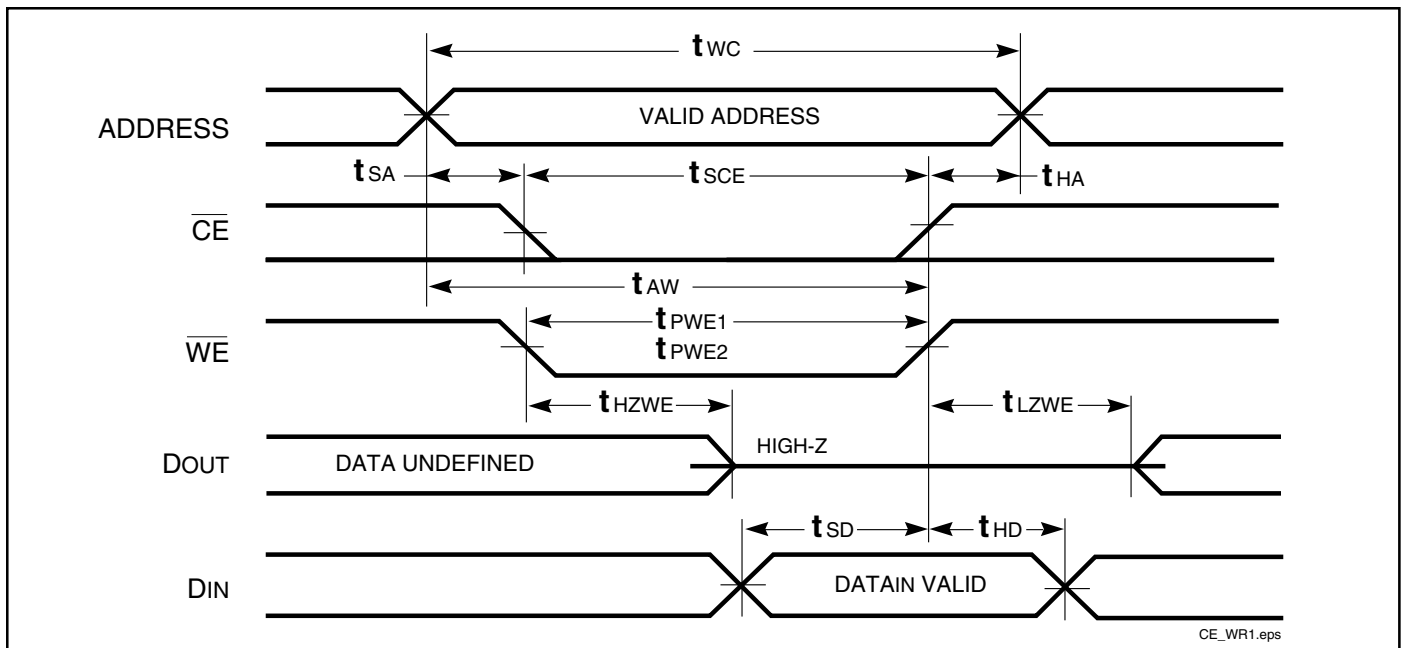
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-8 ns		-10 ns		-12 ns		-15 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	8	—	10	—	12	—	15	—	ns
t _{SCE}	\overline{CE} to Write End	7	—	7	—	8	—	10	—	ns
t _{AW}	Address Setup Time to Write End	8	—	8	—	8	—	10	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t _{PWE₁} ⁽¹⁾	\overline{WE} Pulse Width (\overline{OE} High)	7	—	7	—	8	—	10	—	ns
t _{PWE₂} ⁽²⁾	\overline{WE} Pulse Width (\overline{OE} Low)	8	—	10	—	12	—	15	—	ns
t _{SD}	Data Setup to Write End	5	—	5	—	6	—	7	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{HZWE} ⁽²⁾	\overline{WE} LOW to High-Z Output	—	4	—	5	—	6	—	7	ns
t _{LZWE} ⁽²⁾	\overline{WE} HIGH to Low-Z Output	3	—	3	—	3	—	3	—	ns

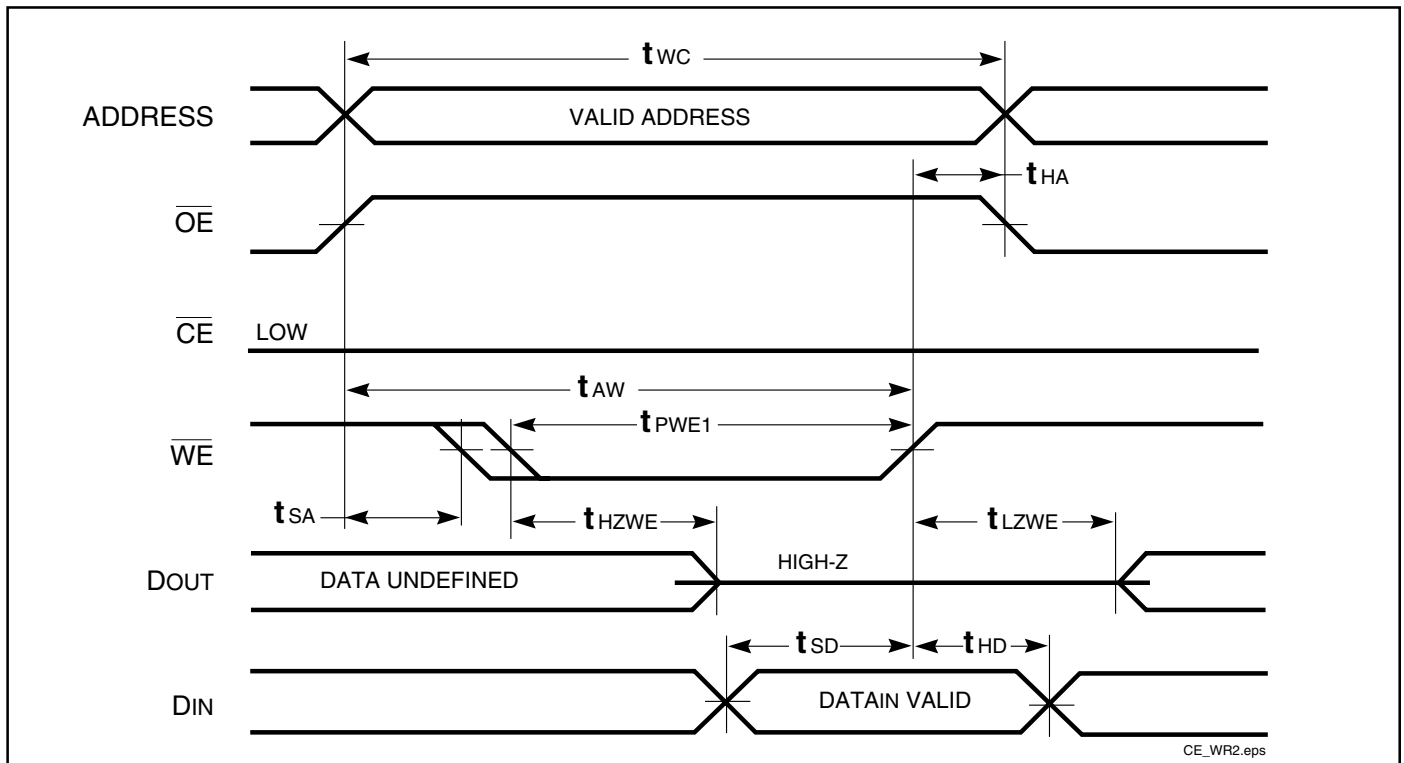
Notes:

1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

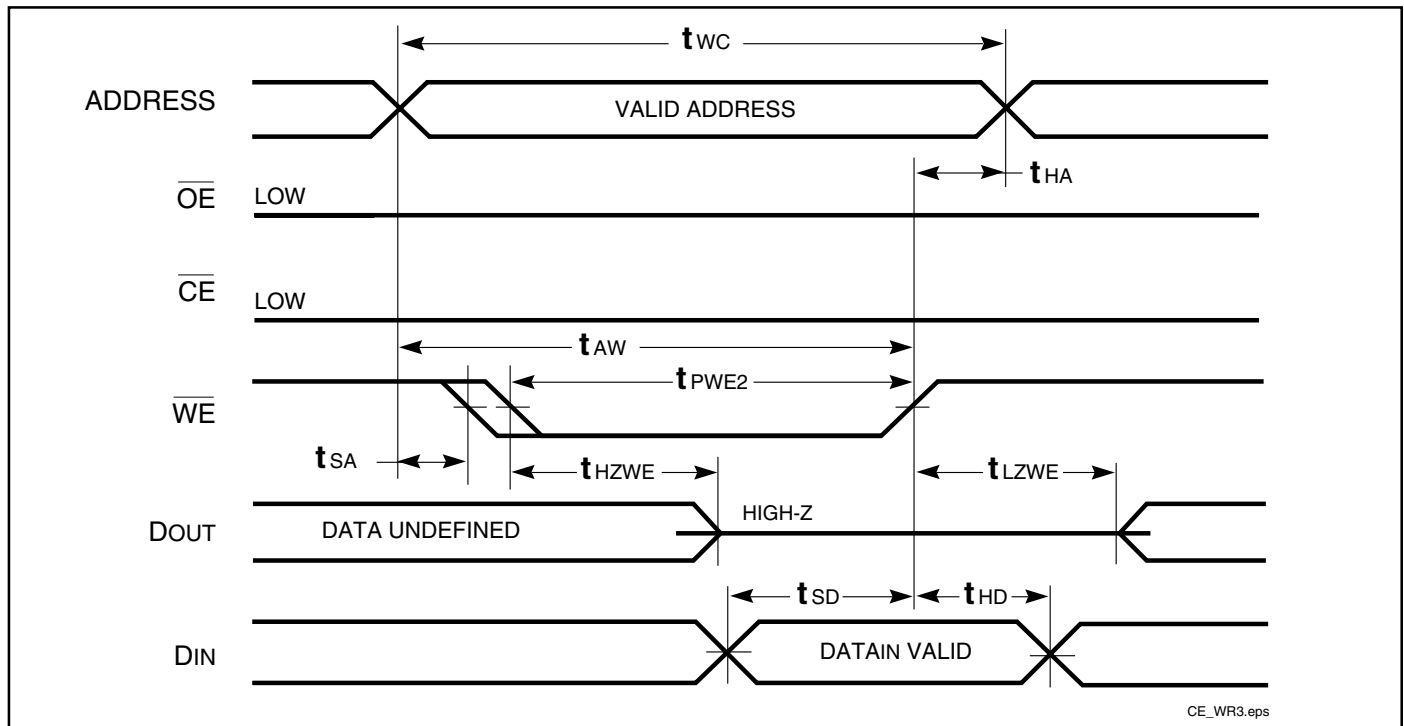
AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) (\overline{CE} Controlled, \overline{OE} = HIGH or LOW)

WRITE CYCLE NO. 2⁽¹⁾ (\overline{WE} Controlled, \overline{OE} = HIGH during Write Cycle)



WRITE CYCLE NO. 3 (\overline{WE} Controlled: \overline{OE} is LOW During Write Cycle)



Notes:

1. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \cdot V_{IH}$.

ORDERING INFORMATION**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
8	IS63LV1024-8T	TSOP (Type II)
	IS63LV1024-8J	300-mil Plastic SOJ
	IS63LV1024-8K	400-mil Plastic SOJ
10	IS63LV1024-10T	TSOP (Type II)
	IS63LV1024-10J	300-mil Plastic SOJ
	IS63LV1024-10K	400-mil Plastic SOJ
12	IS63LV1024-12T	TSOP (Type II)
	IS63LV1024-12J	300-mil Plastic SOJ
	IS63LV1024-12K	400-mil Plastic SOJ
15	IS63LV1024-15T	TSOP (Type II)
	IS63LV1024-15J	300-mil Plastic SOJ
	IS63LV1024-15K	400-mil Plastic SOJ

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
8	IS63LV1024-8TI	TSOP (Type II)
	IS63LV1024-8JI	300-mil Plastic SOJ
	IS63LV1024-8KI	400-mil Plastic SOJ
10	IS63LV1024-10TI	TSOP (Type II)
	IS63LV1024-10JI	300-mil Plastic SOJ
	IS63LV1024-10KI	400-mil Plastic SOJ
12	IS63LV1024-12TI	TSOP (Type II)
	IS63LV1024-12JI	300-mil Plastic SOJ
	IS63LV1024-12KI	400-mil Plastic SOJ
15	IS63LV1024-15TI	TSOP (Type II)
	IS63LV1024-15JI	300-mil Plastic SOJ
	IS63LV1024-15KI	400-mil Plastic SOJ

ISSI®

Integrated Silicon Solution, Inc.

2231 Lawson Lane
 Santa Clara, CA 95054
 Tel: 1-800-379-4774
 Fax: (408) 588-0806
 E-mail: sales@issi.com
www.issi.com