128Mbit GDDR2 SDRAM

1M x 32Bit x 4 Banks
GDDR2 SDRAM
with Differential Data Strobe and DLL

Revision 1.7

January 2003

Revision History

Revision 1.7 (January 23, 2003)
- Changed the device name from GDDR-II to GDDR2

Revision 1.6 (December 18, 2002)
- Typo corrected

Revision 1.5 (December 4, 2002)
- Typo corrected

Revision 1.4 (November 12, 2002)
- Changed the device name from DDR-II to GDDR-II
- Typo corrected

Revision 1.3 (November 8, 2002)
- Typo corrected

Revision 1.2 (November 5, 2002)
- Typo corrected
- Changed the Icc6 from 3mA to 7mA

Revision 1.1 (October 30, 2002)
- Typo corrected

Revision 1.0 (September 30, 2002)
- Changed tCK(max) from 4.5ns to 4.0ns

Revision 0.7 (September 12, 2002)
- Added IBIS curve in the spec
- Defined DC spec
- Typo corrected
- Defined Burst Write with AP (AL=0) Table.
- Defined On-die Termination Status of 2Banks System Table.
- Changed C_{IN1},C_{IN2},C_{IN3},C_{out} and C_{IN4} from 3.5pF to 3.0pF
- Removed CL(Cas Latency) 8 from the spec
- Changed VDD form 2.5V $\pm$ 5% to 2.5V $\pm$ 0.1V
- Changed speed bin from 500/400/333MHz to 500/450/400MHz
- Changed EMRS table

Revision 0.6 (February 28, 2002)
- Changed WL(write latency) from RL(read latency) -1 to AL(additive latency) +1
- Changed tIH/tSS during EMRS from 5ns to 0.5tCK
- Changed tRCDWR
- Changed package ball location of CK, /CK, CKE

Revision 0.5 (January 2002)
- Eliminated DLLEN pin
- Power-up sequence

Revision 0.4 (January 2002)
- Changed EMRS Table
- Changed Self-Refresh exit mode
- Changed On-die Termination Control
- Changed OCD Control method
- Power-up sequence

Revision 0.3 (December 2001)
- Noted the ball names changed from DDR-1 and exchanged DQS and /DQS ball location.
- Added On-die termination control
- Changed OCD align mode entry / exit timing
- Added target value of Data & DQS input/output capacitance(DQ_0~DQ_{31})
- Added Table for auto precharge control
- Typo corrected.

Revision 0.2 (November 2001)
- Data Strobe Scheme is changed from DQS separation of Read DQS, Write DQS to Differential and Bi-directional DQS
- OCD adjustment
- Controlled DQ is changed from DQ0, WDQS2 to DQ23, DQS2 and /DQS2

Revision 0.1 (October 2001)
- Data Strobe Scheme is changed from Bi-directional DQS to DQS separation to Read DQS, Write DQS
- Package Ball layout is changed for mirror package.
- OCD adjustment
  Controlled DQ is changed from DQ0, DQS0 to DQ23, WDQS2
- Added DM descriptions
- 1bank, 2bank system
- Added System Selection mode in EMRS table.

Revision 0.0 (August 2001)

1M x 32Bit x 4 Banks GDDR2 Synchronous DRAM with Differential Data Strobe

FEATURES

- 2.5V ± 0.1V power supply for device operation
- 1.8V ± 0.1V power supply for I/O interface
- On-Die Termination for all inputs except CKE,ZQ
- Output Driver Strength adjustment by EMRS
- SSTL_18 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
  - CAS latency : 5, 6, 7 (clock)
  - Burst length : 4 only
  - Burst type : sequential only
- Additive latency (AL): 0,1(clock)
- Read latency(RL) : CL+AL
- Write latency(WL) : AL+1
- Differential Data Strobes for Data-in, Date out ;
  - 4 DQS and /DQS(one differential strobe per byte)
  - Single Data Strobes by EMRS.
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 32ms refresh period (4K cycle)
  (16ms is under consideration)
- 144 Ball FBGA
- Maximum clock frequency up to 500MHz
- Maximum data rate up to 1Gbps/pin
- DLL for Address, CMD and outputs

ORDERING INFORMATION

Part NO.	Max Freq.	Max Data Rate	Interface	Package
K4N26323AE-GC20	500MHz	1000Mbps/pin	SSTL_18	144 Ball FBGA
K4N26323AE-GC22	450MHz	900Mbps/pin		
K4N26323AE-GC25	400MHz	800Mbps/pin		

GENERAL DESCRIPTION

FOR 1M x 32Bit x 4 Bank GDDR2 SDRAM

The 4Mx32 GDDR2 is 134,217,728 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 1,048,976 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 4GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

PIN CONFIGURATION

Normal Package (Top View)

	2	3	4	5	6	7	8	9	10	11	12	13
B	DQS0	/DQS0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	/DQS3	DQS3
C	DQ4	DM0	VDDQ	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	VDDQ	DM3	DQ27
D	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
E	DQ7	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ24
F	DQ17	DQ16	VDDQ	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	VDDQ	DQ15	DQ14
G	DQ19	DQ18	VDDQ	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	VDDQ	DQ13	DQ12
H	DQS2	/DQS2	NC	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	NC	/DQS1	DQS1
J	DQ20	DM2	VDDQ	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	VDDQ	DM1	DQ11
K	DQ21	DQ22	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ10
L	DQ23	A3	VDD	VSS	RFU_2	VDD	VDD	RFU_1	VSS	VDD	A4	DQ8
M	VREF	A2	A10	/RAS	NC	CKE	NC	ZQ	/CS	A9	A5	VREF
N	A0	A1	A11	BA0	/CAS	CK	/CK	/WE	BA1	A8/AP	A6	A7

NOTE :

1. RFU1 is reserved for A12
2. RFU2 is reserved for BA2
3. (M,13) VREF for CMD and ADDRESS
4. (M,2) VREF for Data input

PIN CONFIGURATION

Mirror Package (Top View)

	2	3	4	5	6	7	8	9	10	11	12	13
B	DQS3	/DQS3	VSSQ	DQ28	DQ29	DQ31	DQ0	DQ2	DQ3	VSSQ	/DQS0	DQS0
C	DQ27	DM3	VDDQ	VDDQ	DQ30	VDDQ	VDDQ	DQ1	VDDQ	VDDQ	DM0	DQ4
D	DQ25	DQ26	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ5	DQ6
E	DQ24	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ7
F	DQ14	DQ15	VDDQ	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	VDDQ	DQ16	DQ17
G	DQ12	DQ13	VDDQ	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	VDDQ	DQ18	DQ19
H	DQS1	/DQS1	NC	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	NC	/DQS2	DQS2
J	DQ11	DM1	VDDQ	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	VDDQ	DM2	DQ20
K	DQ10	DQ9	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ22	DQ21
L	DQ8	A4	VDD	VSS	RFU_1	VDD	VDD	RFU_2	VSS	VDD	A3	DQ23
M	VREF	A5	A9	/CS	ZQ	NC	CKE	NC	/RAS	A10	A2	VREF
N	A7	A6	A8/AP	BA1	/WE	/CK	CK	/CAS	BA0	A11	A1	A0

*** Under consideration**

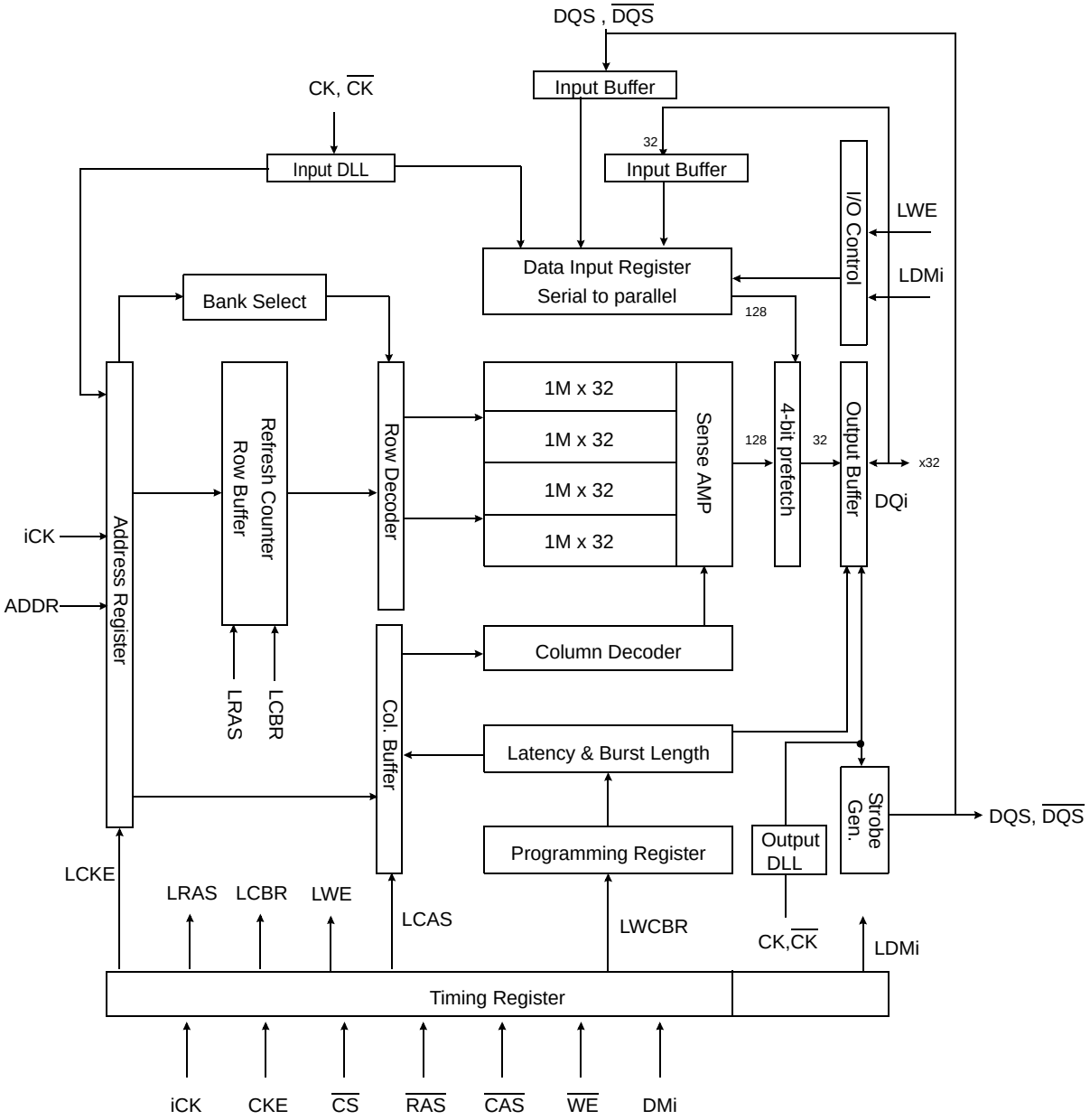
INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and CK are differential clock inputs. CMD, ADD inputs are sampled on the crossing of the positive edge of CK and negative edge of CK. Output (read) data is referenced to the crossings of CK and CK (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM0 ~DM3	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of clock. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A11	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A8 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A8 LOW) or all banks (A8 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/ Output	**Data Input/ Output:** Bi-directional data bus.
DQS0~ DQS3 $\overline{DQS0}$~ $\overline{DQS3}$	Input/ Output	**Data Strobe:** output with read data, input with write data for source synchronous operation.Edge-aligned with read data, centered in write data.

DQS Scheme	Differential DQS per byte
DQS0, $\overline{DQS0}$	DQS0 for DQ0-DQ7
DQS1, $\overline{DQS1}$	DQS1 for DQ8-DQ15
DQS2, $\overline{DQS2}$	DQS2 for DQ16-DQ23
DQS3, $\overline{DQS3}$	DQS3 for DQ24-DQ31

NC/ RFU		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V ± 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 2.5V ± 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage:** half Vddq , **2 Pins :** (M,2) for Data input , (M,13) for CMD and ADDRESS
ZQ	input	Resistor connection pin for On-die termination. The value of Resistor = 2 X (target value (Rterm) of termination resistance of DQ pin of each chip)

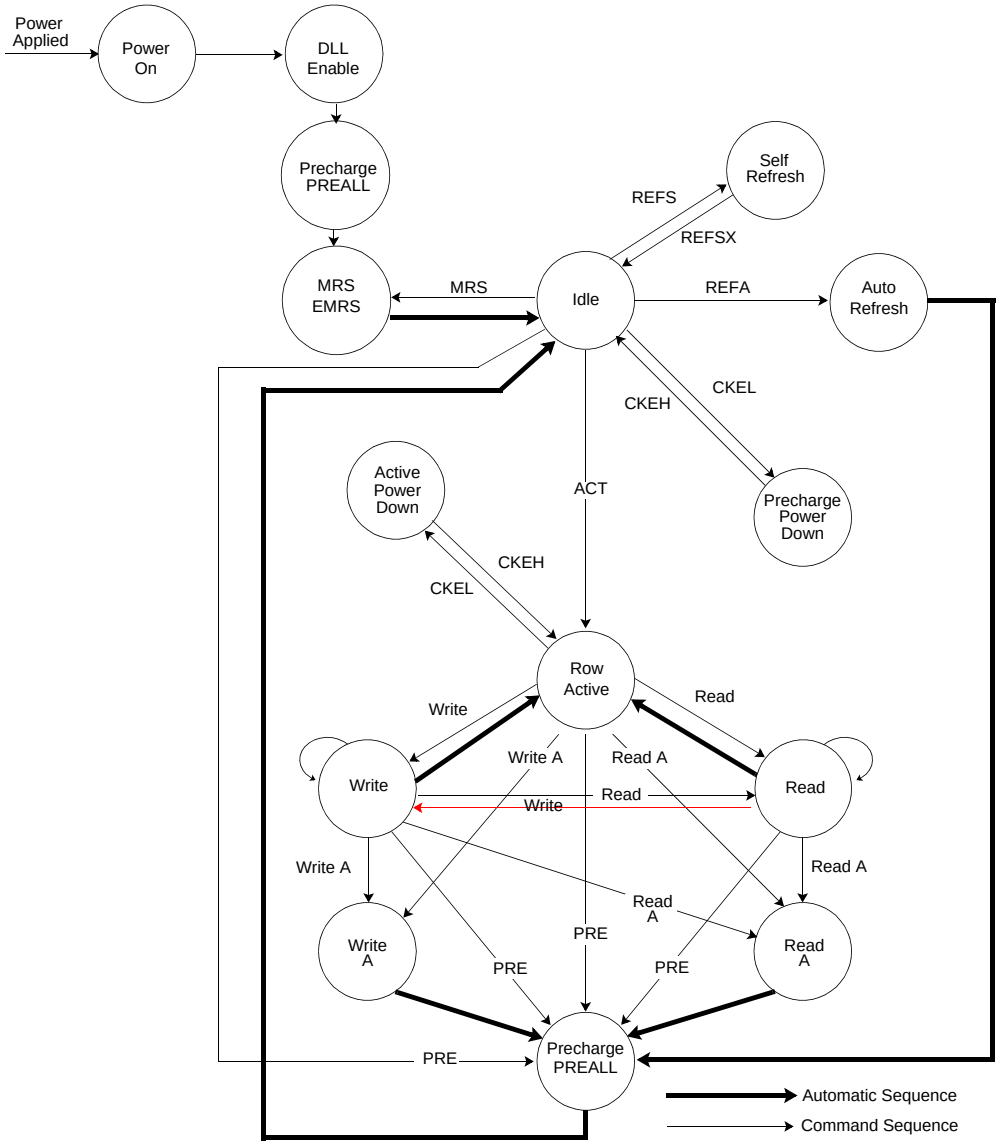
BLOCK DIAGRAM (1Mbit x 32I/O x 4 Bank)



* iCK : internal clock

FUNTIONAL DESCRIPTION

Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

Power-Up Sequence

GDDR2 SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Power Up Sequence
   - Apply Power and Keep CKE at low state. (All other inputs may be undefined)
     - Apply VDD before VDDQ.
     - Apply VDDQ before VREF.
   - Start low frequency clock(100MHz) and maintain stable condition for minimum 200us.
   - The minimum of 200us after stable power and clock (CK, /CK), apply NOP and take CKE to be high.
   - Issue precharge command for all banks of the device (tS/tH =0.5tCK).
   - Issue EMRS command to initialize DRAM with DLL OFF and On-die Termination OFF(tS/tH=0.5tCK) .

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	1	0	X	X			0	X		0	0	X		Extended Mode Register

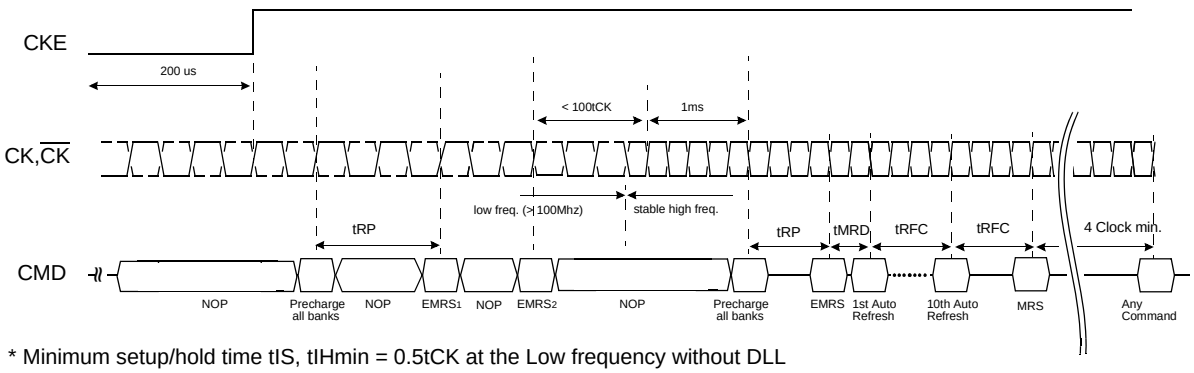
   - Issue EMRS command to control DLL and decide on-die termination state.
     Within 100 clocks after issuing EMRS command for DLL on, stable high frequency clock should be supplied to DRAM.

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	1	0	V	V			1	V		V	V	V		Extended Mode Register

(V=Valid value)

   - The additional 1ms clock cycles are required to lock the DLL and determine value of on-die termination after issuing EMRS command or supplying stable clock from a controller.
     Apply NOP during Locking DLL to protect invalid command.
   - Issue precharge command for all banks of the device.
   - Issue EMRS command
   - Issue at least 10 or more Auto refresh command to update the value of on-die termination.
   - Issue a MRS command to initialize the mode register.
   - Issue any command.

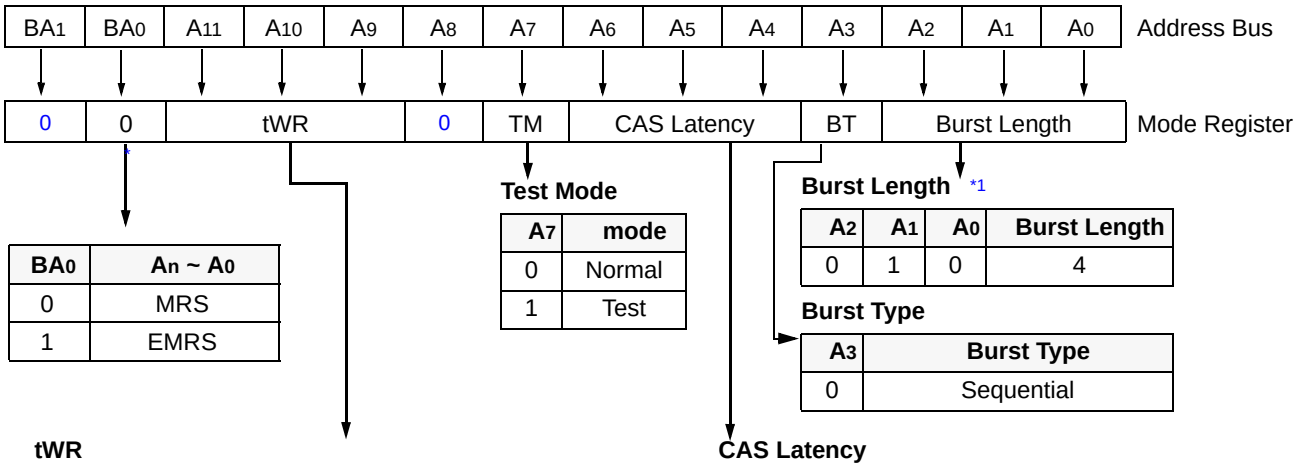
Power up & Initialization Sequence



* Minimum setup/hold time tIS, tIHmin = 0.5tCK at the Low frequency without DLL
* Within 100 tCK after issuing EMRS2, PLL(DLL) of controller should be enabled.
* During changing clock frequency, the changing rate should be smaller than 100ps/30tCK

MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of GDDR2 SDRAM. It programs CAS latency, addressing mode, test mode and various vendor specific options to make GDDR2 SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The GDDR2 SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A_0 ~ A_{11} and BA_0, BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the mode register. Minimum four clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A_0 ~ A_2, addressing mode uses A_3, CAS latency (read latency from column address) uses A_4 ~ A_6. A_7 is used for test mode. A_9 ~ A_{11} are used for tWR. Refer to the table for specific codes for various addressing modes and CAS latencies.



BA_0	A_n ~ A_0
0	MRS
1	EMRS

Test Mode

A_7	mode
0	Normal
1	Test

Burst Length *1

A_2	A_1	A_0	Burst Length
0	1	0	4

Burst Type

A_3	Burst Type
0	Sequential

tWR

A_{11}	A_{10}	A_9	MRS Select
0	0	0	Reserved
0	0	1	Reserved
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

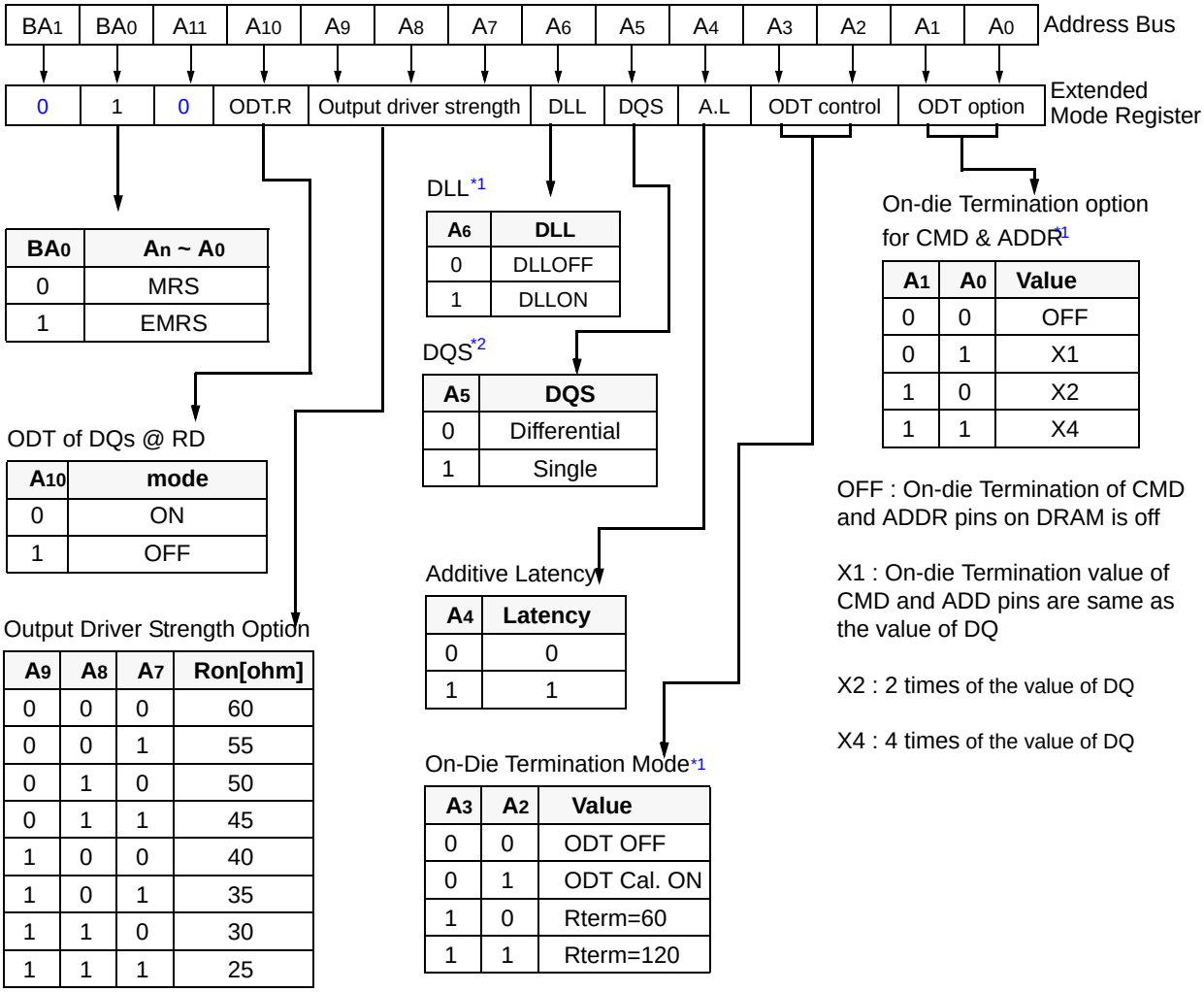
CAS Latency

A_6	A_5	A_4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	5
1	1	0	6
1	1	1	7

*1. BL 4, Sequential Only

EXTENDED MODE REGISTER SET(EMRS)

The extended mode register stores the data output driver strength and on-die termination options. The extended mode register is written by asserting low on CS, RAS, CAS, WE and high on BA0(The GDDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A11 and BA0 in the same cycle as CS, RAS, CAS and WE going low are written in the extended mode register. Four clock cycles are required to complete the write operation in the extended mode register. 8 kinds of the output driver strength are supported by EMRS (A9, A8, A7) code. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. "High" on BA0 is used for EMRS. Refer to the table for specific codes.



BA_0	A_n ~ A_0
0	MRS
1	EMRS

A_6	DLL
0	DLLOFF
1	DLLON

A_5	DQS
0	Differential
1	Single

A_{10}	mode
0	ON
1	OFF

A_4	Latency
0	0
1	1

A_9	A_8	A_7	Ron[ohm]
0	0	0	60
0	0	1	55
0	1	0	50
0	1	1	45
1	0	0	40
1	0	1	35
1	1	0	30
1	1	1	25

A_3	A_2	Value
0	0	ODT OFF
0	1	ODT Cal. ON
1	0	Rterm=60
1	1	Rterm=120

A_1	A_0	Value
0	0	OFF
0	1	X1
1	0	X2
1	1	X4

OFF : On-die Termination of CMD and ADDR pins on DRAM is off

X1 : On-die Termination value of CMD and ADD pins are same as the value of DQ

X2 : 2 times of the value of DQ

X4 : 4 times of the value of DQ

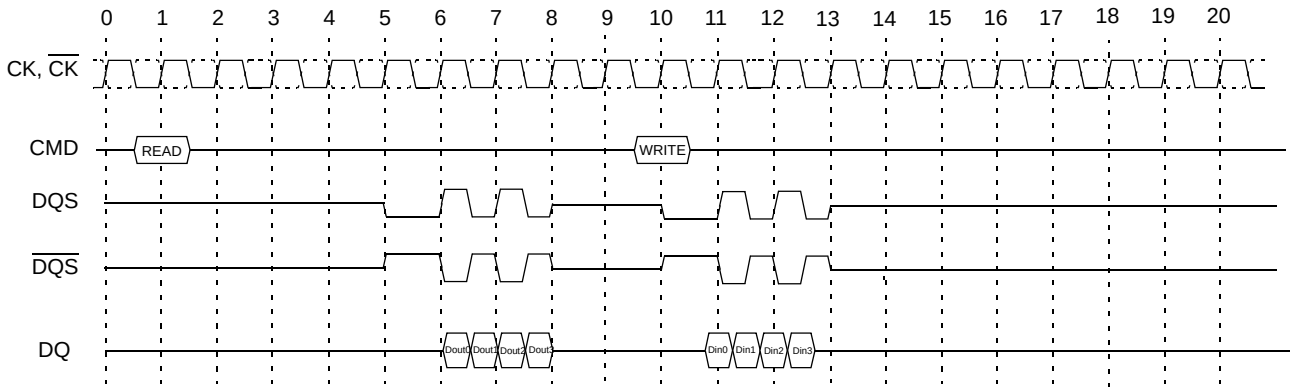
*1. DLL control,ODT control,and ODT option command should be issued at low frequency clock(<100Mhz) with tIS/tIH=0.5tCK
*2. When single DQS is selected, 4 /DQS pins should be connected to VREF.

DQS

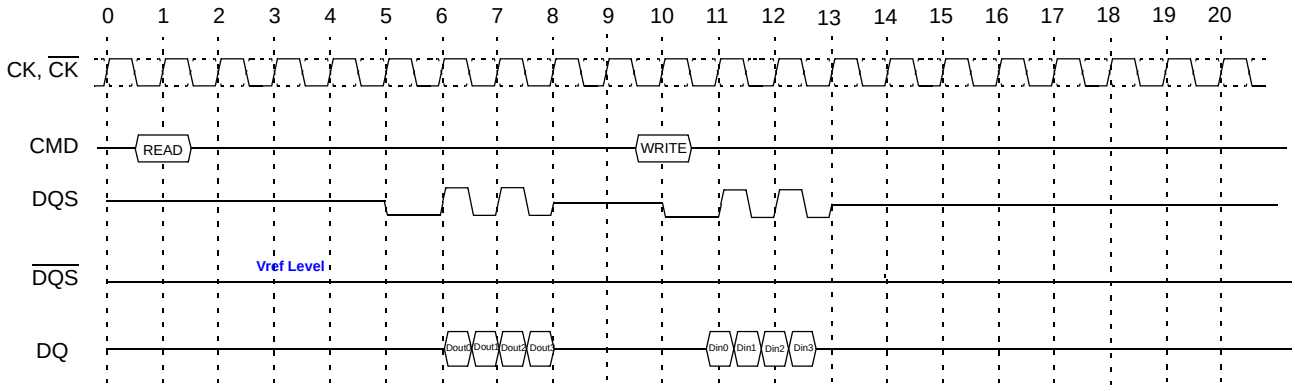
500MHz	450MHZ	400MHz
Differential DQS	Differential DQS	Differential DQS Single DQS

* To support existing DDR-I user , single DQS is supported under 400MHz by EMRS option, When single DQS is selected, 4 /DQS pins should be connected to VREF.

Differntial DQS Timing (CL5, BL4)



Single DQS Timing (CL5, BL4)

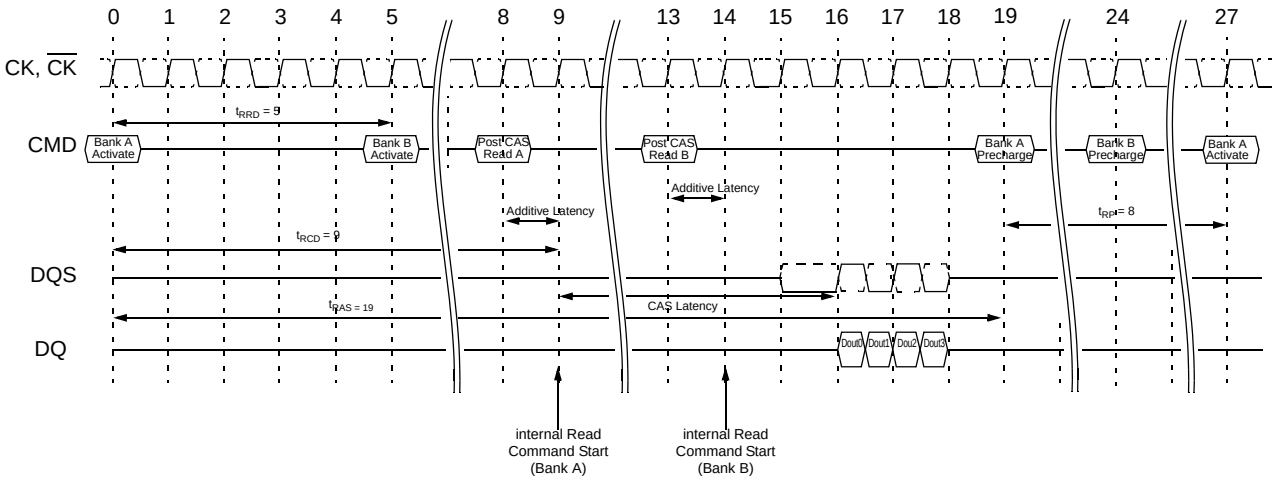


Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 and BA1 are used to select the desired bank. The row address A0 through A11 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the GDDR2 SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied.

Additive latencies of (0,1) are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}), which is equal to tRAS + tRP. The minimum time interval between Bank Activate commands, Bank 0,1, 2, 3 (in any order), is the Bank to Bank delay time (t_{RRD}).

Bank Activate Command Cycle : CL=7, t_{RCD}=9, AL=1, t_{RP}=8, t_{RRD}=5, t_{CCD}=2, t_{RAS}=19



Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. The $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low).

A new burst access must not interrupt the previous 4 bit burst operation. The minimum CAS to CAS delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

Write Latency

The Write Latency(WL) is always defined as AL(Additive Latency)+1 where Read Latency is defined as the sum of additive latency plus CAS latency (RL=AL+CL).

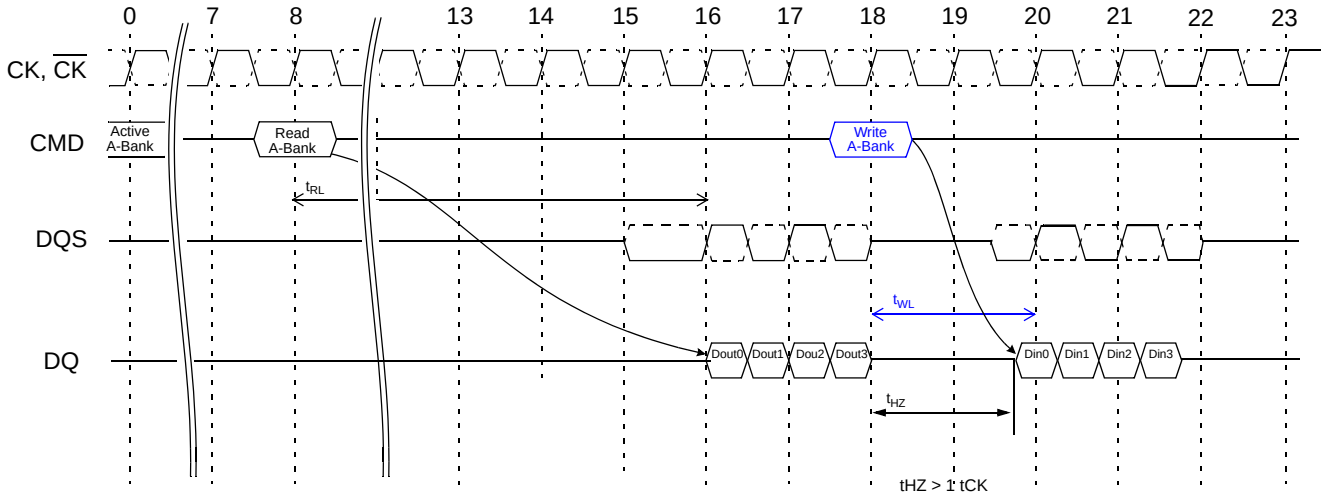
Posted CAS

Posted CAS operation is supported to make command and data bus efficient for sustainable bandwidths in GDDR2 SDRAM. In this operation, the GDDR2 SDRAM allows a CAS read or write command to be issued tRCDmin or 1 tCK earlier than tRCDmin after the RAS bank activate command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the CAS latency (CL). Therefore if a user chooses to issue a R/W command before the tRCDmin, then AL (greater than 0) must be written into the EMRS.

Examples of posted CAS operation

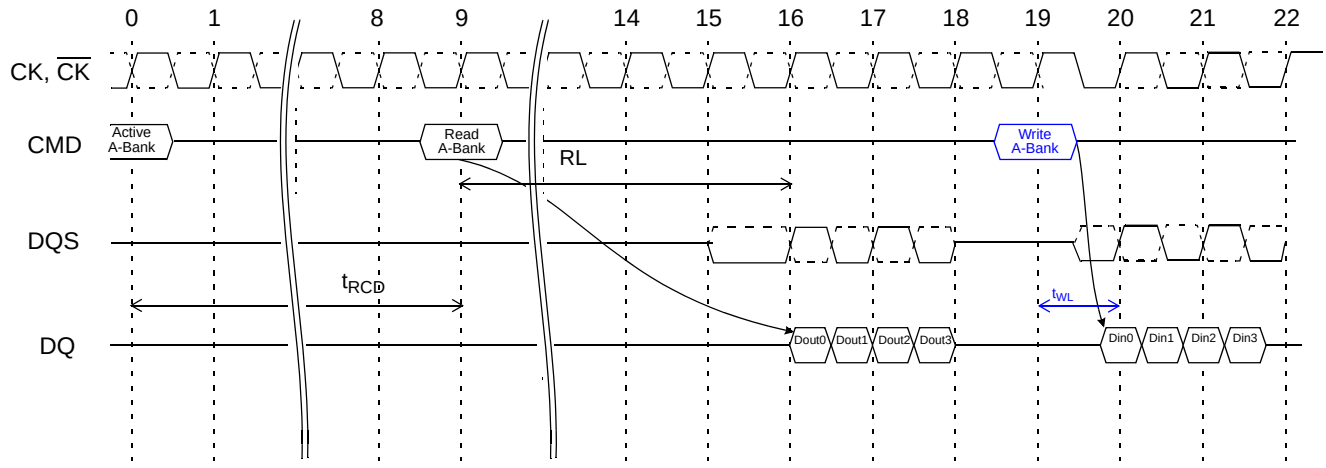
Example 1 Read followed by a write to the same bank

[AL = 1, t_{RCD} = 9, CL = 7, RL = (AL + CL) = 8, WL = (AL + 1) = 2]



Example 2 Read followed by a write to the same bank

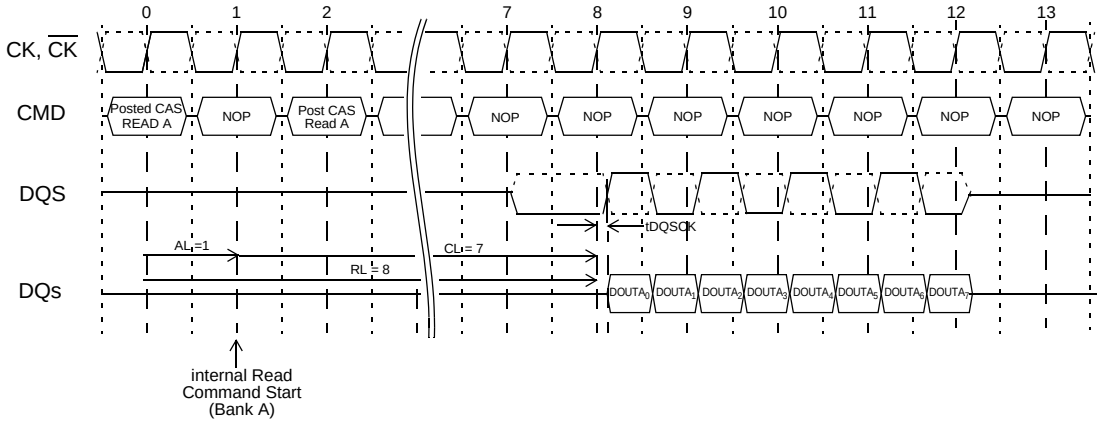
[AL = 0, t_{RCD} = 9, CL = 7, RL = (AL + CL) = 7, WL = (AL + 1) = 1]



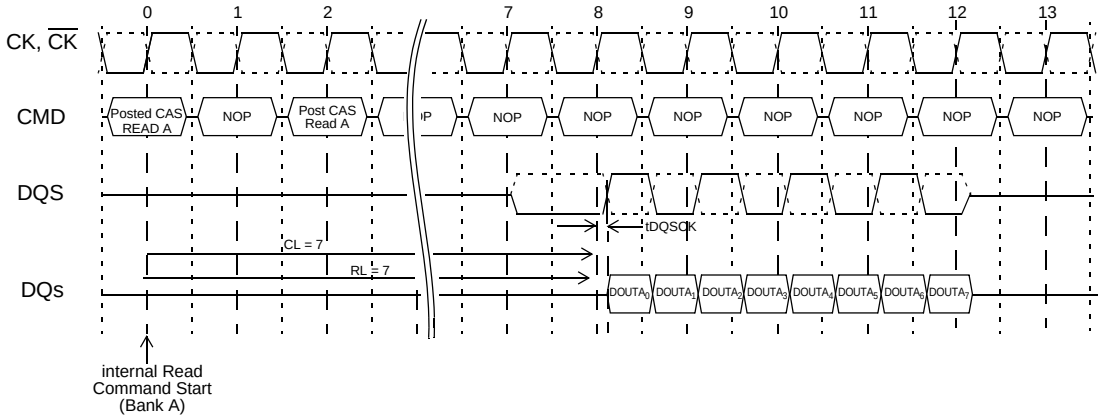
Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR-I SDRAMs. The AL is defined by the Extended Mode Register Set (EMRS).

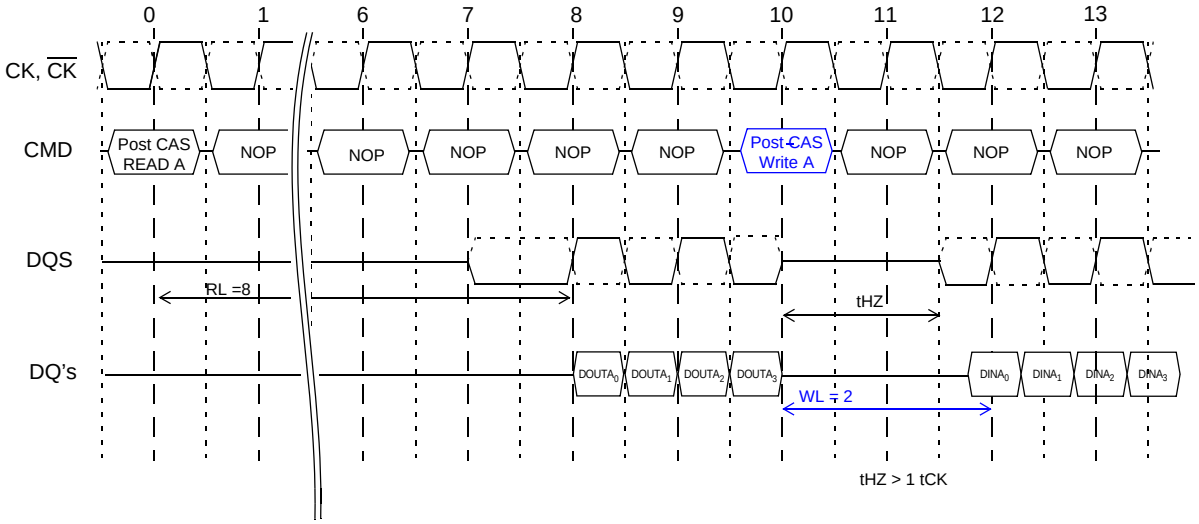
Burst Read Operation: RL = 8 (AL = 1, CL = 7)



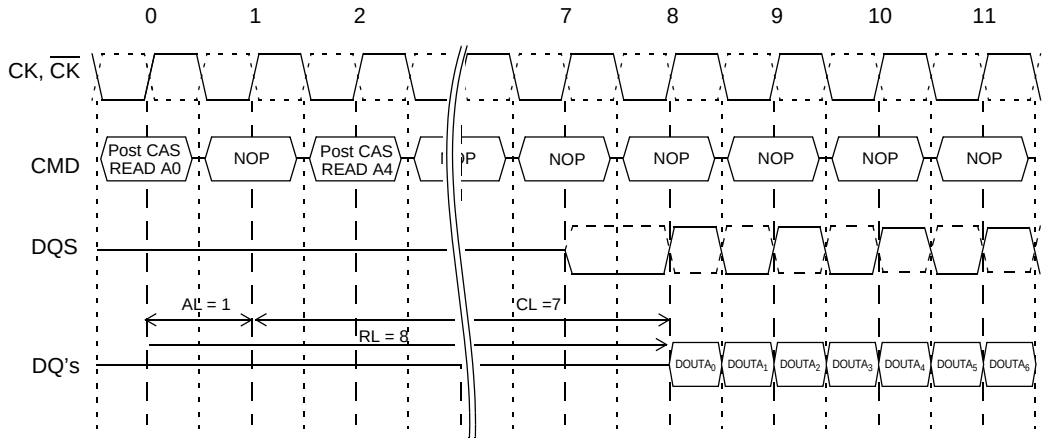
Burst Read Operation: RL = 7 (AL = 0 and CL = 7)



Burst Read followed by Burst Write : AL = 1, CL = 7, RL = 8, WL = (AL+1) = 2



Seamless Burst Read Operation: CL = 7, AL = 1, RL = 8

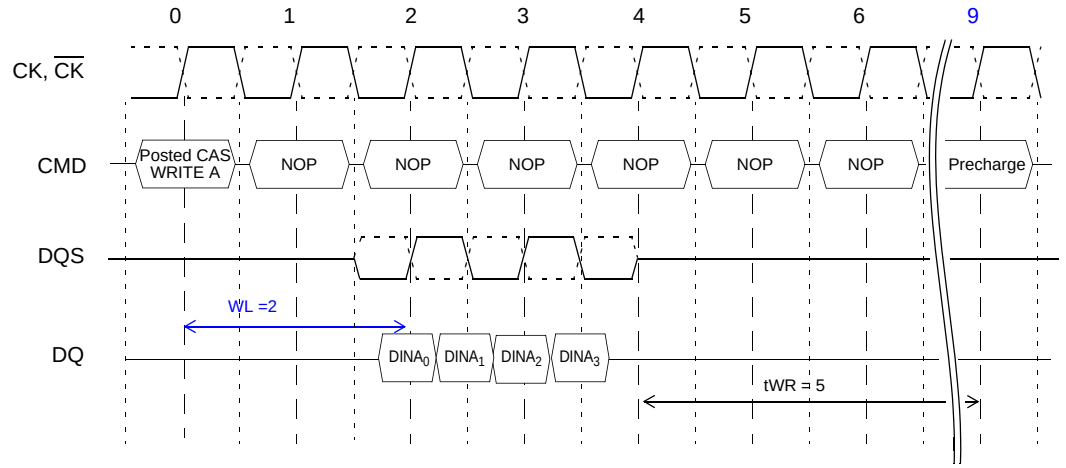


The seamless burst read operation is supported by enabling a read command at every other clock. This operation is allowed regardless of same or different banks as long as the banks are activated.

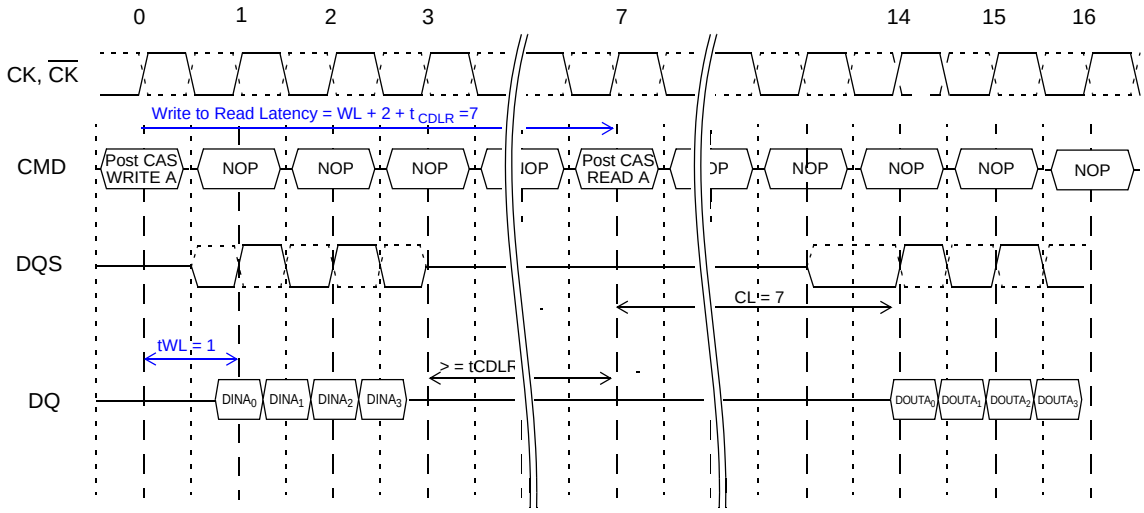
Burst Write Operation

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by an Additive Latency(AL) plus one and is equal to (AL + 1). The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the clock and at the first falling edge of the clock. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the clock until the burst length of 4 is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (tWR).

Burst Write Operation : AL= 1, CL = 7, WL = 2, t_{WR} = 5

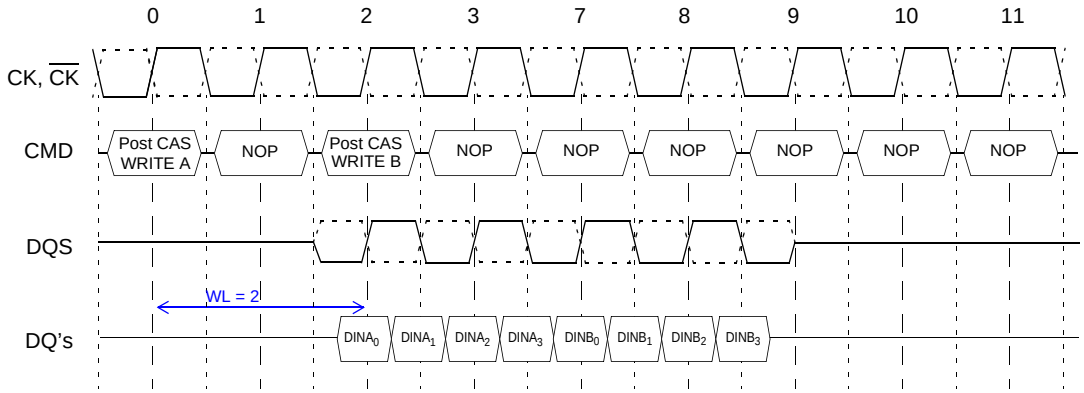


Burst Write followed by Burst Read : RL = 7 (AL=0, CL=7), WL = 1, tCDLR = 4



The minimum number of clock from the burst write command to the burst read command is WL+2+a write-to-read-turn-around-time(tCDLR).

Seamless Burst Write Operation : AL = 1, CL = 7, WL = AL + 1 = 2



The seamless burst write operation is supported by enabling a write command every other clock. This operation is allowed regardless of same or different banks as long as the banks are activated

Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A8, BA0 and BA1 are used to define which bank to precharge when the command is issued.

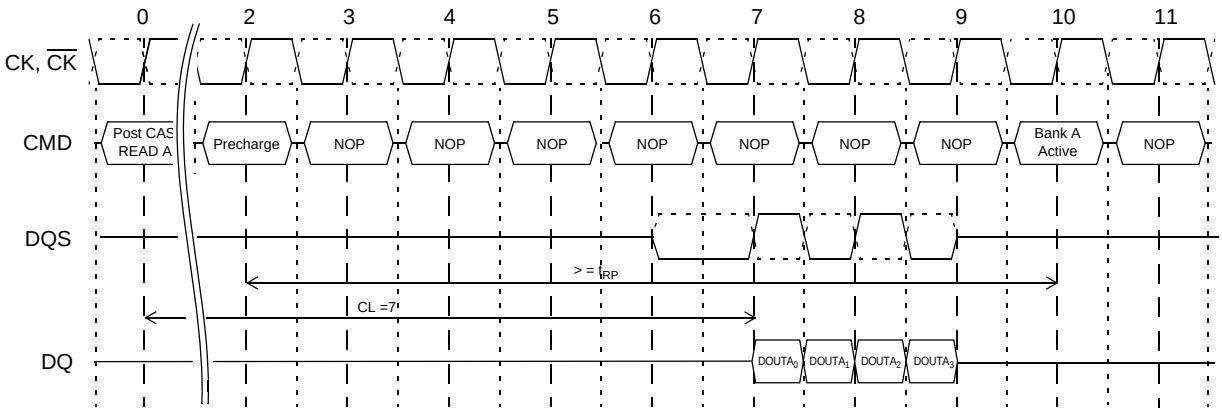
Bank Selection for Precharge by Address Bits

A8	BA1	BA0	Precharged Bank(s)
LOW	LOW	LOW	Bank 0 only
LOW	LOW	HIGH	Bank 1 only
LOW	HIGH	LOW	Bank 2 only
LOW	HIGH	HIGH	Bank 3 only
HIGH	DON'T CARE	DON'T CARE	All Banks 0 ~ 3

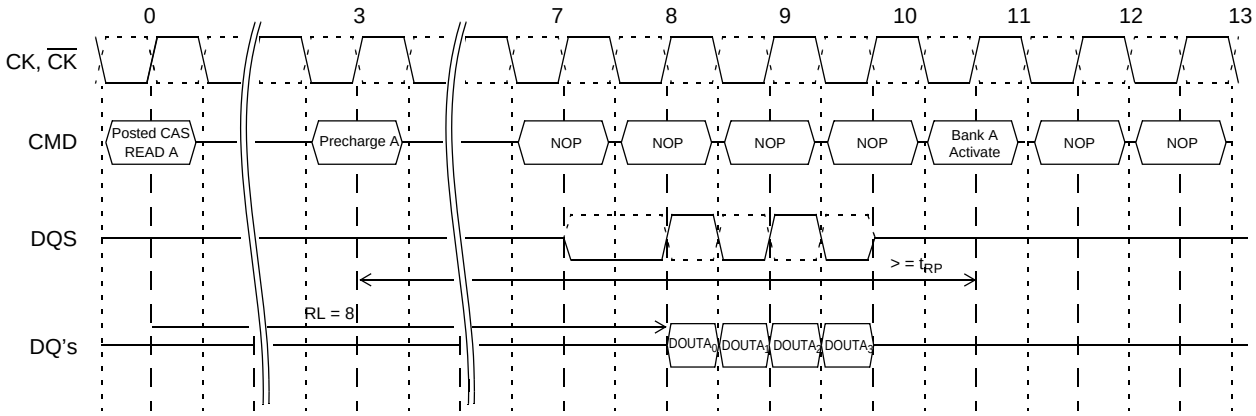
Burst Read Operation Followed by Precharge

For the earliest possible precharge, the precharge command may be issued on the rising edge which is CAS latency (CL) clock cycles before the end of the read burst. A new bank active (command) may be issued to the same bank after the RAS precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.

Burst Read Operation Followed by Precharge: RL = 7 (AL=0, CL=7), t_{RP}= 8



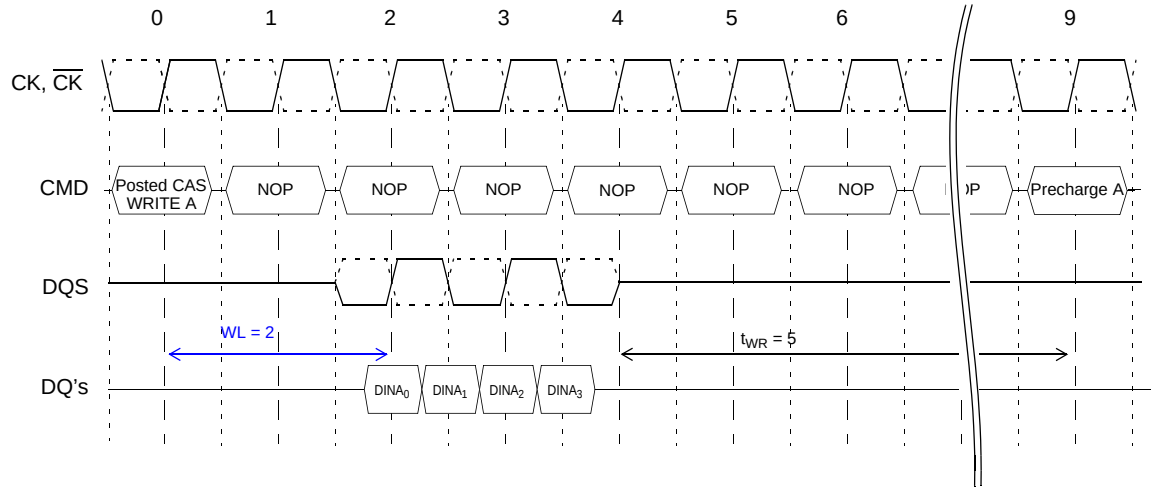
Burst Read Operation Followed by Precharge: RL = 8 (AL=1, CL=7, t_{RP} =8)



Burst Write followed by Precharge

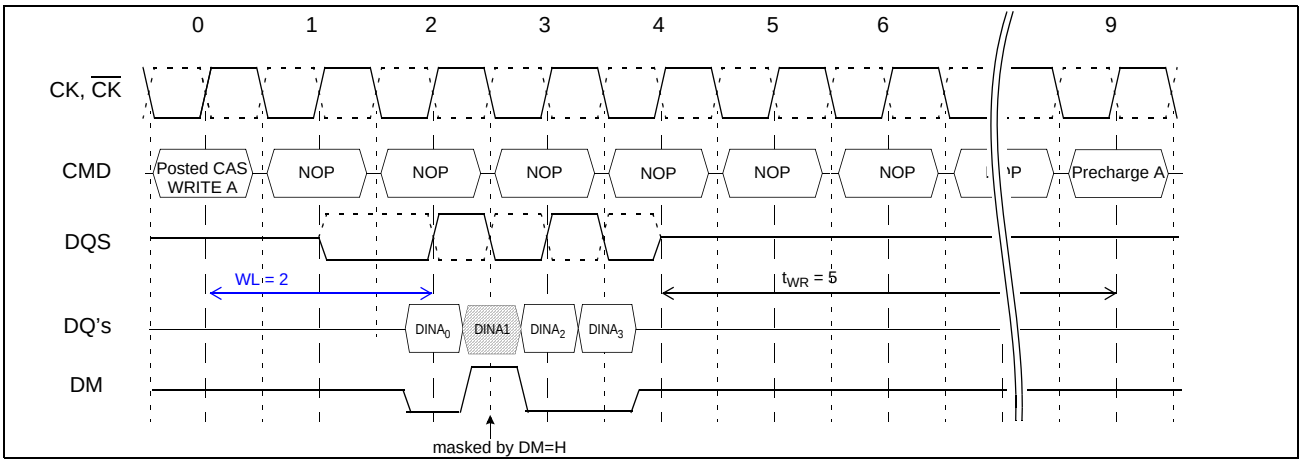
For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (t_{WR}) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the tWR delay, as GDDR2 SDRAM does not support any burst interrupt operation.

Burst Write followed by Precharge: AL = 1, CL = 7, WL = AL + 1 = 2, t_{WR} = 5



DM FUNCTION

The DDR SDRAM has a Data mask function that can be used in conjunction with data Write cycle only, not Read cycle. When the Data Mask is activated (DM high) during write operation the write data is masked immediately (DM to Data-mask Latency is zero).
DM must be issued at the rising edge or the falling edge of Data Strobe instead of a clock edge.



Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the auto-precharge function. When a Read or a Write Command is given to the GDDR2 SDRAM, the CAS timing accepts one extra address, column address A8, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A8 is low when the READ or WRITE Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A8 is high when the Read or Write Command is issued, then the auto-precharge function is engaged.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

Auto-precharge also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

Burst Read with Auto Precharge

If A8 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The GDDR2 SDRAM starts an Auto Precharge operation on the rising edge which is (AL + BL/2)cycles later from the read with Auto Precharge command, when tRAS(min) is satisfied. If tRAS(min) is not satisfied at the edge, the start point of Auto Precharge operation will be delayed until tRAS(min) is satisfied. A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously.

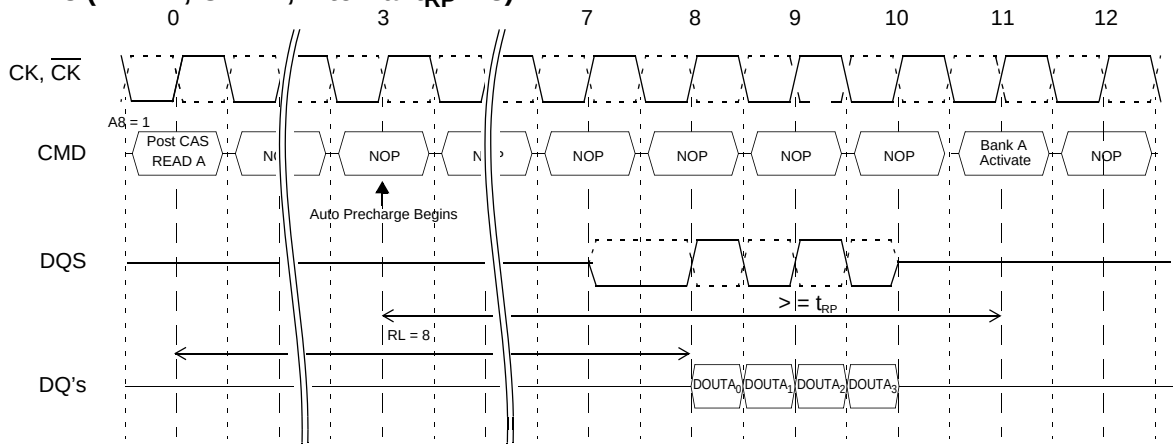
(1) The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

(2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

When the Read with Auto-Precharge command is issued, new command (Read, Read with Auto Precharge or precharge) of same bank can be asserted tCCD=2 clock cycles later.

Burst Read with Auto Precharge Followed by Same Bank Activation :

RL = 8 (AL = 1, CL = 7, internal t_{RP} = 8)



Burst Read with Auto Precharge (AL=0)

Asserted command	For same bank				For different bank			
	1	2	3	4	1	2	3	4
READ	Illegal	Legal	Illegal	Illegal	Illegal	Legal	Legal	Legal
READ with Auto Precharge	Illegal	Legal	Illegal	Illegal	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal
Precharge	Illegal	Legal	Illegal	Illegal	Legal	Legal	Legal	Legal

*When AL(Additive Latency) is 1, a precharge command for same bank can be issued at 3th cycle only and others are same with AL=0.

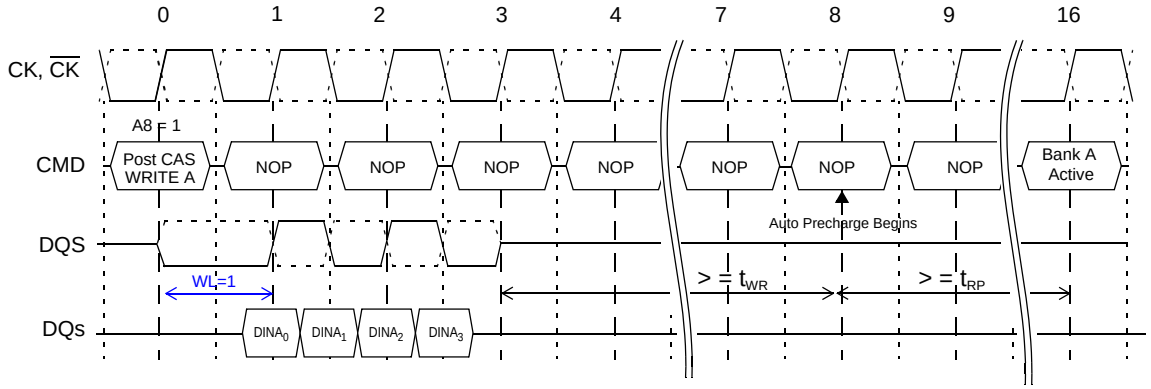
Burst Write with Auto-Precharge

If A8 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The GDDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (tWR). Interruption of the Write with Auto-Precharge function is prohibited. Active command of same bank can be issued WL+tWR+tRP+BL/2 cycles later from the Write with Auto-Precharge command. The bank undergoing Auto-Precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

(1) The data-in to bank activate delay time (tWR + tRP) has been satisfied.

(2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

Burst Write with Auto-Precharge : AL = 0, WL = 1, t_{WR} = 5, t_{RP}=8(for the same bank)



Burst Write with Auto-Precharge (AL=0)

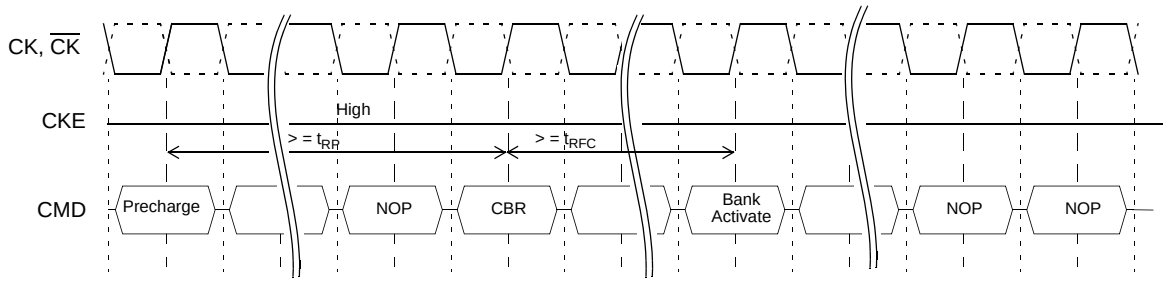
Asserted command	For same bank				For different bank		
	1 ~ 7	8	9 ~ 15	16	1	2 ~ 6	7
WRITE	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
WRITE with Auto Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
READ	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal
READ with Auto Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal
All Bank Precharge	Illegal	Legal	Legal	Legal	-		

*When AL(Additive Latency) is 1, a active command for same bank can be issued from 17th cycle , a READ or READ with Auto Precharge command for different bank can be issued from 8th cycle and others are same with AL=0.
* All Bank Precharge command can be issued from 8th cycle.

Automatic Refresh Command ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)

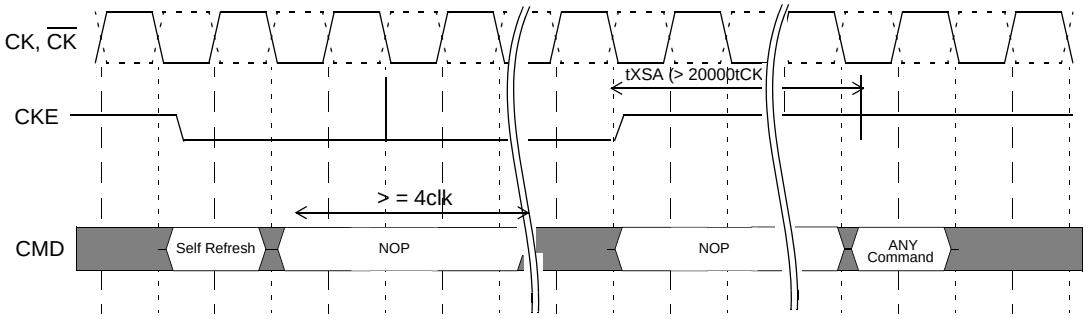
When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Automatic Refresh mode (CBR). All banks of the GDDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (t_{RP}) before the Auto Refresh Command (CBR) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the GDDR2 SDRAM will be in the precharged (idle) state. A delay between the Auto Refresh Command (CBR) and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the Auto Refresh cycle time (t_{RFC}).



Self Refresh Command

The GDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the Self Refresh Command is registered, CKE must be held low to keep the device in Self Refresh mode and NOP command should be issued or $\overline{CS}$ should be held high to ensure stable self refresh operation for next four cycles after the Self Refresh Command. When the GDDR2 SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self Refresh Operation to save power. The user may halt the external clock while the device is in Self Refresh mode, however, the clock must be restarted before the device can exit Self Refresh operation. After CKE is brought high, an internal timer is started to insure CKE is held high for approximately 10ns before registering the Self Refresh exit command. The purpose of this circuit is to filter out noise glitches on the CKE input which may cause the GDDR2 SDRAM to erroneously exit Self Refresh operation. Once the Self Refresh exit command is registered, a delay equal or longer than the tXSA (>20000 tck) must be satisfied before any command can be issued to the device. CKE must remain high for the entire Self Refresh exit period (tXSA > 20000tCK) and commands must be gated off with $\overline{CS}$ held high. Alternatively, NOP commands may be registered on each positive clock edge during the Self Refresh exit interval. (See Figure.)



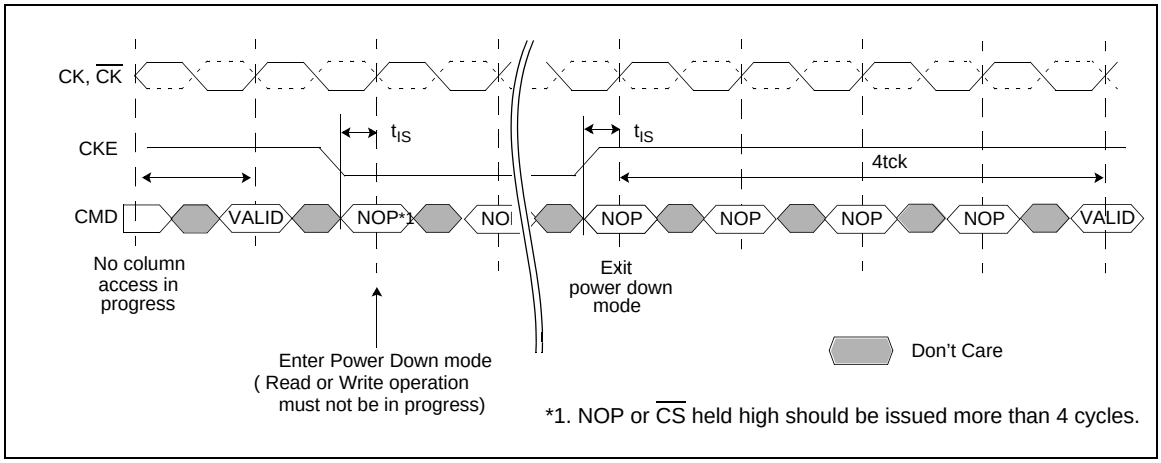
*After self refresh entry, NOP or chip deselect command should be issued during more than 4 cycles and chip deselet command should be issued for tXSA after self refresh exit.

Power-Down

Power-down is entered when CKE is registered LOW (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. During 4 cycles after power down mode issued, NOP should be issued or $\overline{CS}$ must be held high. In Power Down mode, CKE Low and a stable clock signal must be maintained at the inputs of the GDDR2 SDRAM, and all other input signals are “Don’t Care” except first 4 cycles after power down mode issued. Power-down duration is limited by the refresh requirements of the device.

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or $\overline{CS}$ hold high). A valid, executable command may be applied four clock cycles later.

Power Down



*CL + 2tCK after read or CL after last data in, a power-down command can be issued.

Burst Interruption

Interruption of a burst read or write cycle is prohibited.

No Operation Command

The No Operation Command should be used in cases when the GDDR2 SDRAM is in an idle or a wait state. The purpose of the No Operation Command is to prevent the GDDR2 SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle. The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high at the rising edge of the clock, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don’t cares.

On-Die Termination

All pins except ZQ, CKE Pins adopt on-die termination to improve signal integrity of channel. The On-Die Termination should be controlled by EMRS command at low frequency clock (<100Mhz). The On-Die Termination control command should be issued before issuing DLLON command by EMRS or simultaneously to guarantee stable channel condition of /CK and CK pins. If A3, A2 = 0, 0, the On-Die Termination of all pins will be deactivated. If A3, A2 = 0, 1, the On-Die Termination will be self-calibrated by detecting the external Resistor on ZQ pin. If A3, A2 = 1, 0, the value of the On-Die Termination of CK, /CK, 32 DQ's, 4 DM's, 4 /DQS's and 4DQS pins will be the fixed value, 60ohm. If A3, A2 = 1, 1, the value of the On-Die Termination of CK, /CK, 32 DQ's, 4 DM's, 4 /DQS's and 4DQS pins will be the fixed value,120ohm.

If A3, A2 = 0, 1 is issued by EMRS, the value of the on-die termination of each pin is determined by monitoring the value of a external resistor which is connected between ZQ pin and VSSQ, and updated every CBR refresh cycle to compensate variation of voltage and temperature.

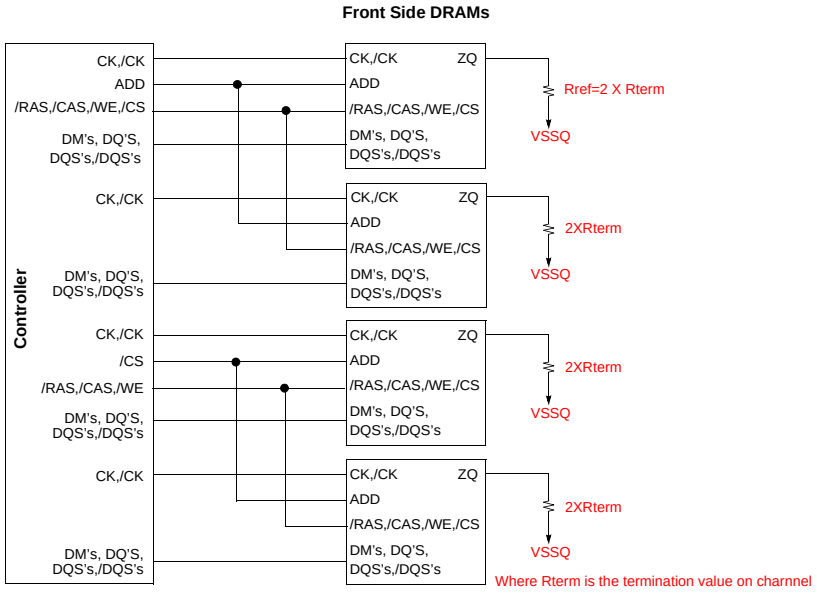
The value of On-Die Termination of CMD and ADD (/RAS, /CAS, /WE, /CS, BA0, BA1 and A0 ~ A11) pins of each DRAM depend on EMRS code (A1, A0). If A1, A0 = 0, 0 , the On-die Termination of CMD and ADD pins will be deactivated. If A1, A0 = 0, 1, the value of the On-die Termination of CMD and ADD pins will be same value as the value of DQ pins. If A1, A0 = 1, 0, the value of the On-Die Termination of CMD and ADD pins will be two times of the value of DQ pins. If A1, A0 = 1, 1, the value of the On-Die Termination of CMD and ADD pins will be four times of the value of DQ pins.

The On-Die Termination for one bank system with self-calibration code (A3, A2 = 0, 1)

The value of external resistor (Rref) at external one bank system is 2 times of target termination value of DQ's on channel (Rterm). Then the value of On-Die Termination of CK, /CK, 32 DQ's, 4 DM's, 4 /DQS's and 4DQS pins is half value of the external resistor. The value of On-Die Termination of CMD and ADD (/RAS, /CAS, /WE, /CS, BA0, BA1 and A0 ~ A11) pins of each DRAM depend on EMRS code (A2, A0).

The following figure shows the typical external one bank system having on-die termination.

Block Diagram of 1 Bank System



The On-die Termination on/off status on DRAM is in accompany with DRAM operation mode.

Power consumption by On-die termination can be reduced by issuing power down mode.

On-Die Termination (ODT) Status of 1 Bank System

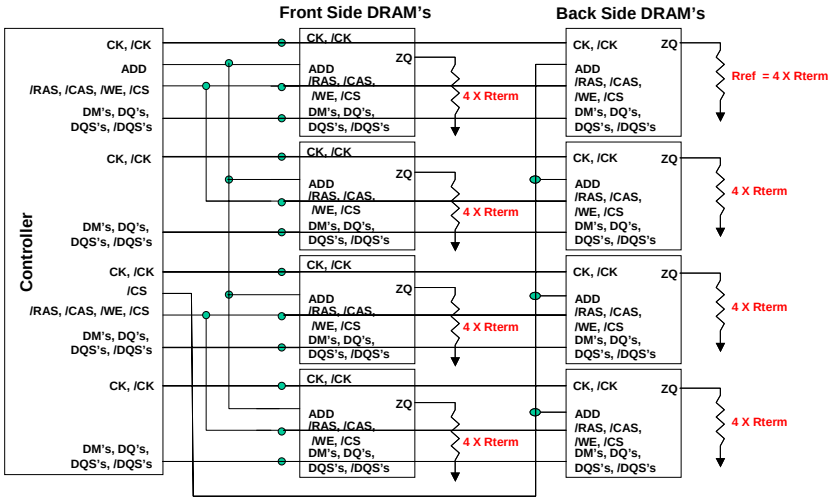
Mode		Pin	ODT of DRAM
Self_refresh		All	OFF
Power Down		CK, /CK	ON
		Other pins	OFF
Active		All	ON
All banks idle		CK, /CK, ADD's, CMD	ON
		DQ's, DQS's, /DQS's, DM's	ON
READ	A10=1	CK, /CK, ADD's, CMD, DM,s	ON
		DQ's, DQS's, /DQS's	OFF
	A10=0	CK, /CK, ADD's, CMD, DM,s	ON
		DQ's, DQS's, /DQS's	ON

*** A10 in EMRS code is used for On-Die Termination of DQ's off when Read data comes out**

The On-die Termination for external two bank system with self-calibration code (A3, A2 = 0, 1)

The external resistor (Rref) is equal to 2X the number of shared DRAM's on one channel X target termination value of DQ channel. The following figure is represented the typical two bank system having on-die termination. 4 DRAM's share one channel for CMD and ADD pins and 2 DRAM's share one channel for DQ's and CLK pins. The external resistor (Rref) is 4 times of target termination value on channel. The On-die Termination value of CK, /CK, 32 DQ's, 4 DM's, 4 /DQS's and 4DQS pins on channel is half value of the external resistor (Rref).

Block Diagram of 2 Banks System



Self-refresh and power down mode in two bank system should be issued for all DRAM's at the same time to keep suitable On-die termination condition on channel.

Mode			Pin	DRAM		Remarks
M1	M2			M1	M2	
Self_refresh	Self_refresh		All	OFF	OFF	*1
Self_refresh	Other States		All			Illegal
Power down	Power down		CK,/CK	ON	ON	
			Other pins	OFF	OFF	*1
Power down	Other States					Illegal
All Banks idle	Active		CK, /CK, ADD's, CMD	ON	ON	
			DQ's, DQS's, /DQS's, DM's	ON	ON	
	Read	A10=1	CK, /CK, ADD's, CMD	ON	ON	
			DQ's, DQS's, /DQS's, DM's	ON	OFF	
		A10=0	CK, /CK, ADD's, CMD	ON	ON	
			DQ's, DQS's, /DQS's, DM's	ON	ON	
Active	Read	A10=1	CK, /CK, ADD's, CMD	ON	ON	
			DQ's, DQS's, /DQS's, DM's	ON	OFF	
		A10=0	CK, /CK, ADD's, CMD	ON	ON	
			DQ's, DQS's, /DQS's, DM's	ON	ON	

1. With these case, the system couldn't have suitable Rterm.
   Because the On-Die termination value on channel is two times than the target value.

4. Command Truth Table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	BA0/BA1	A11 - A9	A8	A7 - A0	Notes
	Previous Cycle	Current Cycle										
Mode Register Set	H	X	L	L	L	L	X	BA0 = 0 and MRS OP Code				1
Extended Mode Register Set	H	X	L	L	L	L	X	BA0 = 1 and EMRS OP Code				1
Auto (CBR) Refresh	H	H	L	L	L	H	X	X	X	X	X	1
Entry Self Refresh	H	L	L	L	L	H	X	X	X	X	X	1
Exit Self Refresh	L	H	H	X	X	X	X	X	X	X	X	1
	L	H	L	H	H	H	X	X	X	X	X	
Single Bank Precharge	H	X	L	L	H	L	X	BA	X	L	X	1,2
Precharge all Banks	H	X	L	L	H	L	X	X	X	H	X	1
Bank Activate	H	X	L	L	H	H	X	BA	Row Address			1,2
Write	H	X	L	H	L	L	X	BA	X	L	Column	1,2,3,
Write with Auto Precharge	H	X	L	H	L	L	X	BA	X	H	Column	1,2,3,
Read	H	X	L	H	L	H	X	BA	X	L	Column	1,2,3
Read with Auto-Precharge	H	X	L	H	L	H	X	BA	X	H	Column	1,2,3
DM	H	X	X	X	X	X	DM	X	X	X	X	6
No Operation	H	X	L	H	H	H	X	X	X	X	X	1
	H	X	H	X	X	X	X	X	X	X	X	1
Power Down Mode Entry	H	L	H	X	X	X	X	X	X	X	X	1,4,5
	H	L	L	H	H	H	X	X	X	X	X	
Power Down Mode Exit	L	H	H	X	X	X	X	X	X	X	X	1,4,5
	L	H	L	H	H	H	X	X	X	X	X	

1. All of the GDDR2 SDRAM operations are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, and $\overline{CAS}$ at the positive rising edge of the clock.
2. Bank Select (BA0,1), determine which bank is to be operated upon.
3. Burst read or write cycle may not be terminated.
4. The Power Down Mode does not perform any refresh operations, therefore the device can't remain in this mode longer than the Refresh period (t_{REF}) of the device. Four clock delay is required for mode entry and exit.
5. If $\overline{CS}$ is low, then when CKE returns high, no command is registered into the chip for one clock cycle.
6. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

5. Clock Enable (CKE) Truth Table

Current State	CKE		Command					Action	Notes
	Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1, BA0, A11 - A0		
Self Refresh	H	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	Exit Self Refresh with No Operation	2
	L	H	L	Command			Address	ILLEGAL	2
	L	L	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	Power Down mode exit, all banks idle	2
	L	H	L	H	H	H	X	Exit Power Down mode with No Operation	2
	L	H	L	Command			Address	ILLEGAL	2
	L	L	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X		Device Deselect	3
	H	H	L	Command			Address	Refer to the Current State Truth Table	3
	H	L	H	X	X	X		Power Down	
	H	L	L	Command except self-refresh command			X	ILLEGAL	
	H	L	L	L	L	H	X	Entry Self Refresh	4
Any State other than listed above	H	H	X	X	X	X	X	Refer to operations in the Current State Truth Table	
	H	L	X	X	X	X	X	Power Down	5
	L	H	X	X	X	X	X	Power Down	
	L	L	X	X	X	X	X	Power Down	

1. For the given Current State CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE (t_{CES}) must be satisfied before any command other than self refresh exit.
3. The inputs (BA1, BA0, A11 - A0) depend on the command that is issued. See the Current State Truth Table for more information.
4. The Auto Refresh, Self Refresh Mode, and the Mode Register Set modes can only be entered from the all banks idle state.
5. Must be a legal command as defined in the Current State Truth Table.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4.5	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS(SSTL_18 In/Out)

Recommended operating conditions (Voltage referenced to V_{SS}=0V, T_j=0 to 100°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	V_{DD}	2.4	2.5	2.6	V	1
Output Supply voltage	V_{DDQ}	1.7	1.8	1.9	V	1
Reference voltage	V_{REF}	0.49*V_{DDQ}	-	0.51*V_{DDQ}	V	2
DC Input logic high voltage	V_{IH} (DC)	V_{REF}+0.125	-	V_{DDQ}+0.30	V	4
DC Input logic low voltage	V_{IL} (DC)	-0.30	-	V_{REF}-0.125	V	5
AC Input logic high voltage	V_{IH}(AC)	V_{REF}+0.25	-	-	V	
AC Input logic low voltage	V_{IL}(AC)	-	-	V_{REF}-0.25	V	
Output logic high voltage	V_{OH}	Vtt+0.4	-	-	V	6
Output logic low voltage	V_{OL}	-	-	Vtt-0.4	V	6
Input leakage current	I_{IL}	-5	-	5	uA	7
Output leakage current	I_{OL}	-5	-	5	uA	7

Note :
1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{REF} is expected to equal 0.50*V_{DDQ} of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the V_{REF} may not exceed + 2% of the DC value. Thus, from 0.50*V_{DDQ}, V_{REF} is allowed + 25mV for DC error and an additional + 25mV for AC noise.
3. V_{tt} of the transmitting device must track V_{REF} of the receiving device.
4. V_{IH}(max.)= V_{DDQ} +1.5V for a pulse and it which can not be greater than 1/3 of the cycle rate.
5. V_{IL}(mim.)= -1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
6. Output logic high voltage and low voltage is depend on channel condition.(Ract , Ron)
7. For any pin under test input of 0V $\leq$ V_{IN} $\leq$ V_{DD} is acceptable. For all other pins that are not under test V_{IN}=0V

DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, T_j=0 to 100°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-20	-22	-25		
Operating Current (One Bank Active)	I_{CC1}	Burst Lenth=4 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA, t_{CC}= t_{CC}(min)	590	540	500	mA	1
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC}= t_{CC}(min)	110	100	95	mA	
Precharge Standby Current in Non Power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), t_{CC}= t_{CC}(min)	230	210	190	mA	
Active Standby Current power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC}= t_{CC}(min)	110	100	95	mA	
Active Standby Current in in Non Power-down mode	I_{CC3N}	CKE ≥ VIH(min), CS ≥ VIH(min), t_{CC}= t_{CC}(min)	510	470	430	mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL}=0mA ,t_{CC}= t_{CC}(min), Page Burst, All Banks activated.	1200	1100	990	mA	
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RFC}$	370	350	330	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	7			mA	
Operating Current (4Bank interleaving)	I_{CC7}	Burst Lenth=4 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA, t_{CC}= t_{CC}(min)	1400	1300	1180	mA	

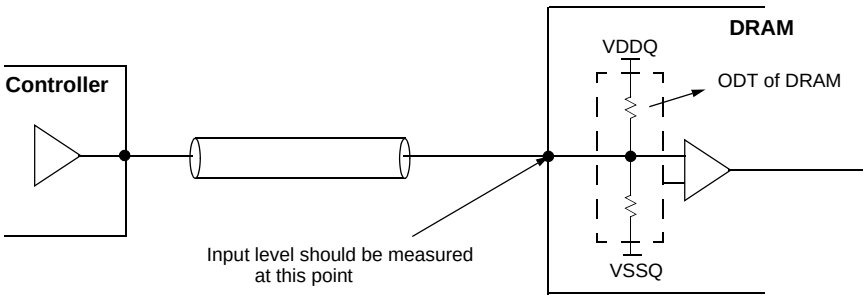
Note : 1. Measured with outputs open & On-Die termination off.
2. Refresh period is 16ms.

AC INPUT OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS}=0V, V_{DD}=2.5V ± 0.1V, V_{DDQ}=1.8V ± 0.1V, T_j=0 to 100 °C)

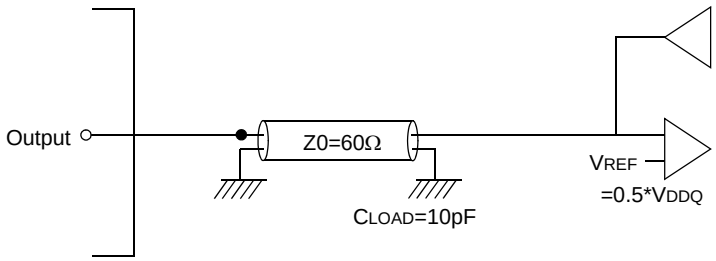
Parameter	Symbol	Min	Typ	Max	Unit	Note
Input High (Logic 1) Voltage; DQ	V_{IH}	V_{REF}+0.25	-	-	V	1
Input Low (Logic 0) Voltage; DQ	V_{IL}	-	-	V_{REF}-0.25	V	2
Clock Input Differential Voltage ; CK and $\overline{CK}$	V_{ID}	0.5	-	V_{DDQ}+0.6	V	3
Clock Input Crossing Point Voltage ; CK and $\overline{CK}$	V_{IX}	0.5*V_{DDQ}-0.2	-	0.5*V_{DDQ}+0.2	V	4

Note : 1. V_{IH}(Max) = 4.2V. The overshoot voltage duration is < 3ns at VDD.
V_{IH} level should be met at the pin of DRAM when ODT=ON.
2. V_{IL}(Min) = -1.5V. The undershoot voltage duration is < 3ns at VSS.
V_{IL} level should be met at the pin of DRAM when ODT=ON.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same



AC OPERATING TEST CONDITIONS (V_{DD}=2.5V±0.1V, T_j= 0 to 100 °C)

Parameter	Value	Unit	Note
Input reference voltage for CK(for single)	0.50*V_{DDQ}	V	
CK and $\overline{CK}$ signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.25/V_{REF}-0.25	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	1/2 V_{DDQ}	V	
Output load condition	See Fig.1		



(Fig. 1) Output Load Circuit

CAPACITANCE (V_{DD}=2.5V, T_A= 25°C, f=1MHz)

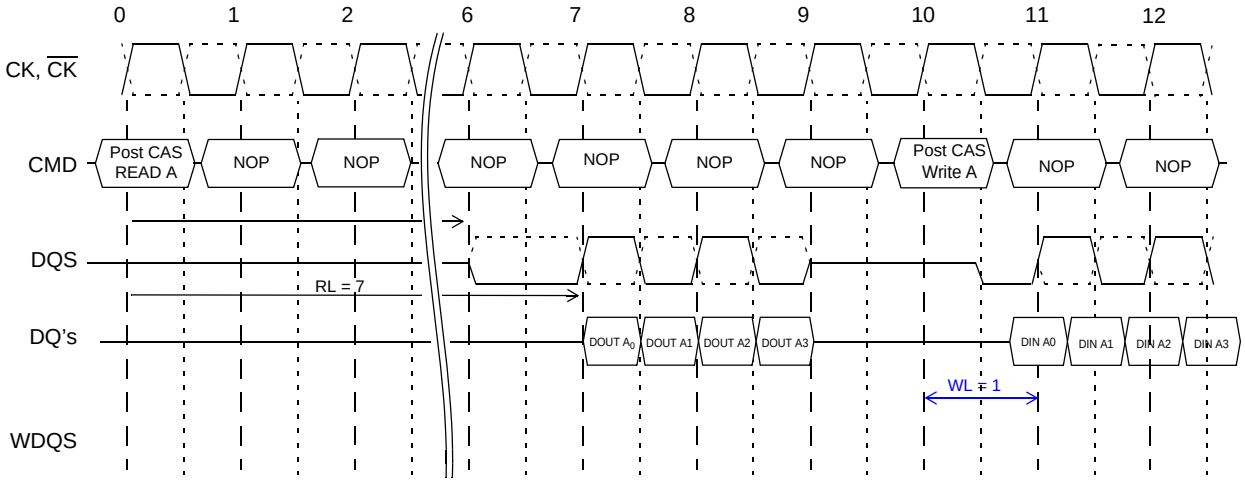
Parameter	Symbol	Min	Max	Unit
Input capacitance (CK, $\overline{CK}$)	C_{IN1}	3.0	5	pF
Input capacitance (A_0~A_{10}, BA_0~BA_1)	C_{IN2}	3.0	5	pF
Input capacitance (CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN3}	3.0	5	pF
Data & DQS input/output capacitance(DQ_0~DQ_{31})	C_{OUT}	3.0	5	pF
Input capacitance(DM0 ~ DM3)	C_{IN4}	3.0	5	pF

AC CHARACTERISTICS

Parameter		Symbol	-20 (GF1000)		-22 (GF900)		-25 (GF800)		Unit
			Min	Max	Min	Max	Min	Max	
CK cycle time	CL=7	tCK	2.0	4.0	-	-	-	-	ns
	CL=6		-	-	2.22	4.0	-	-	ns
	CL=5		-	-	-	-	2.5	4.0	ns
CK high width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK low width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK
DQS out access time from CK		tDQSCK	-0.35	0.35	-0.45	0.45	-0.45	0.45	ns
Data strobe edge to Dout edge		tDQSQ	-0.225	0.225	-0.25	0.25	-0.28	0.28	ns
Read preamble		tRPRE	0.85	1.15	0.88	1.12	0.9	1.1	tCK
Read postamble		tRPST	0.35	0.65	0.38	0.62	0.4	0.6	tCK
DQS in/out high level		tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK
DQS in/out low level		tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Address and Control input setup		tIS	0.5	-	0.55	-	0.6	-	ns
Address and Control input hold		tIH	0.5	-	0.55	-	0.6	-	ns
Write command to first DQS latching transition		tDQSS	WL - 0.15	WL + 0.15	WL - 0.15	WL + 0.15	WL - 0.15	WL + 0.15	tCK
Write preamble setup time		tWPRES	0	-	0	-	0	-	ps
Write postamble		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write preamble		tWPRE	0.35	-	0.35	-	0.35	-	tCK
DQ_in and DM setup time to DQS		tDS	0.25	-	0.27	-	0.3	-	ns
DQ_in and DM hold time to DQS		tDH	0.25	-	0.27	-	0.3	-	ns
Clock half period		tHP	tCL/H min	-	tCL/H min	-	tCL/H min	-	ns
Data output hold time from DQS		tQH	tHP-0.225	-	tHP-0.25	-	tHP-0.28	-	ns
Jitter over 1-6 clock cycles of CK		tJ *1	-	50	-	55	-	65	ps
Cycle to Cycle duty cycle error		tDC,ERR	-	50	-	55	-	65	ps
Rise and fall times of CK		tR, tF	-	400	-	450	-	500	ps

1. The cycle to cycle jitter and 2~6 cycle short term jitter.

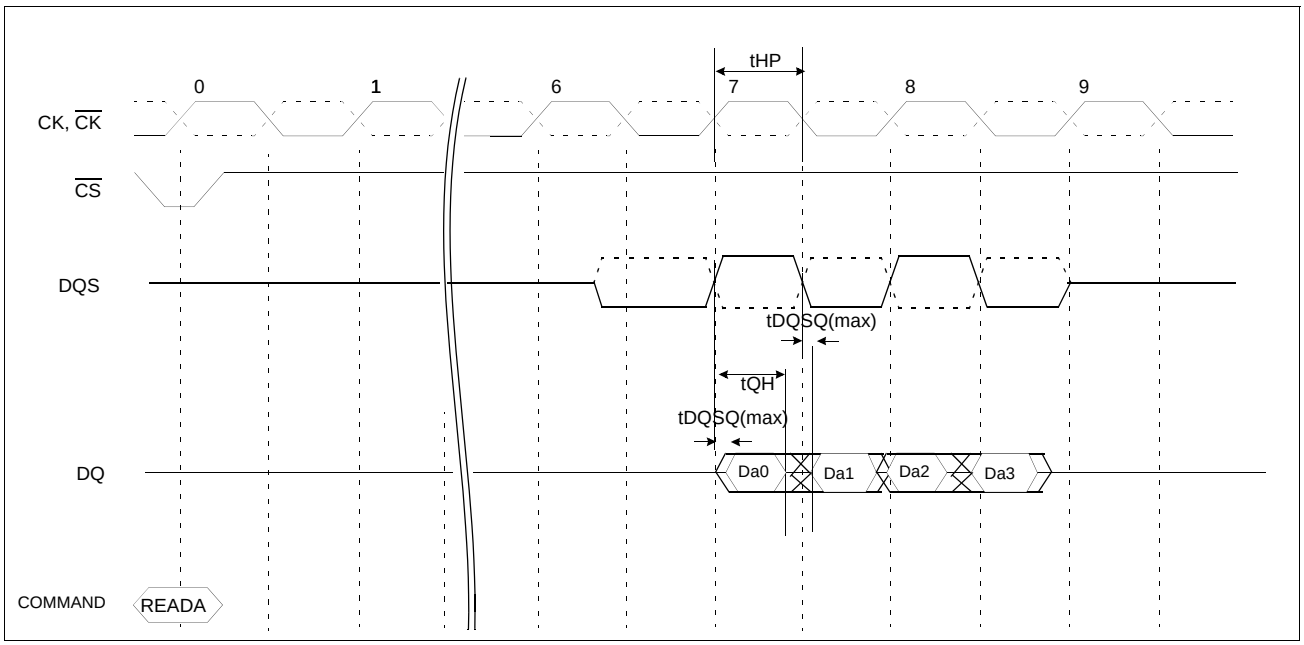
Simplified Timing @ BL=4, CL=7, AL=0



Note 1 :

- The JEDEC DDR-II specification currently defines the output data valid window(tDV) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of tDV(=0.35tCK) artificially penalizes system timing budgets by assuming the worst case output valid window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term, tQH which stands for data output hold time from DQS is defined to account for clock duty cycle variation and replaces tDV
- tQHmin = tHP-X where
  . tHP=Minimum half clock period for any given cycle and is defined by clock high or clock low time(tCH,tCL)
  . X=A frequency dependent timing allowance account for tDQSQmax

tQH Timing (CL7, BL4)

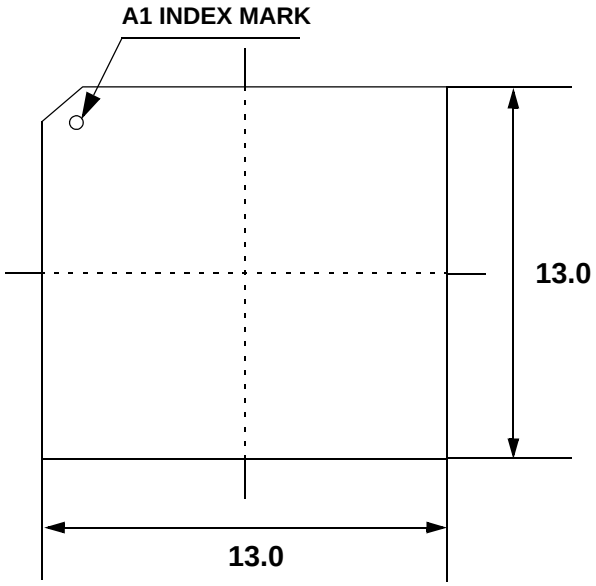


AC CHARACTERISTICS (I)

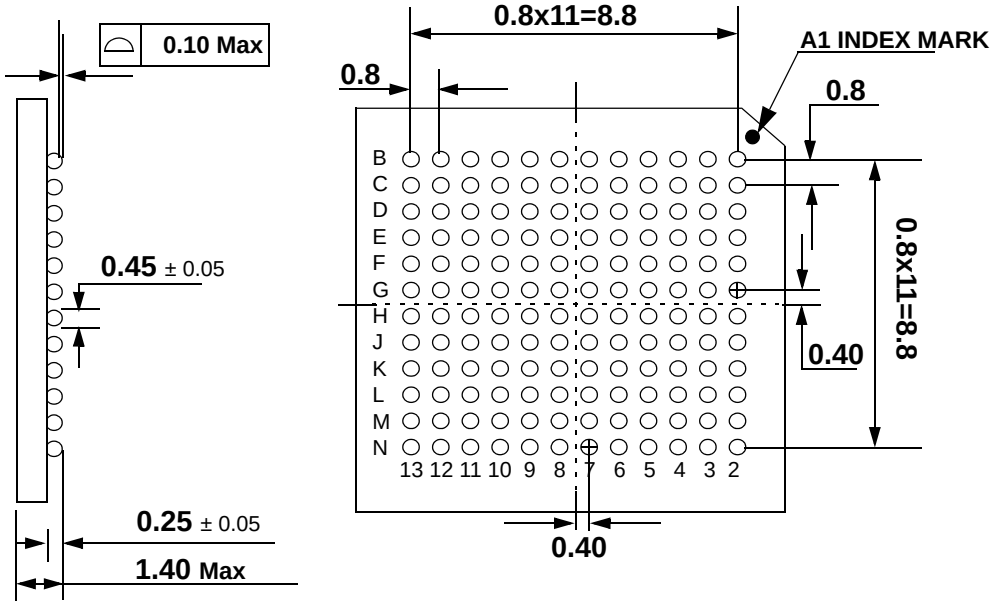
Parameter	Symbol	-20 (GF1000)		-22 (GF900)		-25 (GF800)		Unit
		Min	Max	Min	Max	Min	Max	
Row cycle time	tRC	22	-	21	-	18	-	tCK
Refresh row cycle time	tRFC	27	-	25	-	22	-	tCK
Row active time	tRAS	15	100K	14	100K	12	100K	tCK
RAS to CAS delay for Read	tRCDRD	8	-	8	-	7	-	tCK
RAS to CAS delay for Write	tRCDWR	5	-	5	-	4	-	tCK
Row precharge time	tRP	7	-	7	-	6	-	tCK
Row active to Row active	tRRD	5	-	5	-	4	-	tCK
Last data in to Row precharge	tWR	5	-	5	-	4	-	tCK
Last data in to Read command	tCDLR	4	-	4	-	4	-	tCK
Col. address to Col. address	tCCD	2	-	2	-	2	-	tCK
Mode register set cycle time	tMRD	4	-	4	-	4	-	tCK
Auto precharge write recovery + Precharge	tDAL	12	-	12	-	10	-	tCK
Exit self refresh to any command	tXSA	20000	-	20000	-	20000	-	tCK
Power down exit time	tPDEX	4tCK+tIS	-	4tCK+tIS	-	4tCK+tIS	-	ns
Refresh interval time	tREF	7.8	-	7.8	-	7.8	-	us

Note : 1. For normal write operation, even numbers of Din are to be written inside DRAM

PACKAGE DIMENSIONS (FBGA)



<Top View>



<Bottom View>

Unit : mm

IBIS: I/V Characteristics for Input and Output Buffers

The termination resistor of the controller must be set to a appropriate value to satisfy output voltage level if the ODT of DRAM is on.

30 ohm Driver @ ODT OFF

1. The typical pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.

2. The 30 ohm@ODT OFF variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.

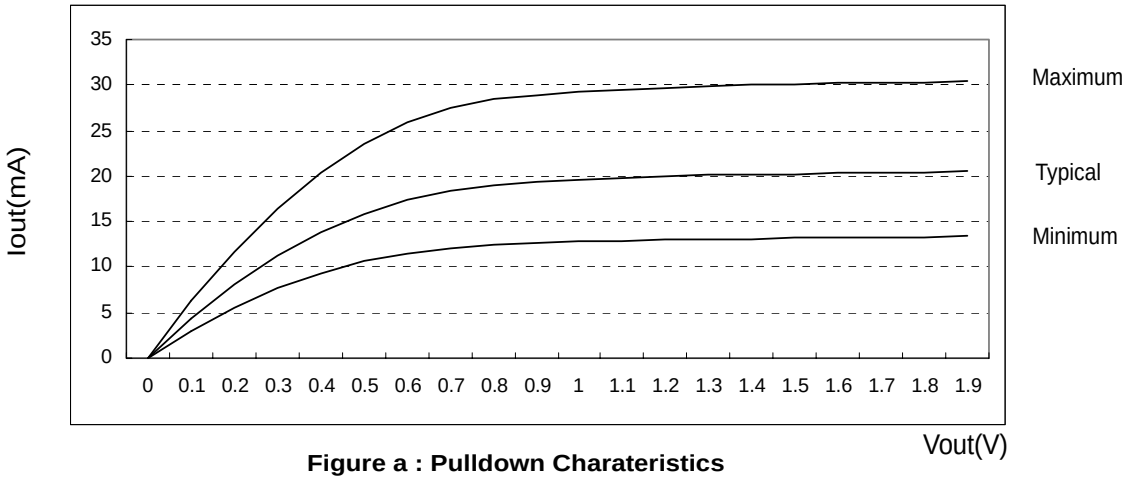


Figure a : Pulldown Charateristics

3. The typical pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.

4. The 30 ohm@ODT OFF variation pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figrue b.

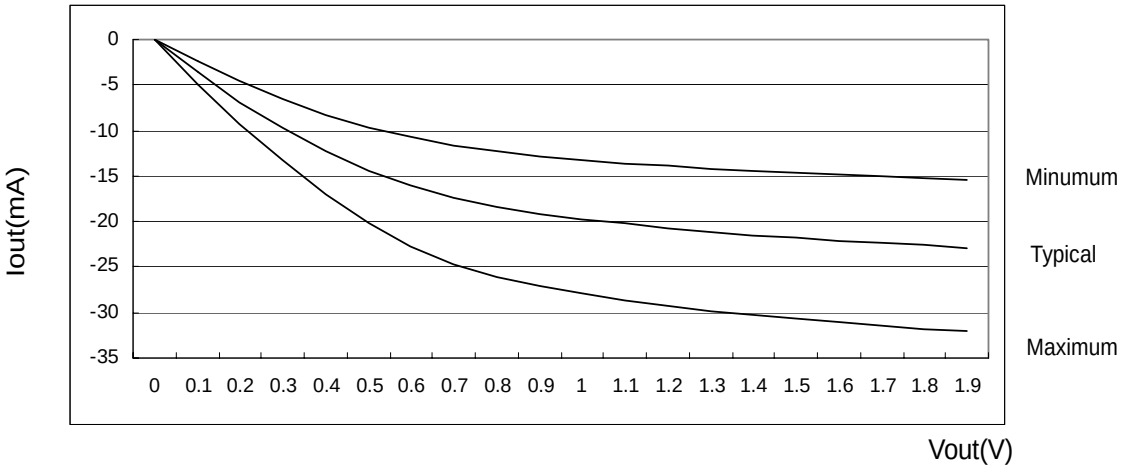


Figure b : PulluP Charateristics

5. The 30 ohm@ODT OFF variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to VDDQ/2

6. The 30 ohm@ODT OFF variation in the ratio of the nominal pullup to pulldown current should be unity ±10%, for device drain to source voltages from 0 to VDDQ/2

	Pulldown Current (mA)			Pullup Current (mA)		
Voltage (V)	Typical	Minimum	Maximum	Typical	Minimum	Maximum
0.0	0.0	0.0	0.0	0.0	0.0	0.0
0.1	4.4	3.0	6.3	-3.6	-2.5	-4.9
0.2	8.1	5.5	11.8	-6.9	-4.6	-9.3
0.3	11.2	7.6	16.4	-9.7	-6.6	-13.3
0.4	13.8	9.3	20.4	-12.2	-8.2	-17.0
0.5	15.9	10.6	23.5	-14.3	-9.6	-20.1
0.6	17.4	11.5	25.9	-16.1	-10.7	-22.7
0.7	18.4	12.1	27.5	-17.4	-11.6	-24.6
0.8	19.0	12.4	28.4	-18.4	-12.3	-26.0
0.9	19.4	12.6	29.0	-19.1	-12.8	-27.1
1.0	19.7	12.8	29.3	-19.7	-13.2	-28.0
1.1	19.8	12.9	29.5	-20.3	-13.6	-28.7
1.2	20.0	13.0	29.7	-20.7	-13.9	-29.3
1.3	20.1	13.1	29.9	-21.1	-14.2	-29.8
1.4	20.2	13.1	30.0	-21.5	-14.5	-30.3
1.5	20.2	13.2	30.1	-21.8	-14.7	-30.7
1.6	20.3	13.2	30.2	-22.1	-14.9	-31.1
1.7	20.4	13.3	30.3	-22.4	-15.1	-31.4
1.8	20.4	13.3	30.3	-22.6	-15.3	-31.8
1.9	20.5	13.5	30.4	-22.9	-15.5	-32.1

Temperature (Tj)

Typical 50 °C
Minimum 100 °C
Maximum 0 °C

Vdd/Vddq
Typical 2.5V
Minimum 2.4V
Maximum 2.6V

The above characteristics are specified under best, worst and normal process variation/conditions

30 ohm Driver @ ODT 60 ohm Fix.

1. The typical pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.

2. The 30 ohm@ODT 60 ohm Fix variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.

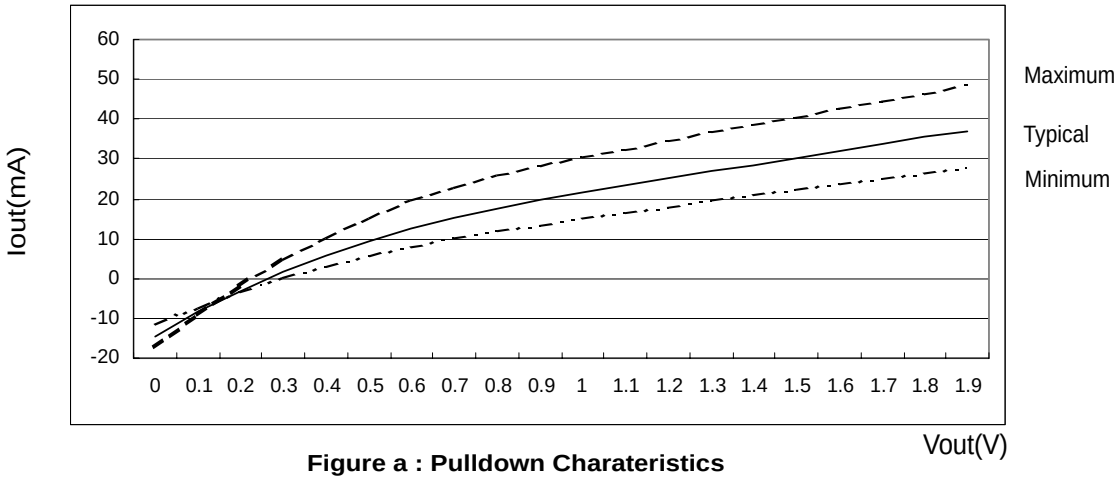


Figure a : Pulldown Charateristics

3. The typical pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.

4. The 30 ohm@ODT 60 ohm Fix variation pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figrue b.

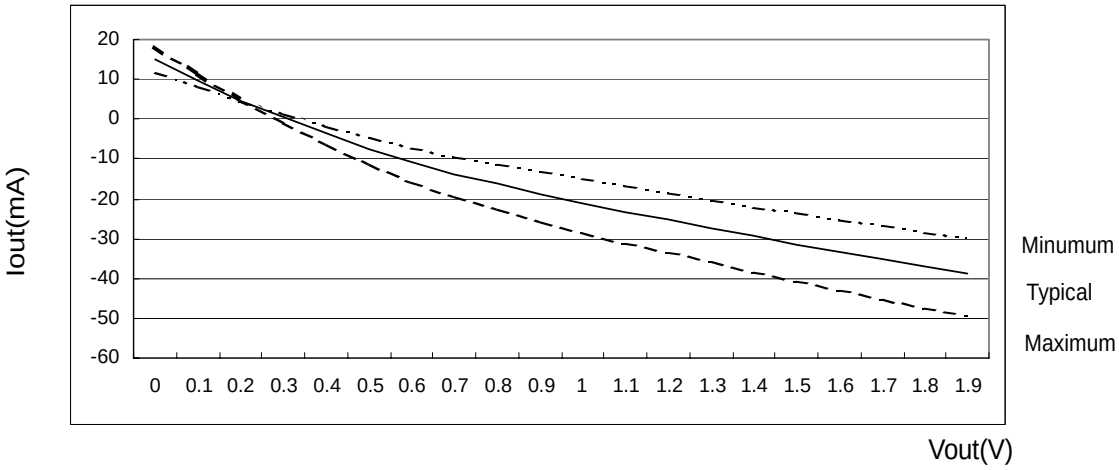


Figure b : PulluP Charateristics

5. The 30 ohm@ODT 60 ohm fix variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to VDDQ/2

6. The 30 ohm@ODT 60 ohm fix variation in the ratio of the nominal pullup to pulldown current should be unity ±10%, for device drain to source voltages from 0 to VDDQ/2

	Pulldown Current (mA)			Pullup Current (mA)		
Voltage (V)	Typical	Minimum	Maximum	Typical	Minimum	Maximum
0.0	-14.4	-11.5	-17.1	14.9	11.9	18.0
0.1	-8.5	-7.1	-9.0	9.7	8.1	11.4
0.2	-3.2	-3.3	-1.8	4.8	4.6	5.1
0.3	1.6	0.2	4.7	0.4	1.3	-0.8
0.4	5.8	3.3	10.4	-3.7	-1.7	-6.2
0.5	9.5	5.9	15.4	-7.4	-4.4	-11.2
0.6	12.7	8.2	19.7	-10.8	-6.9	-15.6
0.7	15.3	10.2	23.1	-13.7	-9.2	-19.4
0.8	17.5	11.9	25.9	-16.4	-11.2	-22.6
0.9	19.6	13.5	28.3	-18.8	-13.2	-25.6
1.0	21.5	15.1	30.5	-21.0	-15.0	-28.3
1.1	23.3	16.6	32.6	-23.2	-16.8	-30.9
1.2	25.1	18.1	34.7	-25.3	-18.5	-33.4
1.3	26.8	19.6	36.7	-27.3	-20.2	-35.8
1.4	28.6	21.0	38.7	-29.4	-21.8	-38.1
1.5	30.3	22.4	40.7	-31.3	-23.5	-40.4
1.6	32.0	23.9	42.7	-33.3	-25.1	-42.7
1.7	33.7	25.3	44.6	-35.2	-26.6	-44.9
1.8	35.4	26.7	46.6	-37.1	-28.2	-47.1
1.9	37.1	28.1	48.5	-39.0	-29.8	-49.3

Temperature (Tj)

Typical	50 °C
Minimum	100 °C
Maximum	0 °C

Vdd/Vddq

Typical	2.5V
Minimum	2.4V
Maximum	2.6V

The above characteristics are specified under best, worst and normal process variation/conditions

30 ohm Driver @ODT 120 ohm Fix.

1. The typical pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.

2. The 30 ohm@ODT 120 ohm Fix variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.

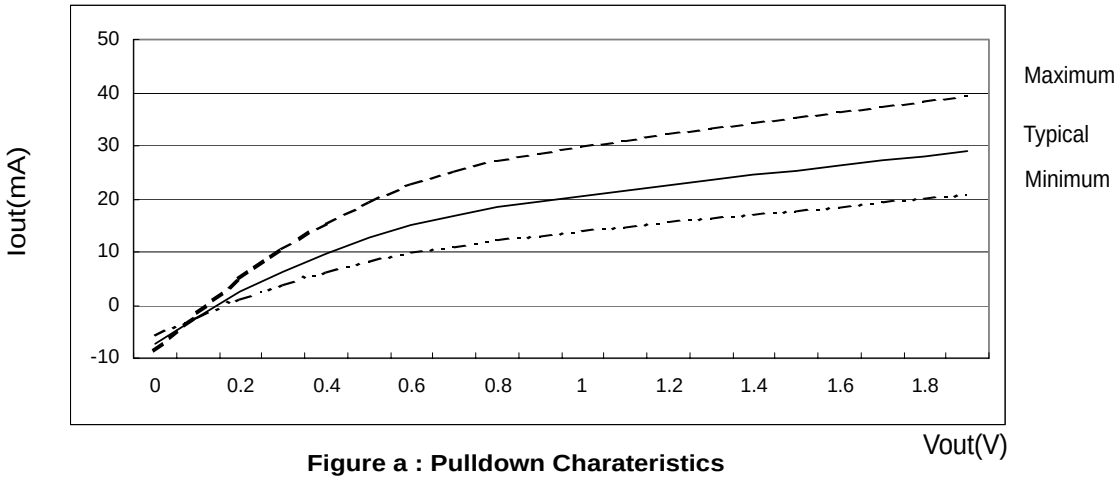


Figure a : Pulldown Charateristics

3. The typical pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.

4. The 30 ohm@ODT 120 ohm Fix variation pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figrue b.

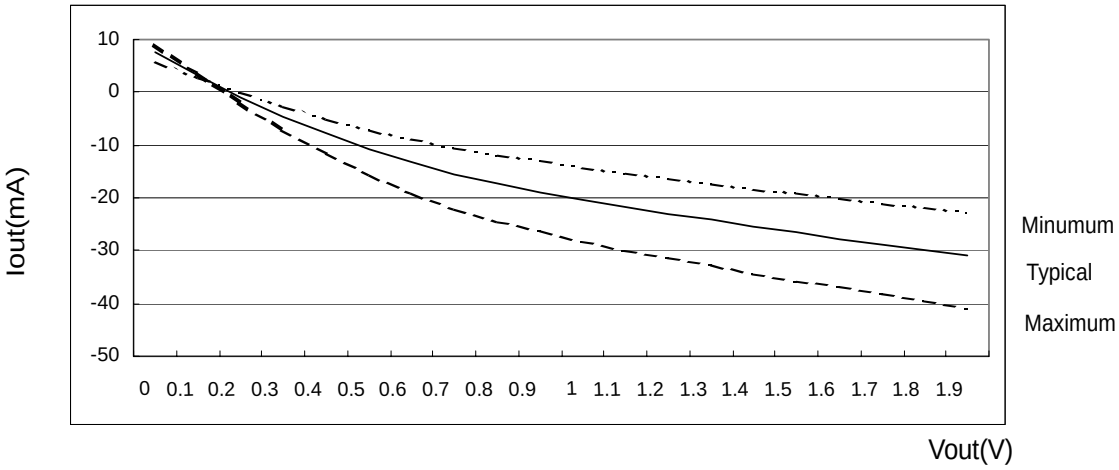


Figure b : PulluP Charateristics

5. The 30 ohm@ODT 120 ohm fix variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to VDDQ/2

6. The 30 ohm@ODT 120 ohm fix variation in the ratio of the nominal pullup to pulldown current should be unity ±10%, for device drain to source voltages from 0 to VDDQ/2

	Pulldown Current (mA)			Pullup Current (mA)		
Voltage (V)	Typical	Minimum	Maximum	Typical	Minimum	Maximum
0.0	-7.2	-5.8	-8.6	7.6	6.1	9.1
0.1	-2.1	-2.1	-1.4	3.1	2.9	3.4
0.2	2.5	1.1	5.0	-0.9	0.1	-2.0
0.3	6.4	3.9	10.6	-4.6	-2.5	-6.9
0.4	9.8	6.3	15.4	-7.9	-4.9	-11.5
0.5	12.7	8.3	19.5	-10.8	-6.9	-15.5
0.6	15.1	9.9	22.8	-13.4	-8.8	-19.1
0.7	16.9	11.2	25.3	-15.5	-10.3	-21.9
0.8	18.3	12.2	27.2	-17.3	-11.7	-24.3
0.9	19.5	13.1	28.7	-18.9	-12.9	-26.3
1.0	20.6	14.0	30.0	-20.4	-14.1	-28.1
1.1	21.6	14.8	31.2	-21.7	-15.2	-29.7
1.2	22.6	15.6	32.3	-23.0	-16.2	-31.3
1.3	23.5	16.4	33.4	-24.2	-17.2	-32.7
1.4	24.5	17.1	34.5	-25.4	-18.1	-34.2
1.5	25.4	17.9	35.5	-26.6	-19.1	-35.5
1.6	26.3	18.6	36.5	-27.7	-20.0	-36.9
1.7	27.1	19.4	37.6	-28.8	-20.9	-38.2
1.8	28.0	20.1	38.6	-29.9	-21.8	-39.5
1.9	28.9	20.9	39.6	-31.0	-22.7	-40.7

Temperature (Tj)

Typical	50 °C
Minimum	100 °C
Maximum	0 °C

Vdd/Vddq

Typical	2.5V
Minimum	2.4V
Maximum	2.6V

The above characteristics are specified under best, worst and normal process variation/conditions

45 ohm @ ODT OFF

1. The typical pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.

2. The 45 ohm@ ODT OFF variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.

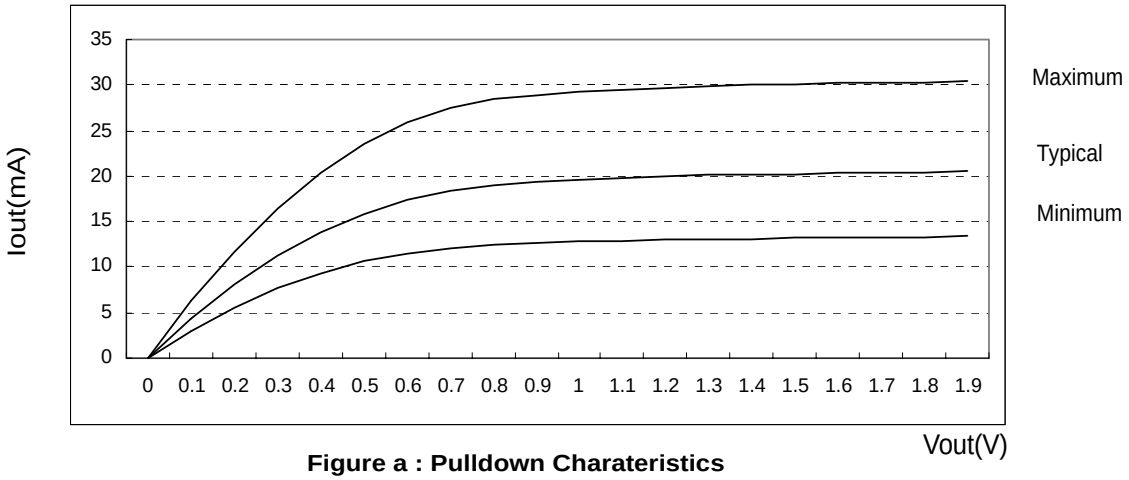


Figure a : Pulldown Charateristics

3. The typical pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.

4. The 45 ohm@ODT OFF variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figrue b.

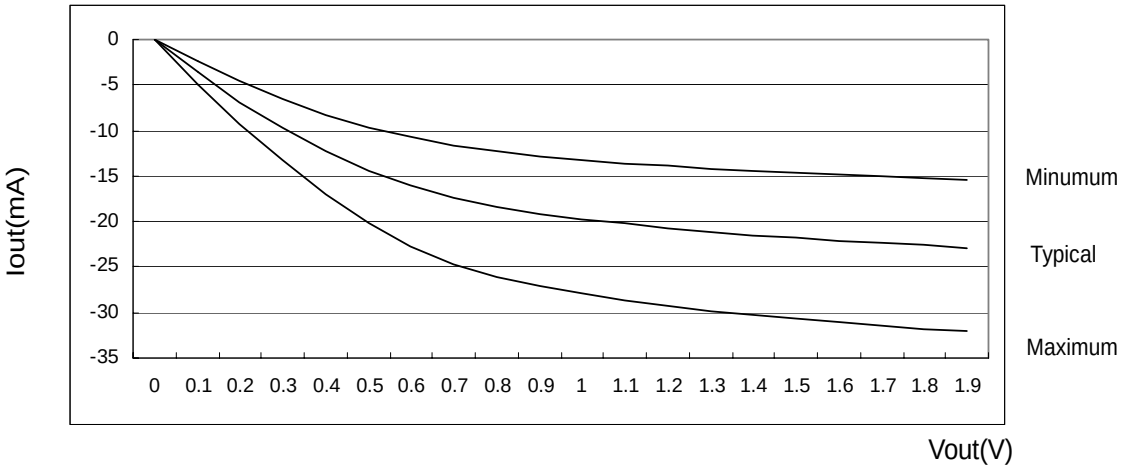


Figure b : PulluP Charateristics

5. The 45 ohm@ODT OFF variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to VDDQ/2

6. The 45 ohm@ODT OFF variation in the ratio of the nominal pullup to pulldown current should be unity ±10%, for device drain to source voltages from 0 to VDDQ/2

	Pulldown Current (mA)			Pullup Current (mA)		
Voltage (V)	Typical	Minimum	Maximum	Typical	Minimum	Maximum
0.0	0.0	0.0	0.0	0.0	0.0	0.0
0.1	2.8	1.9	4.0	-2.2	-1.5	-3.0
0.2	5.2	3.5	7.5	-4.2	-2.8	-5.7
0.3	7.2	4.9	10.5	-6.0	-4.0	-8.2
0.4	8.8	5.9	13.0	-7.5	-5.0	-10.4
0.5	10.1	6.8	15.0	-8.8	-5.9	-12.3
0.6	11.1	7.3	16.5	-9.8	-6.6	-13.9
0.7	11.7	7.7	17.5	-10.6	-7.1	-15.1
0.8	12.1	7.9	18.1	-11.2	-7.5	-15.9
0.9	12.4	8.0	18.4	-11.7	-7.8	-16.6
1.0	12.5	8.1	18.7	-12.1	-8.1	-17.1
1.1	12.6	8.2	18.8	-12.4	-8.3	-17.5
1.2	12.7	8.3	18.9	-12.7	-8.5	-17.9
1.3	12.8	8.3	19.0	-12.9	-8.7	-18.2
1.4	12.8	8.4	19.1	-13.1	-8.8	-18.5
1.5	12.9	8.4	19.2	-13.3	-9.0	-18.8
1.6	12.9	8.4	19.2	-13.5	-9.1	-19.0
1.7	13.0	8.5	19.3	-13.7	-9.2	-19.2
1.8	13.0	8.5	19.3	-13.8	-9.4	-19.4
1.9	13.1	8.6	19.4	-14.0	-9.5	-19.6

Temperature (Tj)

Typical	50 °C
Minimum	100 °C
Maximum	0 °C

Vdd/Vddq

Typical	2.5V
Minimum	2.4V
Maximum	2.6V

The above characteristics are specified under best, worst and normal process variation/conditions

45 ohm Driver @ODT 120 ohm Fix.

1. The typical pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.

2. The 45 ohm@ODT 120 ohm Fix variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.

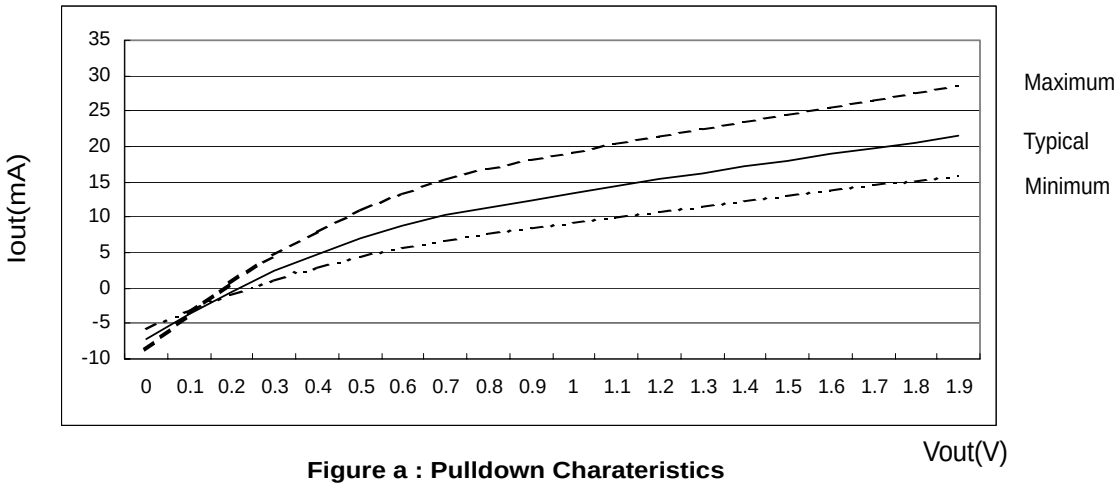


Figure a : Pulldown Charateristics

3. The typical pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.

4. The 45 ohm@ODT 120 ohm Fix variation pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figrue b.

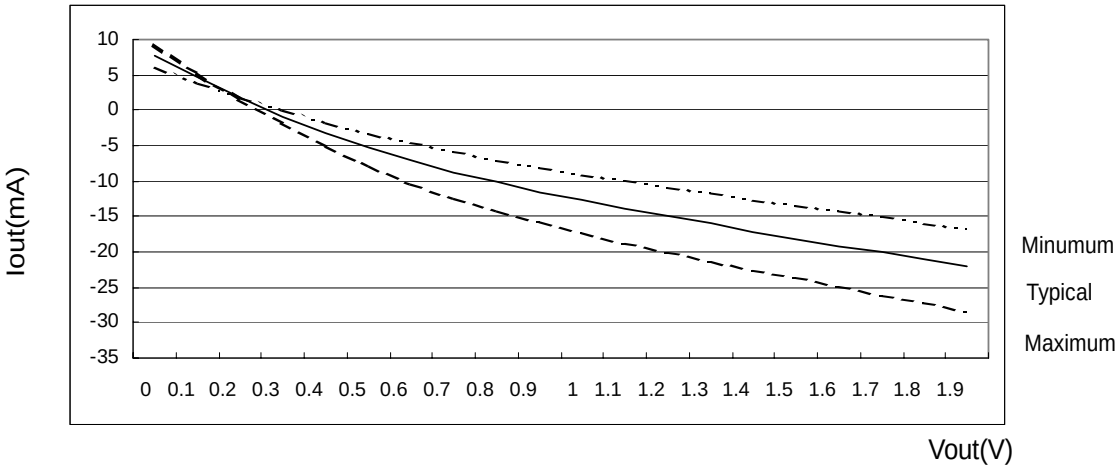


Figure b : PulluP Charateristics

5. The 45 ohm@ODT 120 ohm fix variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to VDDQ/2

6. The 45 ohm@ODT 120 ohm fix variation in the ratio of the nominal pullup to pulldown current should be unity ±10%, for device drain to source voltages from 0 to VDDQ/2

	Pulldown Current (mA)			Pullup Current (mA)		
Voltage (V)	Typical	Minimum	Maximum	Typical	Minimum	Maximum
0.0	-7.3	-5.8	-8.6	7.6	6.1	9.2
0.1	-3.7	-3.2	-3.7	4.6	3.9	5.3
0.2	-0.5	-0.9	0.7	1.8	1.9	1.6
0.3	2.4	1.2	4.6	-0.8	0.0	-1.8
0.4	4.8	2.9	8.0	-3.2	-1.7	-4.9
0.5	7.0	4.4	11.0	-5.3	-3.2	-7.8
0.6	8.8	5.7	13.5	-7.1	-4.6	-10.3
0.7	10.2	6.8	15.4	-8.8	-5.8	-12.4
0.8	11.4	7.7	16.9	-10.2	-7.0	-14.2
0.9	12.5	8.6	18.2	-11.5	-8.0	-15.8
1.0	13.5	9.4	19.3	-12.7	-9.0	-17.3
1.1	14.4	10.7	20.5	-13.9	-9.9	-18.6
1.2	15.4	10.9	21.5	-15.0	-10.8	-19.9
1.3	16.3	11.6	22.6	-16.0	-11.7	-21.2
1.4	17.1	12.4	23.6	-17.1	-12.5	-22.4
1.5	18.0	13.1	24.6	-18.1	-13.4	-23.7
1.6	18.9	13.8	25.6	-19.1	-14.2	-24.8
1.7	19.8	14.6	26.6	-20.1	-15.0	-16.0
1.8	20.6	15.3	27.6	-21.1	-15.8	-27.2
1.9	21.5	16.0	28.6	-22.1	-16.7	-28.3

Temperature (Tj)

Typical	50 °C
Minimum	100 °C
Maximum	0 °C

Vdd/Vddq

Typical	2.5V
Minimum	2.4V
Maximum	2.6V

The above characteristics are specified under best, worst and normal process variation/conditions

60 ohm @ODT OFF

1. The typical pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.

2. The 60 ohm@ODT OFF variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.

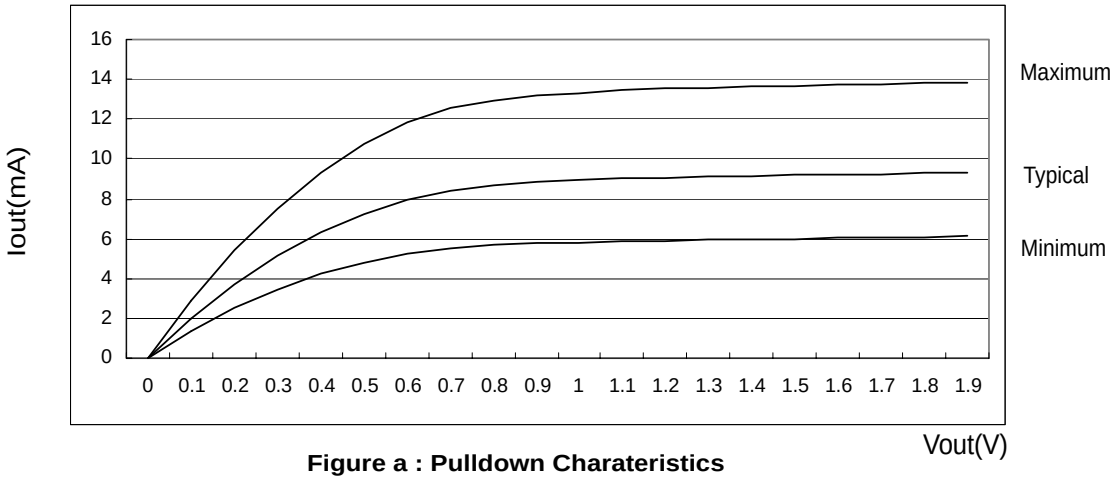


Figure a : Pulldown Charateristics

3. The typical pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.

4. The 60 ohm@ODT OFF variation in drive pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figrue b.

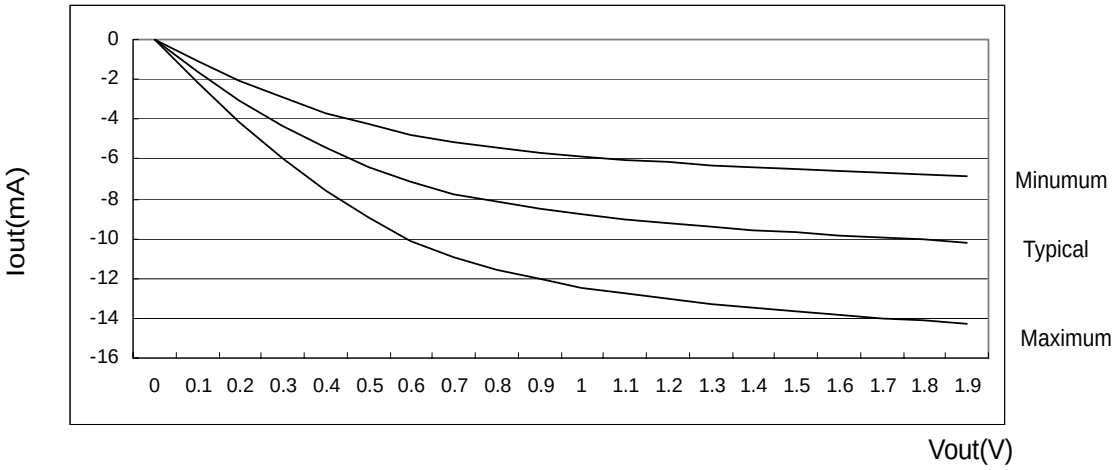


Figure b : PulluP Charateristics

5. The 60 ohm@ODT OFF variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to VDDQ/2

6. The 60 ohm@ODT OFF variation in the ratio of the nominal pullup to pulldown current should be unity ±10%, for device drain to source voltages from 0 to VDDQ/2

	Pulldown Current (mA)			Pullup Current (mA)		
Voltage (V)	Typical	Minimum	Maximum	Typical	Minimum	Maximum
0.0	0.0	0.0	0.0	0.0	0.0	0.0
0.1	2.0	1.4	2.9	-1.6	-1.1	-2.2
0.2	3.7	2.5	5.4	-3.1	-2.1	-4.2
0.3	5.1	3.5	7.5	-4.4	-2.9	-6.0
0.4	6.3	4.2	9.3	-5.5	-3.7	-7.6
0.5	7.3	4.8	10.7	-6.4	-4.3	-9.0
0.6	7.9	5.2	11.8	-7.2	-4.8	-10.1
0.7	8.4	5.5	12.5	-7.7	-5.2	-11.0
0.8	8.7	5.7	12.9	-8.2	-5.5	-11.6
0.9	8.8	5.8	13.2	-8.5	-5.7	-12.1
1.0	8.9	5.8	13.3	-8.8	-5.9	-12.4
1.1	9.0	5.9	13.4	-9.0	-6.0	-12.7
1.2	9.1	5.9	13.5	-9.2	-6.2	-13.0
1.3	9.1	5.9	13.6	-9.4	-6.3	-13.2
1.4	9.2	6.0	13.6	-9.5	-6.4	-13.5
1.5	9.2	6.0	13.7	-9.7	-6.5	-13.6
1.6	9.2	6.0	13.7	-9.8	-6.6	-13.8
1.7	9.3	6.0	13.8	-9.9	-6.7	-14.0
1.8	9.3	6.1	13.8	-10.1	-6.8	-14.1
1.9	9.3	6.2	13.8	-10.2	-6.9	-14.3

Temperature (Tj)

Typical	50 °C
Minimum	100 °C
Maximum	0 °C

Vdd/Vddq

Typical	2.5V
Minimum	2.4V
Maximum	2.6V

The above characteristics are specified under best, worst and normal process variation/conditions

60 ohm Driver @ODT 120 ohm Fix.

1. The typical pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.

2. The 60 ohm@ODT 120 ohm fix variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.

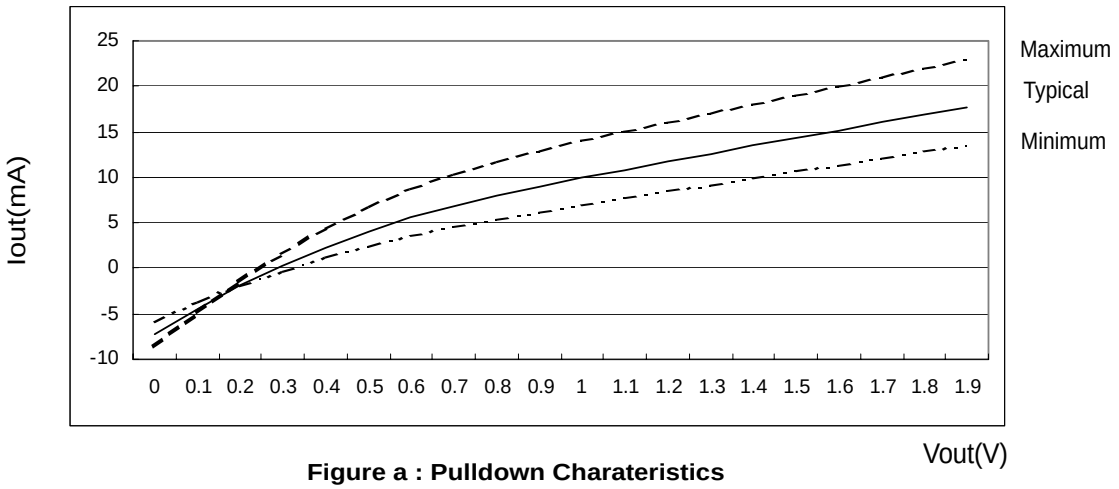


Figure a : Pulldown Charateristics

3. The typical pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.

4. The 60 ohm@ODT 120 ohm fix variation in drive pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figrue b.

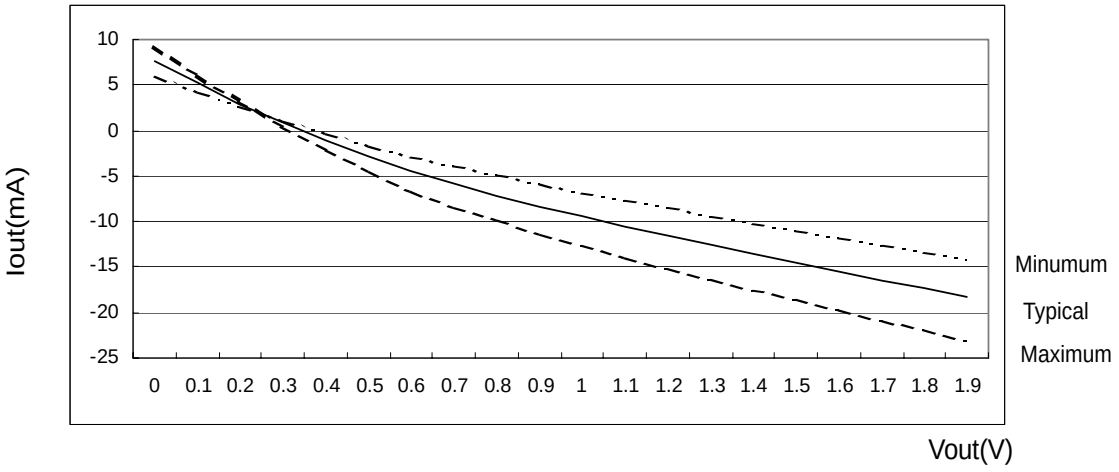


Figure b : PulluP Charateristics

5. The 60 ohm@ODT 120 ohm fix variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to VDDQ/2

6. The 60 ohm@ODT 120 ohm fix variation in the ratio of the nominal pullup to pulldown current should be unity ±10%, for device drain to source voltages from 0 to VDDQ/2

	Pulldown Current (mA)			Pullup Current (mA)		
Voltage (V)	Typical	Minimum	Maximum	Typical	Minimum	Maximum
0.0	-7.3	-5.8	-8.7	7.6	6.1	9.2
0.1	-4.5	-3.7	-4.9	5.2	4.3	6.1
0.2	-2.0	-1.9	-1.4	2.9	2.7	3.2
0.3	0.3	-0.2	1.6	0.8	1.1	0.5
0.4	2.3	1.2	4.3	-1.1	-0.3	-2.1
0.5	4.1	2.5	6.7	-2.9	-1.6	-4.4
0.6	5.6	3.6	8.7	-4.5	-2.8	-6.5
0.7	6.9	4.6	10.4	-5.9	-3.9	-8.3
0.8	8.0	5.5	11.7	-7.1	-4.9	-9.9
0.9	9.0	6.3	12.9	-8.3	-5.9	-11.3
1.0	9.9	7.0	14.0	-9.4	-6.8	-12.6
1.1	10.8	7.8	15.1	-10.5	-7.6	-13.9
1.2	11.7	8.5	16.1	-11.5	-8.5	-15.1
1.3	12.6	9.3	17.1	-12.5	-9.3	-16.3
1.4	13.5	10.0	18.1	-13.5	-10.1	-17.4
1.5	14.2	10.7	19.1	-14.5	-10.9	-18.5
1.6	15.2	11.4	20.1	-15.5	-11.7	-19.7
1.7	16.1	12.1	21.1	-16.4	-12.5	-20.8
1.8	16.9	12.8	22.1	-17.4	-13.3	-21.0
1.9	17.8	13.6	23.1	-18.3	-14.1	-23.0

Temperature (Tj)

Typical	50 °C
Minimum	100 °C
Maximum	0 °C

Vdd/Vddq

Typical	2.5V
Minimum	2.4V
Maximum	2.6V

The above characteristics are specified under best, worst and normal process variation/conditions