S3529B

Programmable High Pass Filter

February 1993

Features

- Cutoff Frequency Selectable in 64 Steps Via Six-Bit
- Control Word
- Cutoff Frequency (f_C) Range of 10Hz to 20kHz,
- 40Hz to 20kHz Via 3.58MHz TV Crystal
- Seventh Order Elliptical Filter
- Passband Ripple: 0.1dB
- Stopband Attenuation: 51dB for $f < .77 f_C$
- Clock Tunable Cutoff Frequency Continuously Variable Via External Clock (Crystal, Resonator, or TTL/CMOS Clock)
- Uncommitted Input and Output Op Amps for Anti-Aliasing and Smoothing Functions
- Low Power CMOS Technology

Typical Applications for the S3528B and S3529B Programmable Filters

Telecommunications

- PBX & Trunk Line Status Monitoring
- Automatic Answering/Forwarding/Billing Systems
- Adaptive Filtering

Remote Control

- Alarm Systems
- Heating Systems
- Acoustic Controllers

Test Equipment/Instrumentation

- Spectrum Analyzers
- Computer Controlled Analog Circuit Testers
- Medical Telemetry Filtering
- ECG Signal Filtering
- Automotive Command Selection and Filtering

Block Diagram

Pin Configuration
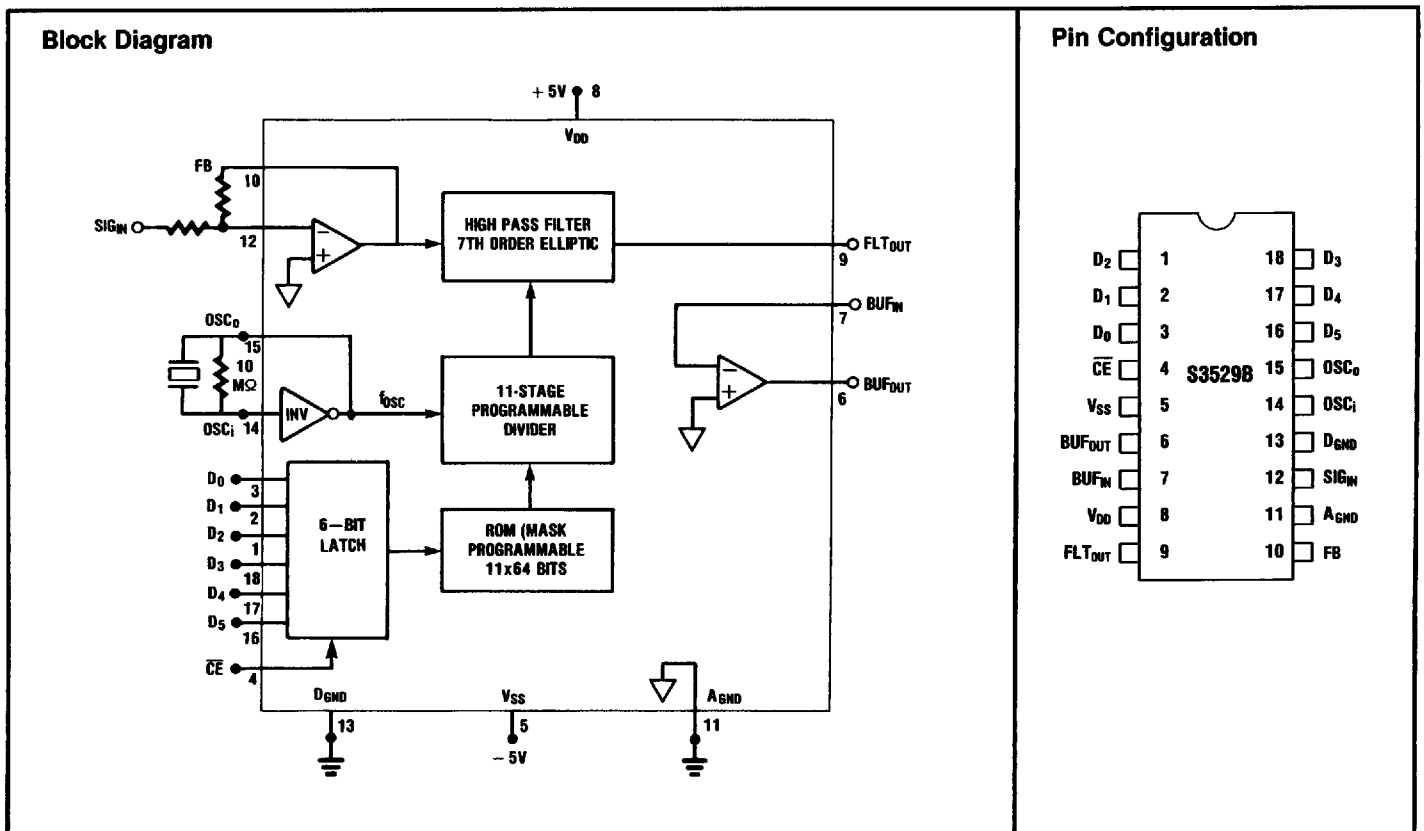
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General Description

The S3529B's CMOS design using switched-capacitor techniques allows easy programming of the filter's cutoff frequency (f_C) in 64 steps via a six-bit control word. For dynamic control of cutoff frequencies, the S3529B can operate as a peripheral to a microprocessor system with the code for the cutoff frequency being latched in from the data bus. When used with the companion low pass filter, the S3528B, a bandpass filter with a variable center frequency is obtained. For special applications the S3529B's internal ROM can be customized to accommodate a specific set of cutoff frequencies from a choice of 2,048 possibilities.

Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$)..+ 15.0V
Operating Temperature..0°C to + 70°C
Storage Temperature.. − 65°C to + 150°C
Input Voltage, All Pins..$V_{SS} - 0.3V \leqslant V_{IN} \leqslant + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to + 70°C, $(V_{DD} - V_{SS}) = 10V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation @10V @13.5V		60 135	110 225	mW mW
R_{IN}	Input Resistance (Pins 1-4, 7, 12, 14, 16-18)	8			MΩ
C_{IN}	Input Capacitance (Pins 1-4, 7, 12, 14, 16-18)			15.0	pF

Digital Electrical Parameters: $V_{DD} = + 5V \pm 10\%$, $V_{SS} = − 5V \pm 10\%$, $T_A = 0°C$ to + 70°C unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	V
V_{IL}	Input Low Voltage	V_{SS}		0.8	V
I_N	Input Leakage Current ($V_{IN} = 0$ to 4VDC)			10	μADC
C_{IN}	Input Capacitance			15	pF

Digital Timing Characteristics

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
t_{CE}	Chip Enable Pulse Width	200	300		ns
t_{AS}	Address Setup Time		300		ns
t_{AH}	Address Hold Time		20		ns
f_{OSC}	Crystal Oscillator Frequency[1]		3.58		MHz
t_{SET}	Settling Time From CE to Stable f_C($f_C = 3200$)[2]		6		ms

Notes:

1. The tables are based on the common 3.58MHz color burst TV crystal.

2. $t_{SET} = \dfrac{10}{f_C} + 3msec$

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General Analog Signal Parameters: $(V_{DD} - V_{SS}) = 10V$, $T_A = 0°C$ to $+70°C$, $f_{OSC} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Pass Band Gain at 2.2 f_C	-0.5	0	0.5	dB
V_{MAX}	Reference Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level ($+3dBm0$)		2.1		VRMS
R_L	Load Resistance (FLT_{OUT}, Pin 9)	10			kΩ
R_L	Load Resistance (BUF_{OUT}, Pin 6)	600			Ω
V_{OUT}	Output Signal Level into R_L for FLT_{OUT}, BUF_{OUT}	2.0	2.1		VRMS
T_{HD}	Total Harmonic Distortion: Input code 22, Frequency = 2kHz; Bandlimited to $f_{clk}/2$		.15		%
WBN	Wideband Noise: Input code 22, Bandlimited to 15kHz		.25		mVRMS
V_{OS}	Buffer Output (Pin 6) Offset Voltage		± 10		mV
V_{OES}	Filter Output (Pin 9) Offset Voltage		± 80		mV

Filter Performance Specifications: High Pass Filter Characteristics $(f_{OSC} = 3.58MHz)$ $(V_{DD} - V_{SS}) = 10V$, $T_A = 0°C$ to $+70°C$

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
	Passband ripple (Ref. 2.2 f_C) $f_C \leq f < 7f_C$		-0.5	± 0.05	0.5	dB
Filter Response: $f_C = 1005Hz$						
	(f_C)	1005Hz	-0.5	± 0.1	0.5	dB
	($0.96 f_C$)	960	-5	-3.0	-1	db
	($0.768 f_C$)	772		-53	-43	db
	($.754 f_C$)	758		-85	-43	db
	($.614 f_C$)	617		-70	-43	db
	Stopband	$f < .768 f_C$		< -53		db
DR	Dynamic Range (V_{FS} to WBN)			78		dB

Pin Description

Pin Name	Pin#	Function
V_{DD}	8	Positive supply voltage pin. Normally $+5$ volts $\pm 10\%$.
V_{SS}	5	Negative supply voltage pin. Normally -5 volts $\pm 10\%$.
A_{GND}	11	Analog ground reference point for analog input signals. Normally connected to ground.
D_{GND}	13	Digital ground reference point for digital input signals. Normally connected to ground.
D_0	3	The input bus to allow selection of the desired cutoff frequency. The value of the word presented to these pins selects the cutoff frequency. It is latched in on the rising edge of $\overline{CE}$. These are high impedance CMOS inputs and can be bridged directly across a microprocessor data bus.
D_1	2	
D_2	1	
D_3	18	
D_4	17	
D_5	16	

Pin Description: (continued)

Pin Name	Pin#	Function
$\overline{CE}$	4	Chip Enable: This pin has 3 states. When $\overline{CE}$ is at V_{DD} the data in the latch is presented to the ROM and the inputs have no effect. When $\overline{CE}$ is at ground the data presented on the inputs is read into the latch but the previous data is still in the ROM. Returning $\overline{CE}$ to V_{DD} presents the new data to the ROM and f_{cutoff} changes. When $\overline{CE}$ is at V_{SS} the inputs go directly to the ROM, changing f_{cutoff} immediately. The configuration for a fixed filter is: $\overline{CE}$ at V_{SS} and the D_0 through D_5 are tied to V_{DD} or V_{SS}/D_{GND} depending on the desired f_{cutoff}.
OSC_i	14	Oscillator In and Oscillator Out. Placing a crystal and a $10M\Omega$ resistor across these pins creates the time base
OSC_0	15	oscillator. An inexpensive choice is to use the 3.58MHz TV crystal.
SIG_{IN}	12	Signal Input. This is the inverting input of the input op amp. The non-inverting input is internally connected to Analog Ground.
FB	10	Feedback. This is the feedback point for the input op amp. The feedback resistor should be $\geq 10k\Omega$ for proper operation.
FLT_{OUT}	9	The high impedance output of the high pass filter. Load should be $10K\Omega$.
BUF_{IN}	7	The inverting input of the buffer amplifier.
BUF_{OUT}	6	The buffer amplifier output to drive low impedance loads. Load should be $\geq 600\Omega$.

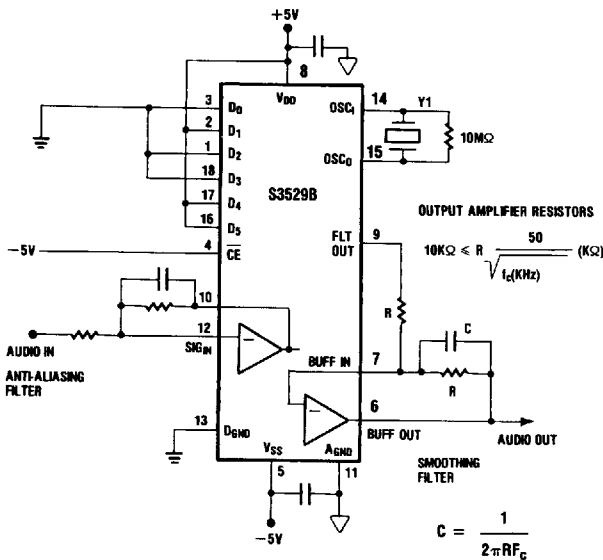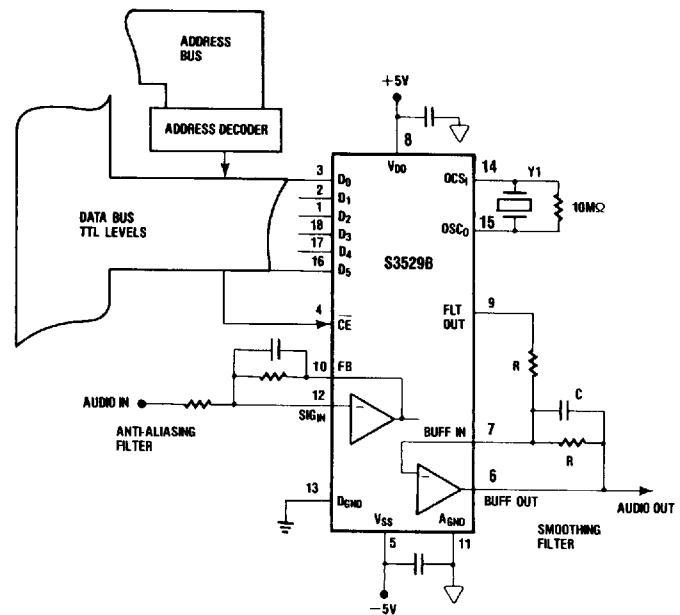### Example of Circuit Connection for S3529B

Figure 1. Stand Alone Operation

Figure 2. Microprocessor Interface

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AMI STANDARD PRODUCTS
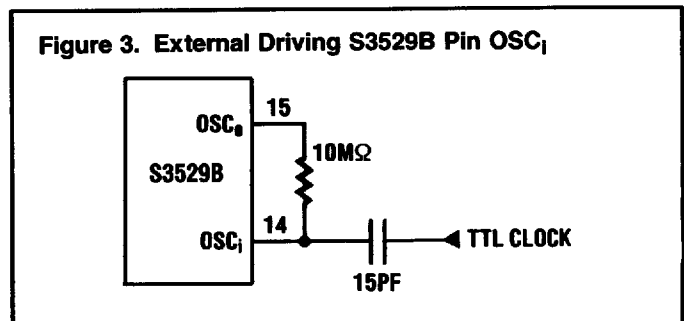
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Table 1. Standard Frequency Table: Programmable Filter S3529B, f_{clock} = 3.58MHz

Voice Band Input D_5-D_0 (HEX)	Divider Ratio	f_c Actual (Hz)	Additional Points Input Code D_5-D_0 (HEX)	Divider Ratio	f_c Actual (Hz)
00	2048	40	0A	188	433
01	895	91	0B	358	227
02	447	182	0C	90	904
03	298	273	0D	87	935
04	224	363	0E	85	957
05	179	455	0F	78	1043
06	149	546	1A	61	1334
07	128	635	1B	58	1402
08	112	726	1C	52	1565
09	99	822	1D	46	1768
10	89	914	1E	44	1849
11	81	1005	1F	40	2034
12	74	1099	2A	38	2136
13	69	1179	2B	35	2325
14	64	1271	2C	22	3697
15	60	1355	2D	20	4067
16	56	1453	2E	18	4519
17	53	1535	2F	16	5085
18	50	1627	35	15	5423
19	47	1731	38	14	5811
20	45	1808	3A	12	6779
21	43	1892	3B	10	8135
22	41	1985	3C	9	9039
23	39	2086	3D	6	13559
24	37	2198	3E	5	16270
25	36	2260	3F	4	20338
26	34	2392			
27	33	2465			
28	32	2543			
29	31	2625			
30	30	2712			
31	29	2805			
32	28	2905			
33	27	3013			
34	26	3129			
36	25	3254			
37	24	3389			
39	23	3537			

$$f_{CUTOFF} = \frac{f_{clock}}{44 \text{ (Divider Ratio)}}$$

Alternate Clock Configurations

If 3.58MHz is already available in the system it can be applied directly as a logic level to the OSC$_{IN}$ (pin 14). (Max. zero~30% V_{DD}, min. one~70% V_{SS}). Waveforms not satisfying these logic levels can be capacitively coupled to OSC$_{IN}$ as long as the 10MΩ feedback resistor is installed as shown in Figure 3.
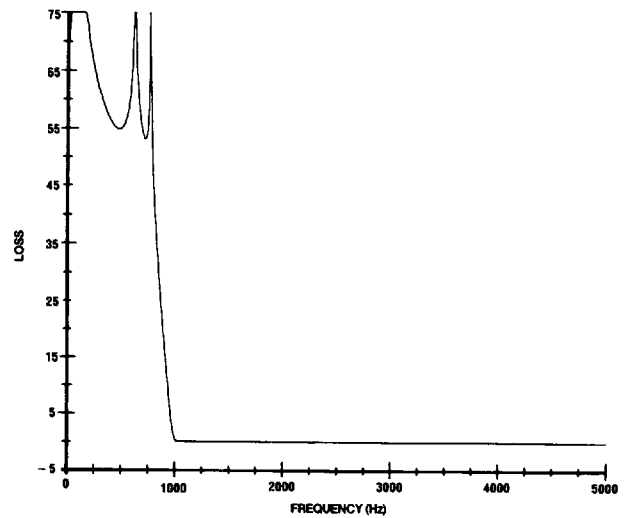

Figure 3. External Driving S3529B Pin OSC$_i$

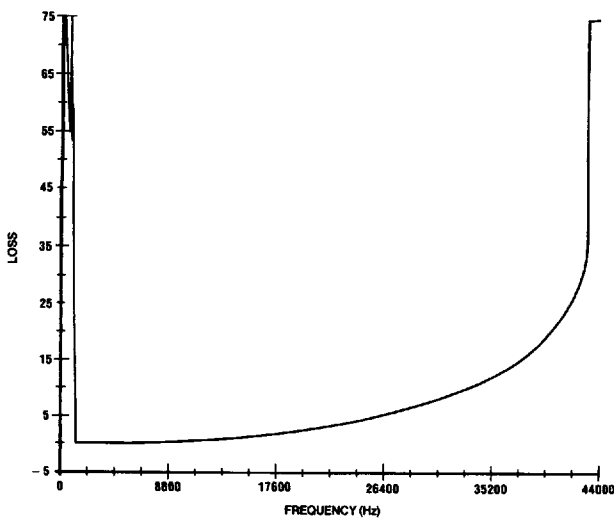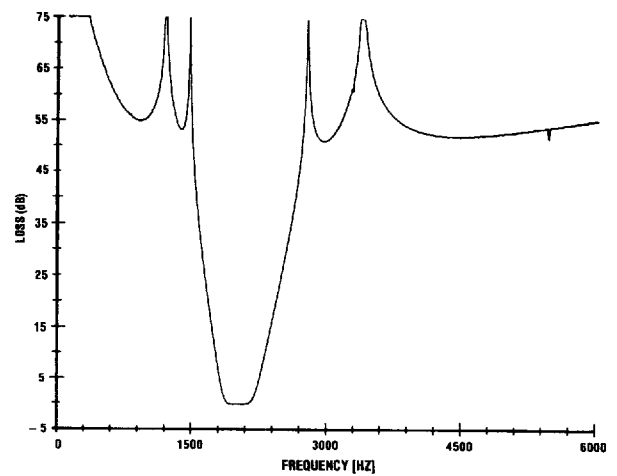**Figure 4. Passband Detail, Control = 110010, f_c = 1005Hz**
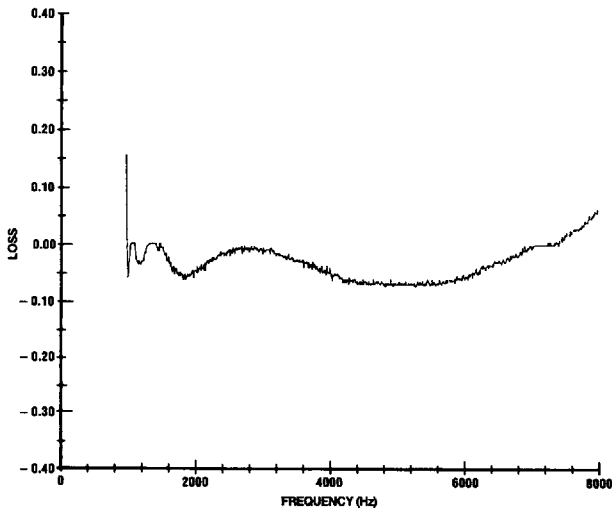
Figure 5. Loss Curve, Control = 110010, f_c = 1005Hz

Figure 6. Loss Response, DC to Clock Detail, Control = 110010, f_c = 1005Hz

Figure 7. Cascaded S3528B and S3529B, Control = 100001 Bandpass Configuration—10% Bandwidth

■ 4055916 0014410 468 ■

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**Figure 8. S3528B and S3529B in Parallel,
Notch Configuration—Narrow Bandwidth**
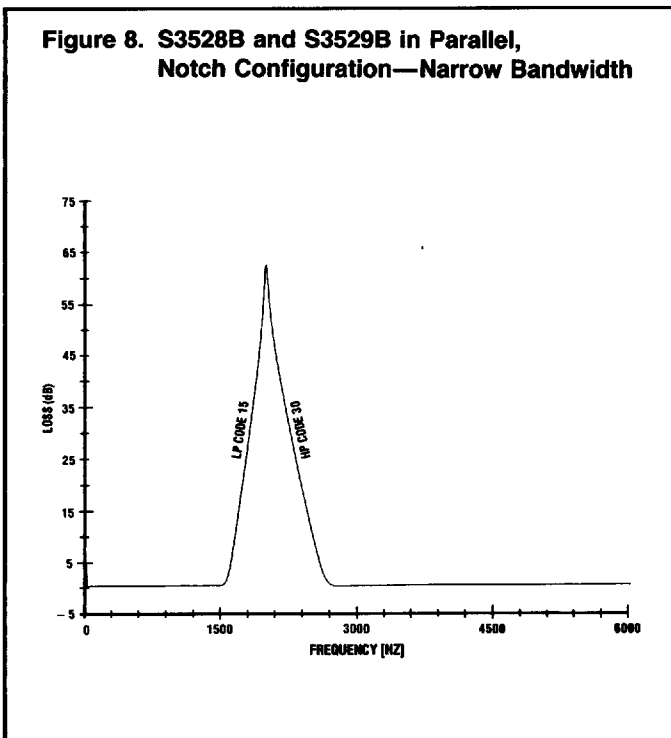
**Figure 9. S3528B and S3529B in Parallel,
Notch Configuration—Wide Bandwidth**
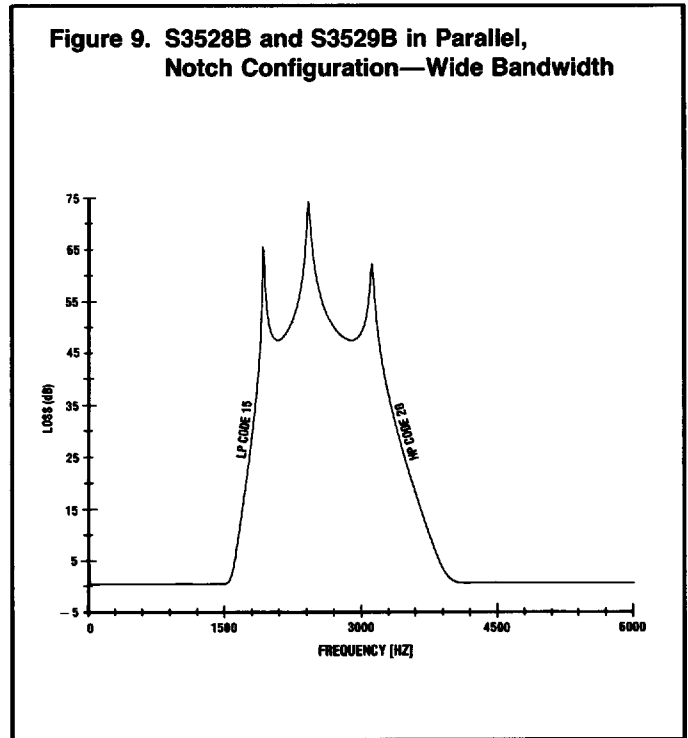
Applications Information

The S3529B High Pass Filter has a very sharp 50dB drop off at f_C. The Passband Ripple is less than 0.5dB. Note that unlike passive element filter, attenuation increases for sampled-data filters at the higher frequencies due to the sample and hold effect. ($f_{CLOCK} = 44xf_{CUTOFF}$).

The S3529B High Pass Filter and the S3528B Low Pass Filter can be used together to make either Band Pass or Band Reject filters. The control code selection determines the bandwidth of the resulting filter.

Figure 10. Bandpass Application: General Case Configuration
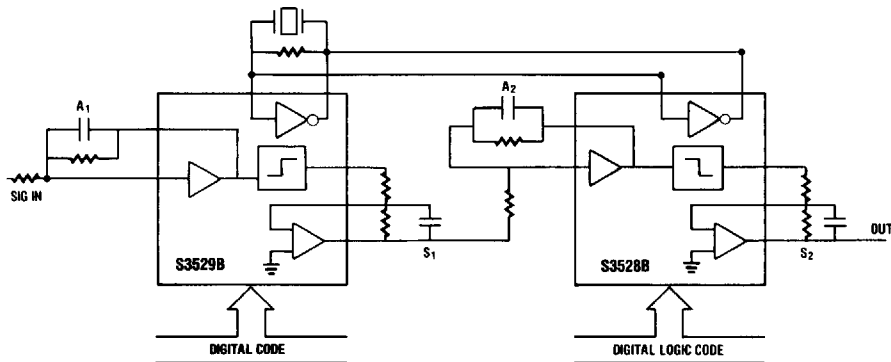
Note:

— Anti-aliasing and smoothing filters on both chips A1, A2, S1, S2

— Lowpass after highpass to remove higher harmonics, unless cosine input filter of lowpass needed to clean noisy input signal

— For wider band width two different oscillators can be used.

— If filter clock (^{f}clock) for lowpass is an integer multiple of the ^{f}clock for highpass, then S1 and A2 may be removed without causing beat frequencies.

• For same digital logic code
  N = multiple of clock#1 to clock#2
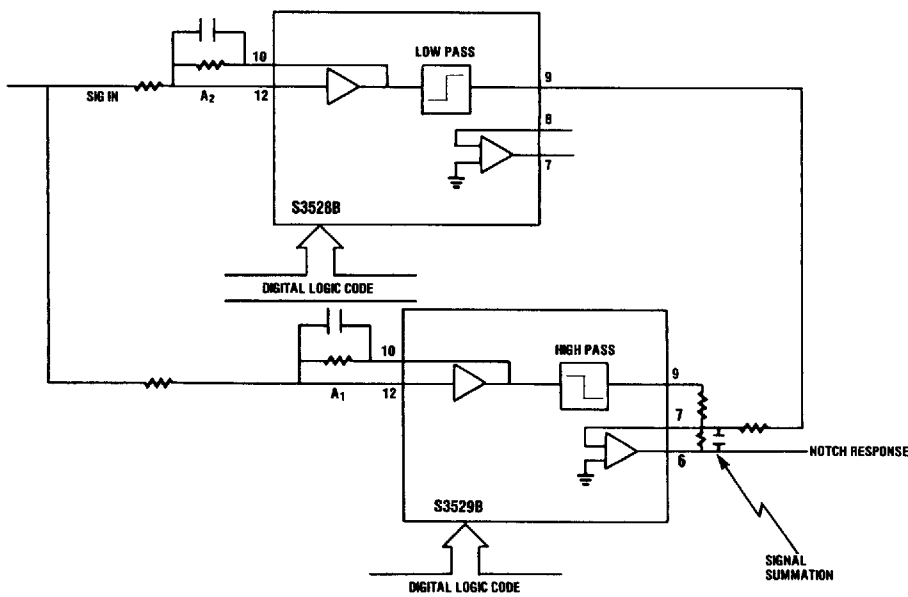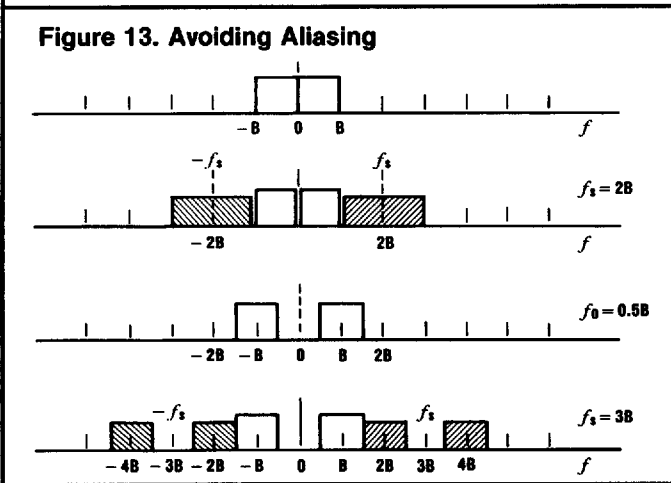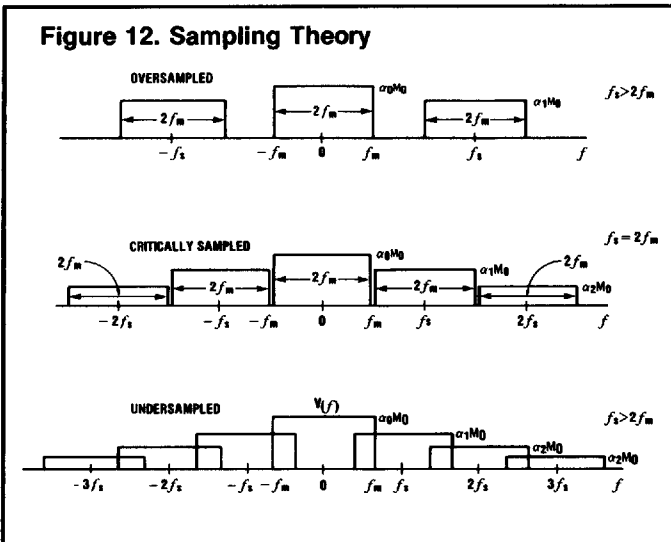
$$f_{cL} = \frac{.9 f_{cu}}{N}$$
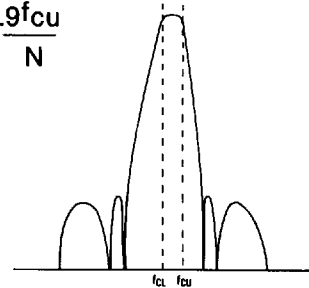
Figure 11. Notch Applications: General Case Configuration

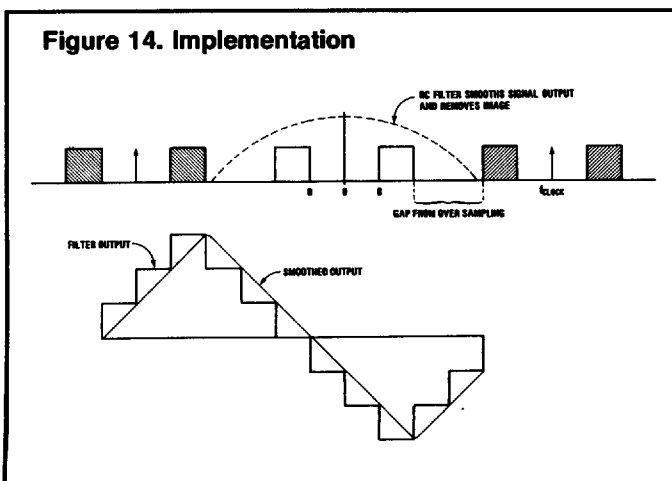## Programmable High Pass Filter

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Figure 12. Sampling Theory

Figure 13. Avoiding Aliasing

Note that critical sampling avoids aliasing, but in the above example no real life filter can separate the message from the image. One must oversample in real life.

Figure 14. Implementation

Applications Information

Anti-Aliasing

fs = sampling frequency
fm = frequency bandwidth of message

In planning an application the fundamentals of sampling devices must be considered.

• Make certain the harmonic image does not fold into the desired pass band. i.e, Oversample.

• Bandlimit the input so that the input frequencies, noise, and tails will not come too close to the clock and be folded back into the pass band.

• Bandlimit the output so that the image is sufficiently attenuated and the switched capacitor output is smoothed. i.e., kill the higher order terms in the Fourier Series.

• For dynamic operation check for aliasing at each cutoff frequency.