



AUDIO/VIDEO SWITCH MATRIX

- I²C BUS CONTROL
- STANDBY MODE

VIDEO SECTION

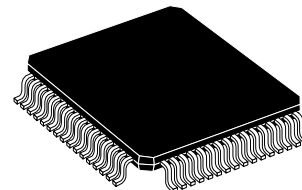
- 5 CVBS INPUTS, 4 CVBS OUTPUTS (ONE WITH SELECTABLE CHROMA TRAP FILTER)
- 5 Y/C INPUTS, 3 Y/C OUTPUTS
- 6dB GAIN ON ALL CVBS/Y AND C OUTPUTS
- 1 Y/C ADDER
- 2 RGB/FB INPUTS, 1 RGB/FB OUTPUT WITH 6dB ADJUSTABLE GAIN
- VIDEO MUTING ON ALL THE OUTPUTS
- 3 SLOW BLANKING INPUTS/OUTPUTS
- SYNC BOTTOM CLAMP ON ALL CVBS/Y AND RGB INPUTS, AVERAGE ON C INPUTS
- BANDWIDTH : 15MHz
- CROSSTALK : 60dB Typ.

AUDIO SECTION

- 5 STEREO INPUTS, 4 STEREO OUTPUTS (TWO WITH LEVEL ADJUSTMENT)
- MONO SOUND OUTPUT
- STEREO TO MONO CAPABILITY ON ALL SCARTS
- AUDIO MUTING ON ALL THE OUTPUTS

DESCRIPTION

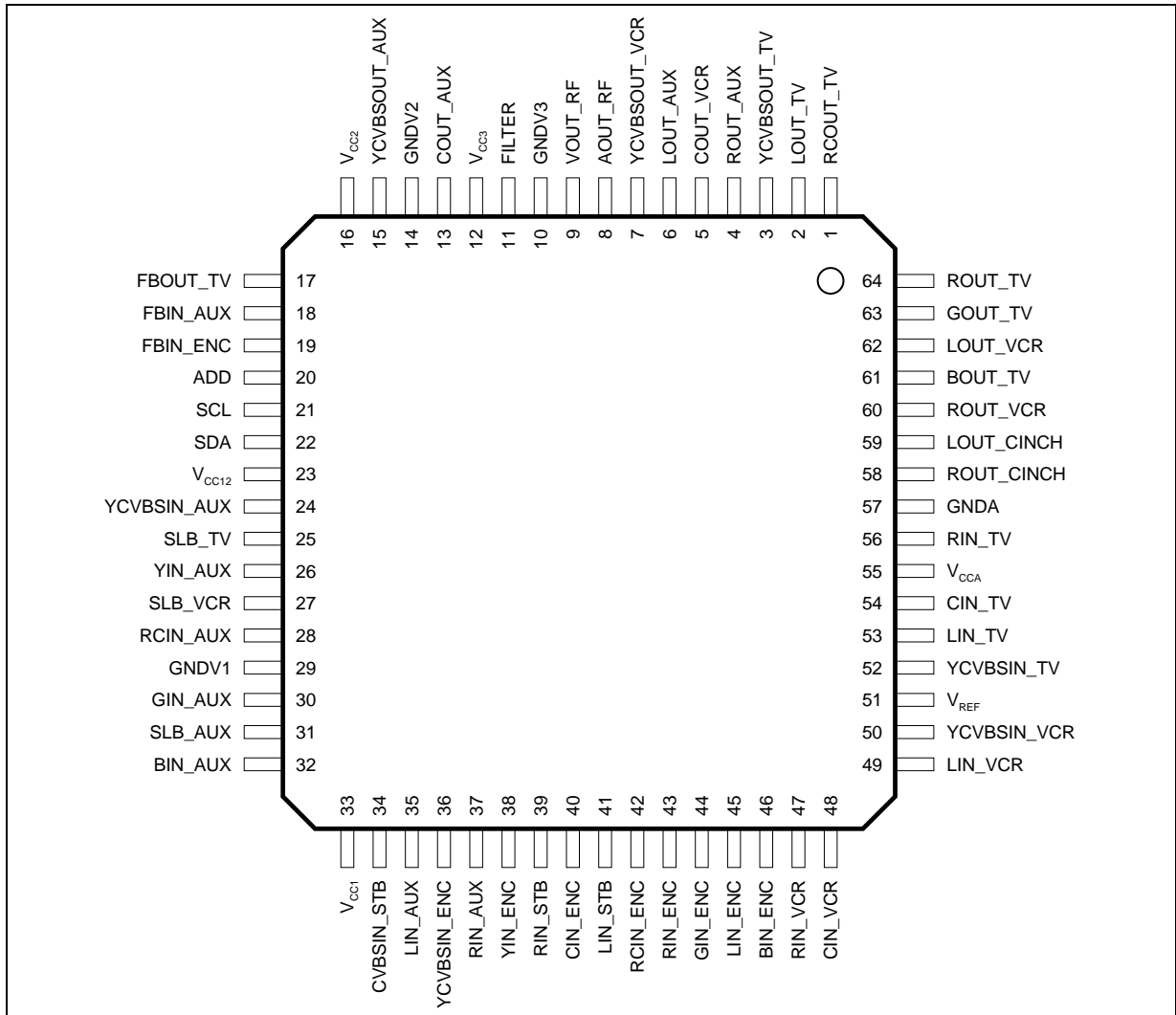
The STV6410A is a highly integrated I²C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. It provides all the audio and video routings required in a full three scart set-top box design. It is also fully pin compatible with STV6411A, the two scart version.



TQFP64 (10 x 10 x 1.4mm)
(Full Plastic Quad Flat Pack)

ORDER CODE : STV6410AD

PIN CONNECTIONS



6410A-01.EPS

PIN LIST

Pin Number	Symbol	Description
1	RCOUT_TV	Red/chroma Output, to TV Scart
2	LOUT_TV	Audio Left Output, to TV Scart
3	YCVBSOUT_TV	Y/CVBS Output, to TV scart
4	ROUT_AUX	Audio Right Output, to AUX Scart
5	COUT_VCR	Chroma Output, to VCR Scart
6	LOUT_AUX	Audio Left Output, to AUX Scart
7	YCVBSOUT_VCR	Y/CVBS Output, to VCR Scart
8	AOUT_RF	Audio (L+R) Output to RF Modulator
9	VOUT_RF	Video (CVBS) Output to RF Modulator
10	GNDV3	Video Switches Ground 3
11	FILTER	Chroma Trap Filter
12	V _{cc3}	Video Switches Supply 3 (8V)
13	COUT_AUX	Chroma Output, to AUX Scart
14	GNDV2	Video Switches Ground 2
15	YCVBSOUT_AUX	Y/CVBS Output, to AUX Scart

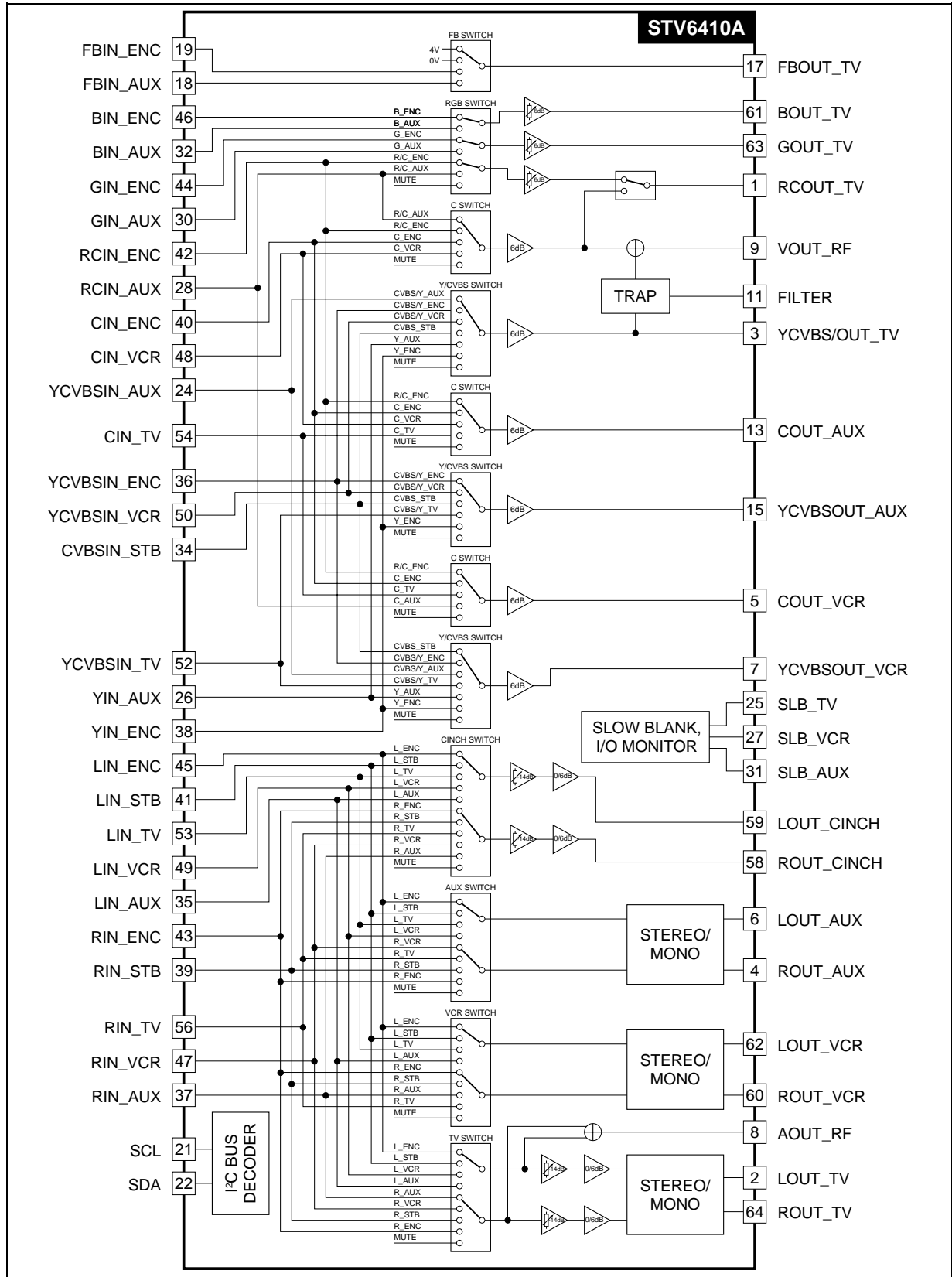
6410A-01.TBL

PIN LIST (continued)

Pin Number	Symbol	Description
16	V _{CCV2}	Video Switches Supply 2 (8V)
17	FBOUT_TV	Fast Blanking Output, to TV Scart
18	FBIN_AUX	Fast Blanking Input, from AUX Scart
19	FBIN_ENC	Fast Blanking Input, from Encoder
20	ADD	I ² C Bus IC Address Programmation
21	SCL	I ² C Bus Clock
22	SDA	I ² C Bus Data
23	V _{CC12}	Slow Blanking Power Supply (12V)
24	YCVBSIN_AUX	Y/CVBS Input from AUX Scart
25	SLB_TV	Slow Blanking Input/Output from TV
26	YIN_AUX	Y Input, from AUX Scart
27	SLB_VCR	Slow Blanking Input/Output from VCR
28	RCIN_AUX	Red/Chroma Input, from AUX Scart
29	GNDV1	Video Switches Ground 1
30	GIN_AUX	Green Input, from AUX Scart
31	SLB_AUX	Slow Blanking Input/Output from AUX
32	BIN_AUX	Blue Input, from AUX Scart
33	V _{CCV1}	Video Switches Supply 1 (8V)
34	CVBSIN_STB	CVBS Input from STB
35	LIN_AUX	Audio Left Input, from AUX Scart
36	YCVBSIN_ENC	Y/CVBS Input from Encoder
37	RIN_AUX	Audio Right Input, from AUX Scart
38	YIN_ENC	Y Input, from Encoder
39	RIN_STB	Audio Right Input, from STB
40	CIN_ENC	Chroma Input, from Encoder
41	LIN_STB	Audio Left Input, from STB
42	RCIN_ENC	Red/Chroma Input, from Encoder
43	RIN_ENC	Audio Right Input, from Encoder
44	GIN_ENC	Green Input, from Encoder
45	LIN_ENC	Audio Left Input, from Encoder
46	BIN_ENC	Blue Input, from Encoder
47	RIN_VCR	Audio Right Input, from VCR Scart
48	CIN_VCR	Chroma Input, from VCR Scart
49	LIN_VCR	Audio Left Input, from VCR
50	YCVBSIN_VCR	Y/CVBS Input from VCR Scart
51	V _{REF}	Voltage Reference Decoupling
52	YCVBSIN_TV	Y/CVBS Input, from TV Scart
53	LIN_TV	Audio Left Input, from TV Scart
54	CIN_TV	Chroma Input, from TV Scart
55	V _{CCA}	Audio Switches Supply (8V)
56	RIN_TV	Audio right input, from TV Scart
57	GND A	Audio Switches Ground
58	ROUT_CINCH	Audio Right Output, to CINCH
59	LOUT_CINCH	Audio Left Output, to CINCH
60	ROUT_VCR	Audio Right Output, to VCR sCart
61	BOUT_TV	Blue Output, to TV Scart
62	LOUT_VCR	Audio Left Output, to VCR Scart
63	GOUT_TV	Green Output, to TV Scart
64	ROUT_TV	Audio Right Output, to TV Scart

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
AV_{CC}, VV_{CC}	Supply voltage for Audio and Video Sections	10	V
V_I	Voltage at pin i to GND. Except SDA, SCL at 5.5V max	0, V_{CC}	V
V_{CC12}	Supply Voltage for Slow Blanking Sections	13.2	V
V_{SLBK}	Voltage at slow blanking pins to GND	0, V_{CC12}	V
VESD	Maximum ESD Voltage allowed (100pF capacitor discharged through 1.5k Ω serial resistor - Human Body Model)	± 4	kV
T_{oper}	Operating Ambient Temperature	0, +70	$^{\circ}C$
T_{stg}	Storage Temperature	-20, +150	$^{\circ}C$

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THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	Max. 68	$^{\circ}C/W$

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ELECTRICAL CHARACTERISTICS

$T_{amb} = 25^{\circ}C$, $AV_{CC} = VV_{CC} = 8V$, $V_{CC12} = 12V$, $R_{LOUTA} = 10k\Omega$, $R_{GA} = 600\Omega$, $R_{GV} = 50\Omega$, $R_{LOUTV} = 4.7k\Omega$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AV_{CC}	Audio Operating Supply Voltage		7.5	8	8.5	V
VV_{CC}	Video Operating Supply Voltage		7.5	8	8.5	V
V_{CC12}	Slow Blanking Control Supply Voltage		11.2	12	12.8	V
ACTIVE (all channels ON)						
I_{CCA}	Audio Supply Current	$AV_{CC} = 8V$, no input signal		10	15	mA
I_{CCV}	Video Supply Current ($I_{CCV1} + I_{CCV2} + I_{CCV3}$)	$VV_{CC} = 8V$, no input signal		65	80	mA
I_{CC12}	12V Supply Current	$V_{CC12} = 12V$ SIBlk input mode SIBlk output mode, no load		0 2.0	2 3	μA mA
STANDBY (all channels OFF)						
I_{CCAstd}	Audio Supply Current in stand by mode	$AV_{CC} = 8V$		1.2		mA
I_{CCVstd}	Video Supply Current in stand by mode ($I_{CCV1} + I_{CCV2} + I_{CCV3}$)	$VV_{CC} = 8V$		9		mA

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ELECTRICAL CHARACTERISTICS (continued)

$T_{amb} = 25^{\circ}\text{C}$, $AV_{CC} = V_{VCC} = 8\text{V}$, $V_{CC12} = 12\text{V}$, $R_{LOUTA} = 10\text{k}\Omega$, $R_{GA} = 600\Omega$, $R_{GV} = 50\Omega$, $R_{LOUTV} = 4.7\text{k}\Omega$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AUDIO SECTION						
SVR100	Supply Voltage Rejection	$V_{RIPPLE} = 500\text{mV}_{RMS}$ at $f = 100\text{Hz}$, Gain = 0dB, V_{REF} filter cap = $47\mu\text{F}$ V_{REF} filter cap = $220\mu\text{F}$	60	72 82		dB dB
SVR1K	Supply Voltage Rejection	$V_{RIPPLE} = 500\text{mV}_{RMS}$ at $f = 1\text{kHz}$, Gain = 0dB	70	80		dB
V_{INDC}	Input DC Level	$AV_{CC} = 8\text{V}$		$V_{CC}/2$		V
V_{INAC}	Input signal amplitude				2	V_{RMS}
R_{IN}	Input Resistance		45	55		$\text{k}\Omega$
$R_{INmatch}$	Input resistance matching			± 1	± 10	%
F_{range}	Bandwidth	-3dB, $0.5V_{RMS}$, $R_L = 10\text{k}\Omega$, Gain = 0dB	50			kHz
Flatness	Spread of gain in audio band	$0.5V_{RMS}$, 20Hz to 20kHz, Gain = 0dB			0.5	dB
C_s	Channel Separation (from audio inputs) Between L & R of TV outputs	$V_{IN} = 0.5V_{RMS}$, $f = 1\text{kHz}$, on one input, $R_L = 10\text{k}\Omega$, Gain = 0dB	80 70	90 74		dB dB
C_i	Channel Isolation from video inputs	$V_{IN} = 1 V_{PP}$, $f = 15\text{kHz}$, on one input, $R_L = 10\text{k}\Omega$, Gain = 0dB	70	85		dB
V_{OUT}	Output DC Level	$AV_{CC} = 8\text{V}$		$V_{CC}/2$		V
V_{OFF}	DC Offset change	Switching between inputs		1	± 15	mV
R_{OUT}	Output Resistance			60		Ω
eNI	Equivalent Input Voltage Noise	BW = 20Hz, 20kHz, Gain = 0dB		5		μV
G0	0dB Gain	$0.5V_{RMS}$, $R_L = 10\text{k}\Omega$, Gain = 0dB	-0.5		+0.5	dB
G_{STEP}	Step of Gain	-14dB to +6dB	1.75	2	2.25	dB
G_{MATCH1}	Gain matching between different inputs on one output	$V_{IN} = 0.5V_{RMS}$, 1kHz, Gain = 0dB	-0.5		0.5	dB
G_{MATCH2}	Gain matching between Left/Right outputs of one input channel	$V_{IN} = 0.5V_{RMS}$, 1kHz, Gain = 0dB	-0.5		0.5	dB
THD	Total Harmonic Distorsion	1kHz, LPF @ 80kHz $V_{IN} = V_{OUT} = 0.5V_{RMS}$ $V_{IN} = V_{OUT} = 2V_{RMS}$		0.002 0.003	0.05	% %
V_{CL}	Output clipping Level	THD = 0.2%, 1kHz	2.1	2.25		V_{RMS}
R_L	Output Load Resistance	$V_{IN} = 1V_{RMS}$, THD = 0.3%, Gain = 0dB	2	2.25		$\text{k}\Omega$
Mute	Mute Suppression	$V_{IN} = 0.5V_{RMS}$, on one input	90			dB

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ELECTRICAL CHARACTERISTICS (continued)

$T_{amb} = 25^{\circ}\text{C}$, $AV_{CC} = VV_{CC} = 8\text{V}$, $V_{CC12} = 12\text{V}$, $R_{LOUTA} = 10\text{k}\Omega$, $R_{GA} = 600\Omega$, $R_{GV} = 50\Omega$, $R_{LOUTV} = 4.7\text{k}\Omega$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VIDEO SECTION						
V_{DCIN}	DC Input Level	Bottom Synch Pulse		2		V
I_{CLAMP}	Clamping current	at $V_{DCIN} - 400\text{mV}$	1	2		mA
I_{LEAK}	Input Leakage Current	$V_{IN} = V_{DCIN} + 1\text{V}$		1	10	μA
C_{IN}	Input Capacitance			2		pF
V_{IN}	Max Input Signal	$VV_{CC} = 8\text{V}$	1.5	2		V_{PP}
DYN	Dynamic Output Signal	$VV_{CC} = 8\text{V}$	3	4		V_{PP}
BW	Bandwidth at -3dB Y/CVBS RGB Y/C mixer (on RF out)	$V_{IN} = 1V_{PP}$ $V_{IN} = 1V_{PP}$ $V_{INY} = 1V_{PP}$, $V_{INC} = \text{muted}$	15 15 10	18 18 15		MHz MHz MHz
CT	Crosstalk Isolation between Channels	$V_{IN} = 1V_{PP}$ at $f = 5\text{MHz}$, on one input	50	60		dB
R_{OUT}	Output Resistance			50		Ω
R_{LOAD}	Load Impedance		1	4.7	∞	k Ω
G_{RGB}	Gain at RGB outputs	$V_{IN} = 1V_{PP}$, gain set to 6dB	5.5	6	6.5	dB
G_{RGBM}	Gain matching between R, G, B	$V_{IN} = 1V_{PP}$, gain set to 6dB	-0.3	0	0.3	dB
$G_{RGBSTEP}$	Step of Gain	3dB to 6dB	0.75	1	1.25	dB
G_{YCVBS}	Gain on Y/CVBS channels	$V_{IN} = 1V_{PP}$	5.5	6	6.5	dB
G_{YCVBSM}	Gain matching between Y, CVBS inputs	$V_{IN} = 1V_{PP}$	-0.5	0	0.5	dB
DC_{OUT}	DC Output Voltage	Bottom sync pulse	1.1	1.3		V
$DC_{OUT\text{ RF}}$	RF Output Voltage	Bottom sync pulse	1.5	1.8		V
DPHI	Differential Phase	$V_{IN} = 1V_{PP}$, 4.43MHz		0.7		$^{\circ}$
DG	Differential Gain	$V_{IN} = 1V_{PP}$, 4.43MHz		0.4		%
Mute	Mute Suppression	$V_{IN} = 1V_{PP}$ at $f = 5\text{MHz}$, on one input	-55			dB
I_{VOUT}	Output current	$V_{OUT\text{ DC}} @ +1\text{V}$	1.5	2.5		mA

CHROMA SECTION

V_{DCIN}	DC Input Level			3		V
R_{IN}	Input Resistance		45	55		k Ω
C_{IN}	Input Capacitance			2		pF
V_{IN}	Max Input Signal		1.5	2		V_{PP}
Dyn	Dynamic Output Signal		3	3.8		V
DC_{OUT}	DC Output Voltage		1.9	2.3		V
CBW	Chroma Bandwidth	$C_{IN} = 1V_{PP}$ at -3dB	10	19		MHz
CT	Crosstalk Isolation between Channel	$V_{IN} = 1V_{PP}$ at $f = 5\text{MHz}$, on one input		52		dB
R_{OUT}	Output Resistance			50		Ω
G_{OUTC}	Gain at OUTC	$V_{IN} = 1V_{PP}$	5.5	6	6.5	dB
G_{CM}	Gain matching between C inputs	$V_{IN} = 1V_{PP}$	-0.5	0	0.5	dB
Mute	Mute Suppression	$V_{IN} = 1V_{PP}$ at $f = 5\text{MHz}$, on one input	55			dB
CtoYdel	Chroma to luma delay,source Y/C	Pin other than RF_OUT 1, $V_{PP} @ 5\text{MHz}$		± 4	± 20	ns
CtoYdel	Chroma to luma delay,source Y/C	Pin RF_OUT		± 4	± 20	ns

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ELECTRICAL CHARACTERISTICS (continued)

$T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = V_{CC} = 8\text{V}$, $V_{CC12} = 12\text{V}$, $R_{LOUTA} = 10\text{k}\Omega$, $R_{GA} = 600\Omega$, $R_{GV} = 50\Omega$, $R_{LOUTV} = 4.7\text{k}\Omega$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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SLOW BLANKING SECTION

INPUT (Input mode $V_{CC8} = 8\text{V} \pm 5\%$)						
SLB _{low}	Input Low Level Threshold		2.5	3.25	4	V
SLB _{high}	Input High Level Threshold		7.5	8.25	9	V
I_{IN}	Input current			50	100	μA
OUTPUT (Output mode $V_{CC12} = 12\text{V} \pm 5\%$, $V_{CC8} = 8\text{V} \pm 5\%$, $R_{LOAD} > 10\text{k}\Omega$)						
SLB _{LOW}	Output Low Level (int. TV)		0	0.02	1.5	V
SLB _{MED}	Output Med Level (ext. 16/9)		5	5.75	6.5	V
SLB _{HIGH}	Output High Level (ext. 4/3)		10	11	12	V

FAST BLANKING SECTION

INPUT (Input mode $V_{CCV} = 8\text{V} \pm 5\%$)						
FB _{low/high}	Input Low/High Level Threshold		0.4	0.7	0.9	V
I_{IN}	Input current			2	10	μA
OUTPUT (Output mode $V_{CCV} = 8\text{V} \pm 5\%$, $R_{LOAD} > 1\text{k}\Omega$)						
FB _{LOW}	Output Low Level	$I_{IN} = 1.0\text{mA}$ $I_{IN} = 0.2\text{mA}$	0		0.7 0.3	V V
FB _{HIGH}	Output High Level	$I_{OUT} = 1.0\text{mA}$	3.6	4	4.4	V
FB _{DEL}	Fast blanking to RGB delay	at 50% on digital RGB transients, at 2.7V _{ON} FB rise transient, at 1.5V on FB fall $C_{LOAD} = 10\text{pF}$ max		30		ns
FB _{TRANS}	Fast Blanking transitions at FB output Rise Time Fall Time	$C_{LOAD} = 10\text{pF}$ max between 10% and 90% between 90% and 10%		30 30		ns ns

ADDRESS SELECTION INPUT

ADDsel_L	Address selection low level			0	0.2	V
ADDsel_H	Address selection high level		4		V_{CC} (8V)	V
I_{LEAK}	Leakage Current				10	μA

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ELECTRICAL CHARACTERISTICS (continued)

$T_{amb} = 25^{\circ}\text{C}$, $AV_{CC} = VV_{CC} = 8\text{V}$, $V_{CC12} = 12\text{V}$, $R_{LOUTA} = 10\text{k}\Omega$, $R_{GA} = 600\Omega$, $R_{GV} = 50\Omega$, $R_{LOUTV} = 4.7\text{k}\Omega$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I²C BUS CHARACTERISTICS						
SCL						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		3		5.5	V
I_{LI}	Input Leakage Current	$V_{IN} = 0$ to 5.5V	-10	0	10	μA
f_{SCL}	Clock Frequency		0		100	kHz
t_R	Input Rise Time	1.5V to 3V			1	μs
t_F	Input Fall Time	1.5V to 3V			300	ns
C_I	Input Capacitance				10	pF
SDA						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		3		5.5	V
I_{LI}	Input Leakage Current	$V_{IN} = 0$ to 5.5V	-10	0	10	μA
C_I	Input Capacitance				10	pF
t_R	Input Rise Time	1.5V to 3V			1	μs
t_F	Input Fall Time	1.5V to 3V			300	ns
V_{OL}	Low level Output Voltage	$I_{OL} = 3\text{mA}$			0.4	V
t_F	Output Fall Time	3V to 1.5V			250	ns
C_L	Load Capacitance				400	pF
TIMING						
t_{LOW}	Clock Low Period		4.7			μs
t_{HIGH}	Clock High Period		4			μs
$t_{SU,DAT}$	Data Set-up Time		250			ns
$t_{HD,DAT}$	Data Hold Time		0		340	ns
$t_{SU,STO}$	Set-up Time from Clock High to Stop		4			μs
t_{BUF}	Start Set-up Time following a Stop		4.7			μs
$t_{HD,STA}$	Start Hold Time		4			μs
$t_{SU,STA}$	Start Set-up Time following Clock Low to High Transition		4.7			μs

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STV6410A

I²C BUS SELECTION

Data transfers follow the usual I2C format: after the start condition (S), a 7-bit slave address is sent, followed by an eighth bit which is a data direction bit (W). A 8-bit subaddress is sent to select a register, followed by a 8-bit data word to put in it.

The IC's I2C bus decoder permits the automatic incrementation mode in write mode.

String Format

Write only mode (S : start condition, P : stop condition, A : acknowledge)

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	DATA	A	P
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Read only mode

S	SLAVE ADDRESS	1	A	DATA	A	P
---	---------------	---	---	------	---	---

Slave Address

Address	A6	A5	A4	A3	A2	A1	A0
Value	1	0	0	1	0	1	X

Auto Increment Mode

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	DATA0	A	DATA1	A	DATAN	A	P
---	---------------	---	---	------------	---	-------	---	-------	---	-------	-------	---	---

I²C Bus Address

Write Address : 1001 01X0

Read Address : 1001 01X1

Address Selection Pin Grounded : X = 0, write address = 94HEX, read address = 95HEX

Address Selection Pin to Supply : X = 1, write address = 96HEX, read address = 97HEX

Input Signals Summary (Write Mode)

Reg. Address (HEX)	DATA D7	DATA D6	DATA D5	DATA D4	DATA D3	DATA D2	DATA D1	DATA D0
00	TV Audio Level Adjustment			0/6dBGain	TV Mono	TV Audio Outputs control		
01	Cinch Audio Level Adjustment			0/6dBGain	Not used	Cinch Audio Outputs control		
02	AUX Mono	VCR Mono	AUX Audio Outputs control			VCR Audio Outputs control		
03	Not used	TV chroma mute	Y/CVBS & Chroma TV outputs control			TV RF ouput control		TV R/C ouput control
04	TV RGB outputs control		TV FB Output control		RGB Gain		R/Csub AUX Clamp	R/Csub Encoder Clamp
05	AUX Chroma Mute	AUX Y/CVBS & Chrroma Outputs control			VCR Chroma Mute	VCR Y/CVBS & Chroma Outputs control		
06	Not used	Not used	Slow Blanking AUX SCART		Slow Blanking VCR SCART		Slow Blanking TV SCART	
07	VCR Output OFF	AUX Output OFF	TV Output OFF	ENCOD Clamp disable	TV Clamp disable	ASTB Clamp disable	VCR Clamp disable	AUX Clamp disable
08	Not used	Not used	Not used	Not used	Not used	Not used	RF Mod Output OFF	CINCH Output OFF

Not used data must be put to "0"

I²C BUS SELECTION (continued)

Input Signals (Write Mode)

Data Byte

TV Audio Output

Register Address (HEX)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
00	Audio Output selection	3	X	X	X	X	X	0	0	0	Muted
			X	X	X	X	X	0	0	1	AUX inputs selected
			X	X	X	X	X	0	1	0	VCR inputs selected
			X	X	X	X	X	0	1	1	ASTB inputs selected
			X	X	X	X	X	1	0	0	NOT ALLOWED
			X	X	X	X	X	1	0	1	Encoder inputs selected
			X	X	X	X	X	1	1	0	NOT ALLOWED
			X	X	X	X	X	1	1	1	NOT ALLOWED
	Stereo or Mono Mode	1	X	X	X	X	0	X	X	X	0 = Stereo
			X	X	X	X	1	X	X	X	1 = Mono
	6dB Extra Gain	1	X	X	X	0	X	X	X	X	0 = 0dB
			X	X	X	1	X	X	X	X	1 = +6dB
Level Adjustment	3	0	0	0	X	X	X	X	X	0dB Adjustment	
		1	1	1	X	X	X	X	X	-14dB Adjustment (-2dB/step)	

Audio Cinch Output

Register Address (HEX)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
01	Audio Output Selection	3	X	X	X	X	X	0	0	0	Muted
			X	X	X	X	X	0	0	1	AUX inputs selected
			X	X	X	X	X	0	1	0	VCR inputs selected
			X	X	X	X	X	0	1	1	ASTB inputs selected
			X	X	X	X	X	1	0	0	TV inputs selected
			X	X	X	X	X	1	0	1	Encoder input selected
			X	X	X	X	X	1	1	0	NOT ALLOWED
			X	X	X	X	X	1	1	1	NOT ALLOWED
6dB Extra Gain	1	X	X	X	0	X	X	X	X	0 = 0dB	
		X	X	X	1	X	X	X	X	1 = +6dB	
Level Adjustment	3	0	0	0	X	X	X	X	X	0dB Adjustment	
		1	1	1	X	X	X	X	X	-14dB Adjustment (-2dB/step)	

I²C BUS SELECTION (continued)

VCR And AUX Audio Outputs Selection

Register Address (HEX)	Description	Bits	Data							Comments	
			d7	d6	d5	d4	d3	d2	d1		d0
02	VCR Audio Output Selection	3	X	X	X	X	X	0	0	0	Muted
			X	X	X	X	X	0	0	1	AUX inputs selected
			X	X	X	X	X	0	1	0	NOT ALLOWED
			X	X	X	X	X	0	1	1	ASTB inputs selected
			X	X	X	X	X	1	0	0	TV inputs selected
			X	X	X	X	X	1	0	1	Encoder inputs selected
			X	X	X	X	X	1	1	0	NOT ALLOWED
			X	X	X	X	X	1	1	1	NOT ALLOWED
			X	0	X	X	X	X	X	X	0 = Stereo
	X	1	X	X	X	X	X	X	1 = Mono		
	AUX Audio Output Selection	3	X	X	0	0	0	X	X	X	Muted
			X	X	0	0	1	X	X	X	NOT ALLOWED
			X	X	0	1	0	X	X	X	VCR inputs selected
			X	X	0	1	1	X	X	X	ASTB inputs selected
			X	X	1	0	0	X	X	X	TV inputs selected
			X	X	1	0	1	X	X	X	Encoder inputs selected
			X	X	1	1	0	X	X	X	NOT ALLOWED
			X	X	1	1	1	X	X	X	NOT ALLOWED
			0	X	X	X	X	X	X	X	0 = Stereo
1			X	X	X	X	X	X	X	1 = Mono	

I²C BUS SELECTION (continued)

TV Video Output

Register Address (HEX)	Description	Bits	Data							Comments	
			d7	d6	d5	d4	d3	d2	d1		d0
03	R/C TV Output Selection	1	X	X	X	X	X	X	X	0	Red signal selected
			X	X	X	X	X	X	X	1	Chroma signal selected
	RF output : adder control and chroma subcarrier filter selection	2	X	X	X	X	X	X	0	X	CVBS to RF output
			X	X	X	X	X	X	1	X	Y+C to RF output
			X	X	X	X	X	0	X	X	Filter not active
			X	X	X	X	X	1	X	X	Filter active
	Y/CVBS output and chroma signal selection	3	X	X	0	0	0	X	X	X	Y/CVBS & chroma muted
			X	X	0	0	1	X	X	X	Y/CVBS_AUX & R/C_AUX
			X	X	0	1	0	X	X	X	Y_AUX & R/C_AUX
			X	X	0	1	1	X	X	X	Y/CVBS_VCR & C_VCR
			X	X	1	0	0	X	X	X	CVBS_ASTB & Chr. muted
			X	X	1	0	1	X	X	X	Y/CVBS_ENC & R/C_ENC
			X	X	1	1	0	X	X	X	Y_ENC & C_ENC
	Chroma switch muting	1	X	0	X	X	X	X	X	X	Chroma Output controlled by d5-d4-d3 from register 03.
			X	1	X	X	X	X	X	X	Chroma Output forced to mute.
	04	ENCODER R/Csub Clamp	1	X	X	X	X	X	X	0	Bottom Level Clamp
				X	X	X	X	X	X	1	Average Level Clamp
AUX R/Csub Clamp		1	X	X	X	X	X	X	0	X	Bottom Level Clamp
			X	X	X	X	X	X	1	X	Average Level Clamp
RGB output Gain		2	X	X	X	X	0	0	X	X	+6dB gain
			X	X	X	X	1	1	X	X	+3dB gain (1dB/Step)
FB Output		2	X	X	0	0	X	X	X	X	FB forced to low level
			X	X	0	1	X	X	X	X	FB forced to high level
			X	X	1	0	X	X	X	X	FB from Encoder
			X	X	1	1	X	X	X	X	FB from AUX
RGB outputs selection		2	0	0	X	X	X	X	X	X	Muted
			0	1	X	X	X	X	X	X	RGB_Encoder selected
			1	0	X	X	X	X	X	X	RGB_AUX selected
	1		1	X	X	X	X	X	X	NOT ALLOWED	

I²C BUS SELECTION (continued)

VCR And AUX Video Outputs

Register Address (HEX)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
05	VCR Y/CVBS & Chroma Outputs Selection	3	X	X	X	X	X	0	0	0	Y/CVBS & chroma muted
			X	X	X	X	X	0	0	1	Y/CVBS_AUX & R/C_AUX
			X	X	X	X	X	0	1	0	Y_AUX & R/C_AUX
			X	X	X	X	X	0	1	1	NOT ALLOWED
			X	X	X	X	X	1	0	0	CVBS_ASTB & Chr. muted
			X	X	X	X	X	1	0	1	Y/CVBS_ENC & R/C_ENC
			X	X	X	X	X	1	1	0	Y_ENC & C_ENC
			X	X	X	X	X	1	1	1	Y/CVBS_TV & C_TV
	VCR Chroma Output Muting	1	X	X	X	X	0	X	X	X	Chroma Output controlled by d2-d1-d0 from register 05.
			X	X	X	X	1	X	X	X	Chroma Output forced to mute.
	AUX Video Output Selection	3	X	0	0	0	X	X	X	X	Y/CVBS & chroma muted
			X	0	0	1	X	X	X	X	NOT ALLOWED
			X	0	1	0	X	X	X	X	NOT ALLOWED
			X	0	1	1	X	X	X	X	Y/CVBS_VCR & C_VCR
			X	1	0	0	X	X	X	X	CVBS_ASTB & Chr. muted
			X	1	0	1	X	X	X	X	Y/CVBS_ENC & R/C_ENC
			X	1	1	0	X	X	X	X	Y_ENC & C_ENC
			X	1	1	1	X	X	X	X	Y/CVBS_TV & C_TV
	AUX Chroma Output Muting	1	0	X	X	X	X	X	X	X	Chroma Output controlled by d6-d5-d4 from register 05.
			1	X	X	X	X	X	X	X	Chroma Output forced to mute.

Slow Blanking Switches

Register Address (HEX)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
06	Slow Blanking TV SCART	2	X	X	X	X	X	X	0	0	Input mode
			X	X	X	X	X	X	0	1	Output < 2V
			X	X	X	X	X	X	1	0	Output 16/9 format
			X	X	X	X	X	X	1	1	Output 4/3 format
	Slow Blanking VCR SCART	2	X	X	X	X	0	0	X	X	Input mode
			X	X	X	X	0	1	X	X	Output < 2V
			X	X	X	X	1	0	X	X	Output 16/9 format
			X	X	X	X	1	1	X	X	Output 4/3 format
	Slow Blanking AUX SCART	2	X	X	0	0	X	X	X	X	Input mode
			X	X	0	1	X	X	X	X	Output < 2V
			X	X	1	0	X	X	X	X	Output 16/9 format
			X	X	1	1	X	X	X	X	Output 4/3 format

I²C BUS SELECTION (continued)

Standby Modes Selection

Register Address (HEX)	Description	Bits	Data							Comments	
			d7	d6	d5	d4	d3	d2	d1		d0
07	AUX Clamps Disabling	1	X	X	X	X	X	X	X	0	Clamp Active
			X	X	X	X	X	X	X	1	Clamp Disabled
	VCR Clamps Disabling	1	X	X	X	X	X	X	0	X	Clamp Active
			X	X	X	X	X	X	1	X	Clamp Disabled
	ASTB Clamps Disabling	1	X	X	X	X	X	0	X	X	Clamp Active
			X	X	X	X	X	1	X	X	Clamp Disabled
	TV Clamps Disabling	1	X	X	X	X	0	X	X	X	Clamp Active
			X	X	X	X	1	X	X	X	Clamp Disabled
	Encoder Clamps Disabling	1	X	X	X	0	X	X	X	X	Clamp Active
			X	X	X	1	X	X	X	X	Clamp Disabled
	TV/RGB Output Disabling	1	X	X	0	X	X	X	X	X	Audio & Video Outputs ON
			X	X	1	X	X	X	X	X	Audio & Video Outputs OFF
AUX Output Disabling	1	X	0	X	X	X	X	X	X	Audio & Video Outputs ON	
		X	1	X	X	X	X	X	X	Audio & Video Outputs OFF	
VCR Output Disabling	1	0	X	X	X	X	X	X	X	Audio & Video Outputs ON	
		1	X	X	X	X	X	X	X	Audio & Video Outputs OFF	
08	CINCH Output Disabling	1	X	X	X	X	X	X	X	0	CINCH Output ON
			X	X	X	X	X	X	X	1	CINCH Output OFF
	RF MOD Output Disabling	1	X	X	X	X	X	X	0	X	RF MOD Output ON
			X	X	X	X	X	X	1	X	RF MOD Output OFF

Output Signals (Read Mode)

Data Byte

Register Address (HEX)	Description	Bits	Data							Comments	
			d7	d6	d5	d4	d3	d2	d1		d0
	Slow Blanking TV SCART	2	X	X	X	X	X	X	0	1	Input < 2V
			X	X	X	X	X	X	1	0	Input 16/9 format
			X	X	X	X	X	X	1	1	Input 4/3 format
	Slow Blanking VCR SCART	2	X	X	X	X	0	1	X	X	Input < 2V
			X	X	X	X	1	0	X	X	Input 16/9 format
			X	X	X	X	1	1	X	X	Input 4/3 format
	Slow Blanking AUX SCART	2	X	X	0	1	X	X	X	X	Input < 2V
			X	X	1	0	X	X	X	X	Input 16/9 format
			X	X	1	1	X	X	X	X	Input 4/3 format

I²C BUS SELECTION (continued)

Power-on Reset - Bus Register Initial Conditions

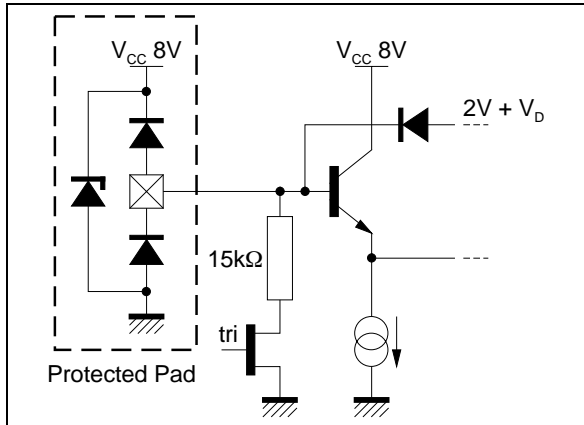
Power on reset is active when the power supply voltage is below (Tbf) volts.

Not significant bits (X) are preset to "0"

Register Address HEX	DATA								COMMENTS
	d7	d6	d5	d4	d3	d2	d1	d0	
00	0	0	0	0	0	0	0	0	Audio TV Output Muted, Stereo Mode, 0dB Gain, 0dB Gain Adjustment.
01	0	0	0	0	0	0	0	0	Audio Cinch Output Muted, 0 dB Gain, 0dB Gain Adjustment.
02	0	0	0	0	0	0	0	0	Audio VCR Output Muted, Audio AUX Output Muted.
03	0	0	0	0	0	0	0	0	Red signal selected on R/C_TV output, CVBS to RF output, TV video and chroma switches muted, Chroma output controlled by d5-d4-d3 from register 03.
04	0	0	0	0	0	0	0	0	Encoder R/Csub Bottom Level Clamp, AUX R/Csub Bottom Level Clamp, RGB Outputs 6dB Gain, FB Output forced to 0V, RGB outputs muted.
05	0	0	0	0	0	0	0	0	VCR Video and chroma switches Muted, VCR Chroma Output controlled by d2-d1-d0 from register 05, AUX Video and chroma switches Muted, AUX Chroma Output controlled by d6-d5-d4 from register 05.
06	0	0	0	0	0	0	0	0	TV SCART Slow Blanking Input Mode, VCR SCART Slow Blanking Input Mode, AUX SCART Slow Blanking Input Mode.
07	0	0	0	0	0	0	0	0	AUX, VCR, ASTB, TV, ENCODER Clamps Active ; TV/RGB, AUX, VCR Outputs ON.
08	0	0	0	0	0	0	0	0	Cinch, RF Mod Outputs ON.

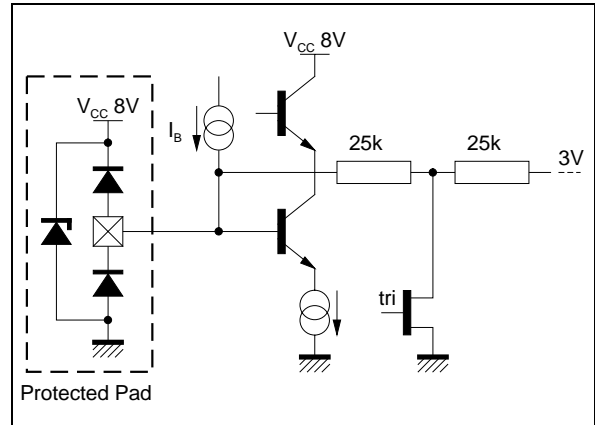
INPUT/OUTPUT GROUPS

Figure 1 : Bottom Clamped Video Inputs (Pins 24, 26, 30, 32, 34, 36, 38, 44, 46, 50, 52)



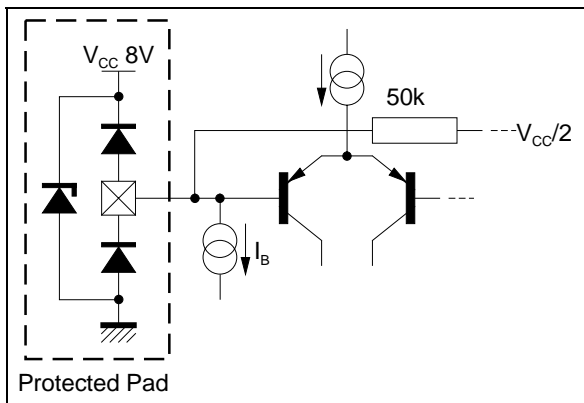
6410A-03.EPS

Figure 2 : Average Clamped Video Inputs (Pins 40, 48, 54)



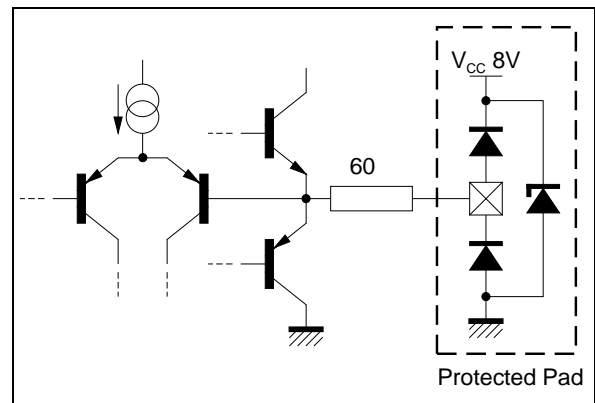
6410A-04.EPS

Figure 3 : Audio Inputs (5 Stereo) (Pins 35-37, 39-41, 47-49, 53-56)



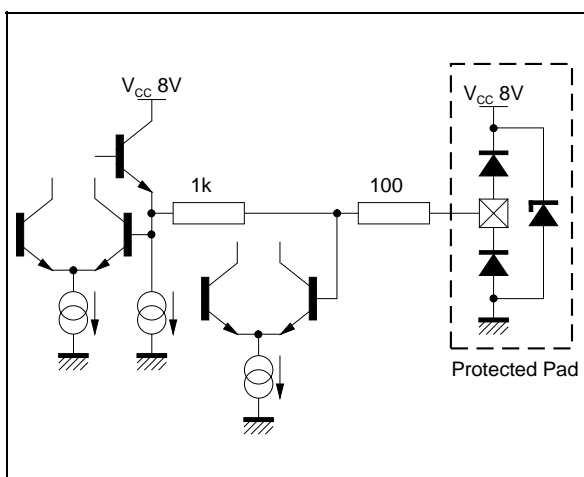
6410A-05.EPS

Figure 4 : Audio Outputs (4 Stereo +1) (Pins 58, 59, 60-62, 4-6, 8)



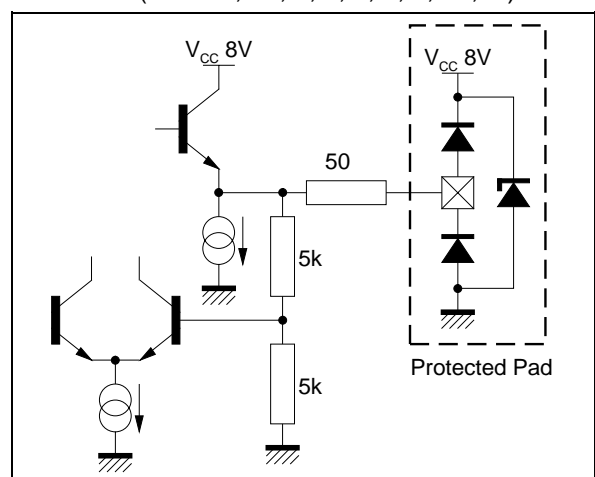
6410A-06.EPS

Figure 5 : Trap Filter (Pin 11)



6410A-07.EPS

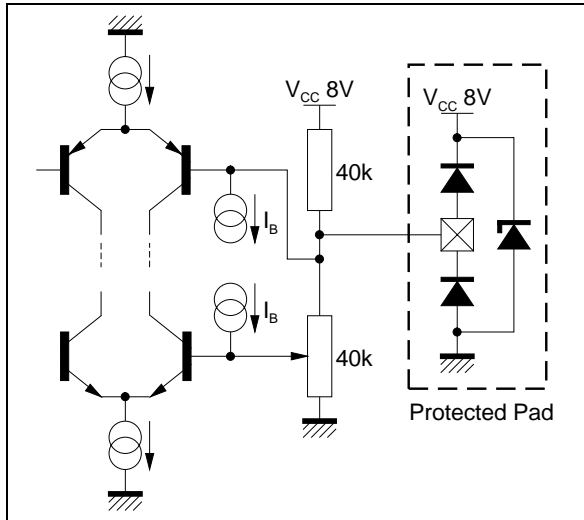
Figure 6 : Video Outputs (Pins 61, 63, 1, 3, 5, 7, 9, 13,15)



6410A-08.EPS

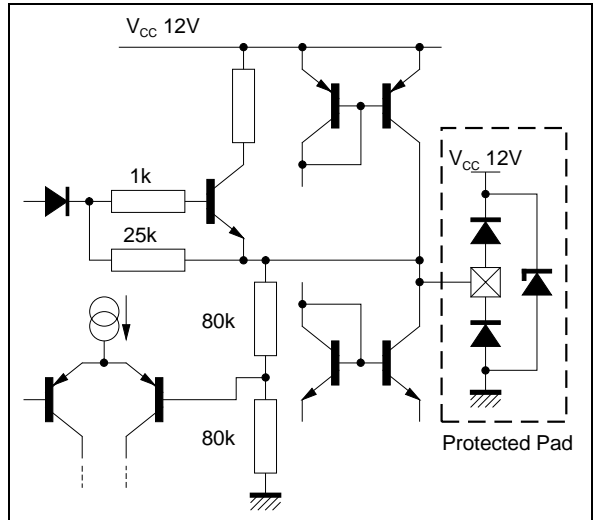
INPUT/OUTPUT GROUPS (continued)

Figure 7 : V_{REF} External Capacitor (Pin 51)



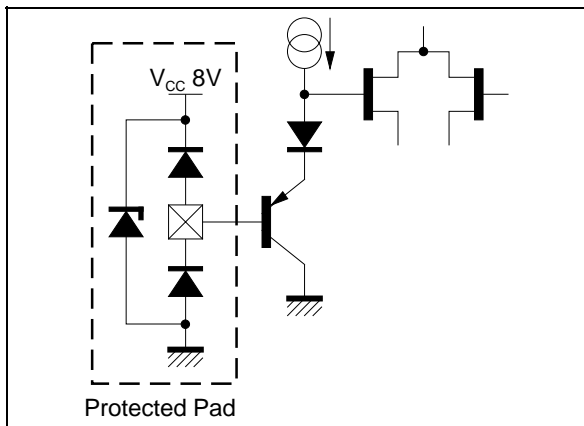
6410A-09.EPS

Figure 8 : Slow Blanking (Pins 25, 27, 31)



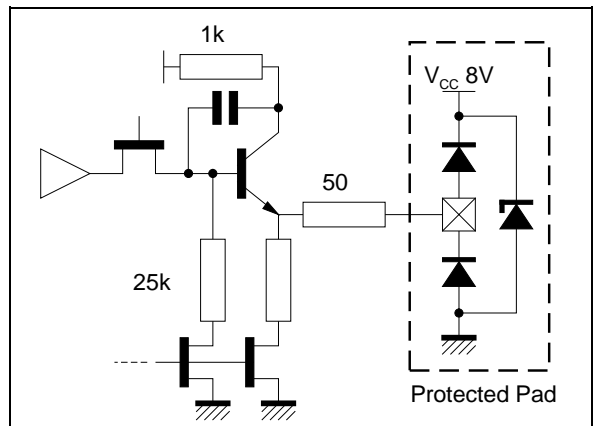
6410A-10.EPS

Figure 9 : Input Fast Blanking (Pins 18, 19)



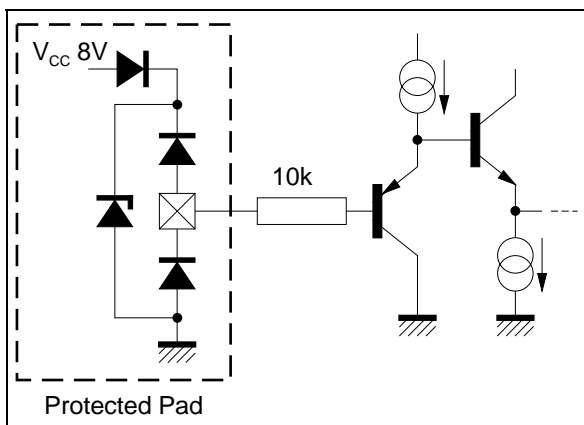
6410A-11.EPS

Figure 10 : Output Fast Blanking (Pin 17)



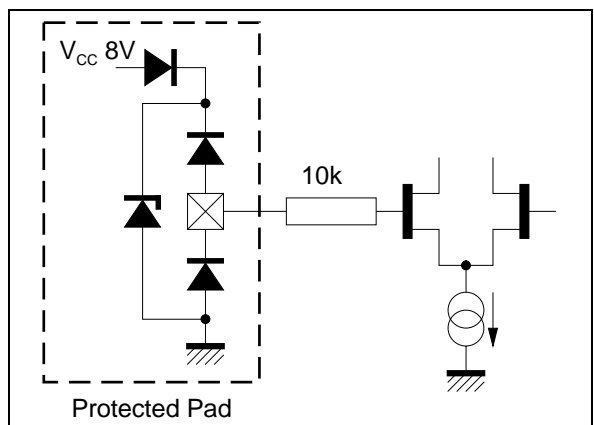
6410A-12.EPS

Figure 11 : I^2C Bus (Add) (Pin 20)



6410A-13.EPS

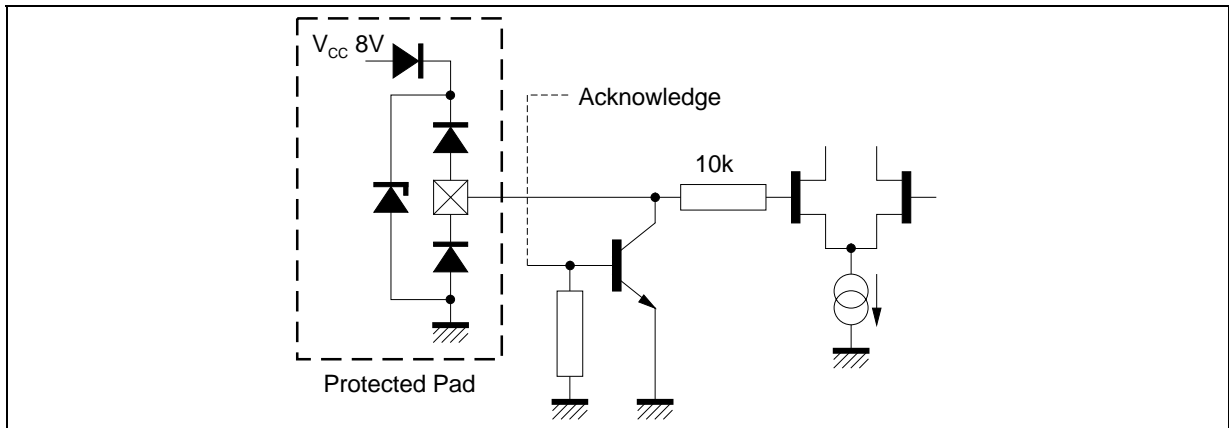
Figure 12 : I^2C Bus (SCL) (Pin 21)



6410A-14.EPS

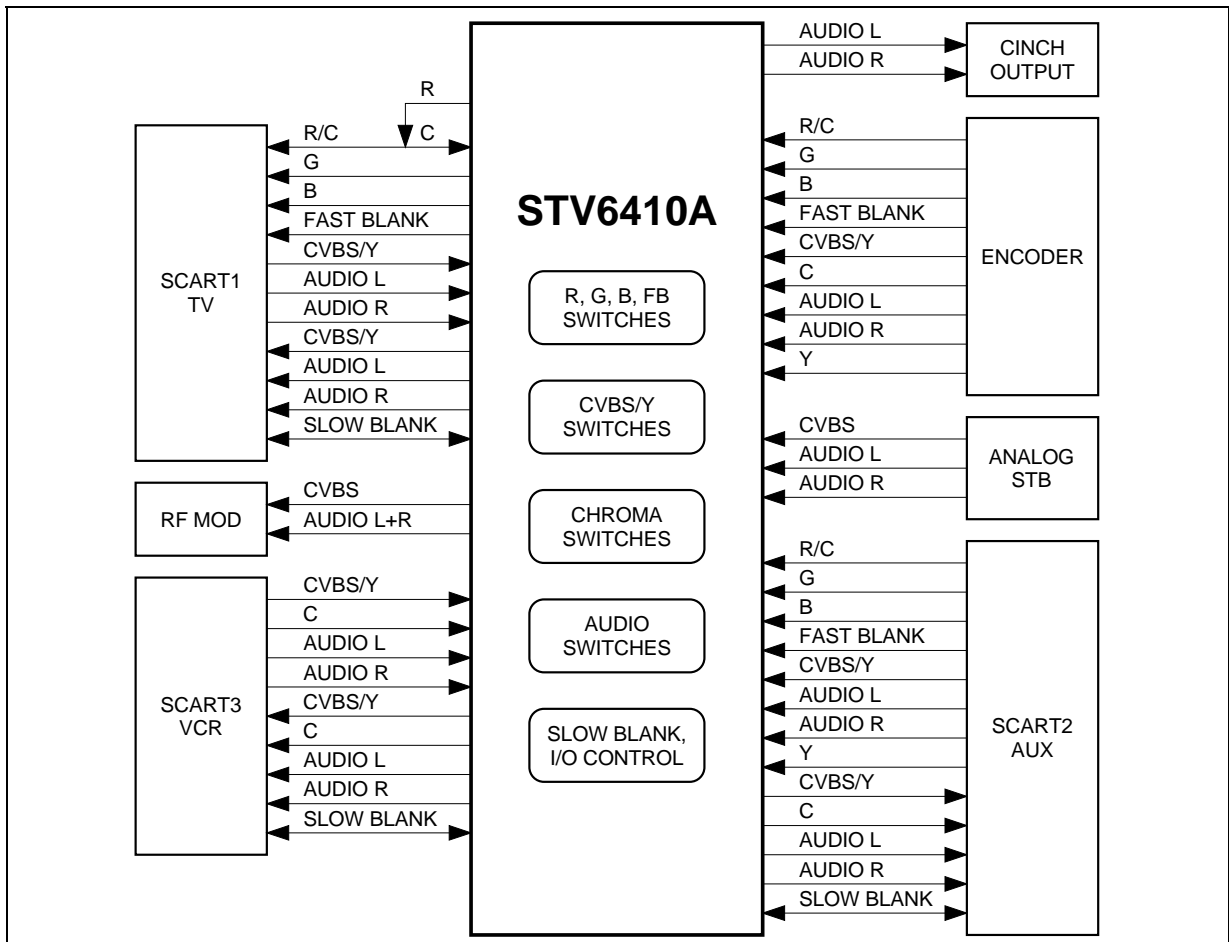
INPUT/OUTPUT GROUPS (continued)

Figure 13 : I²C Bus (SDA) (Pin 22)



6410A-15.EPS

APPLICATION DIAGRAM



6410A-16.EPS

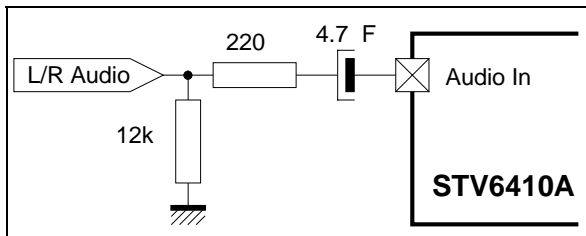
APPLICATION NOTE

1 - Audio Part

1.a - Inputs

The audio inputs are designed to follow sources up to (at least) $2V_{RMS}$ (that is around $6V_{PP}$) with an expected DC level of $V_{CC}/2$ (4V typ.). That's why the device is providing this DC polarization. That means that in most of the cases the inputs are AC coupled via chemical capacitors. The recommended values are $1\mu F$, $2.2\mu F$ or $4.7\mu F$ (internal polar. is made via a $50k\Omega$ resistor). I want to point out that the internal polarization is filtered by an external capacitor (on Pin called 'VREF'). This capacitor contribute to good performance of the device. Its value should be $47\mu F$ or more (coupled with an $47nF$ HF cap. for internal video references).

Figure 14 : Audio Inputs

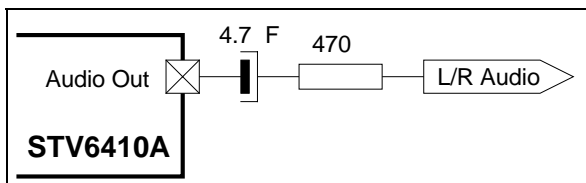


NB: In some particular cases (loopback from outputs to inputs) the AC coupling capacitor can be removed... but some small offsets in the audio chain can cause some noise while switching from one input to another.

1.b - Outputs

Audio output buffers are able to provide more than $2.1V_{RMS}$ (around $6V_{PP}$) on a typical load of $10k\Omega$ (in fact a $2k\Omega$ load is acceptable). The DC level is once more $V_{CC}/2$ for best dynamic performance. Usually some AC coupling capacitors are used at the outputs. To drive some typical $10k\Omega$ loads, it is normal to use capacitors with value 5 to 10 times the value of the input capacitors. That gives a value between $4.7\mu F$ and $47\mu F$. Moreover it can be a good idea to insert resistors (220Ω or 470Ω) in the audio outputs. That will provide a protection for output stages. No external drivers or buffers are needed in typical use of the device.

Figure 15 : Audio Outputs



2 - Video Part

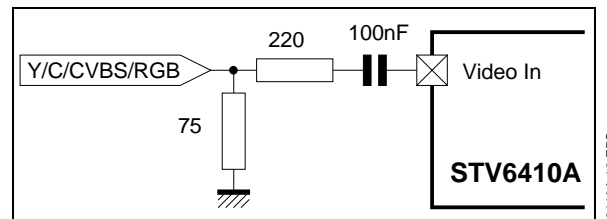
2.a - Inputs

Video inputs need to be AC coupled. But only some small capacitor values are requested thanks to the internal clamps provided by these devices. Usually some $100nF$ HF capacitors ($47nF$ to $220nF$) are enough to provide good performances on Y, CVBS, RGB and C inputs.

Chrominance inputs : - average clamp - that means that the DC is measured as the average value of the input signal and set to an internal reference (close to 3V). The dynamic allowed is more than 1.5V.

RGB, Y, CVBS inputs : - bottom sync top clamp - that means that the DC level is measured at the lowest value of the input signal and set to an internal reference (close to 2V). The dynamic allowed is more than 1.5V.

Figure 16 : Video Inputs

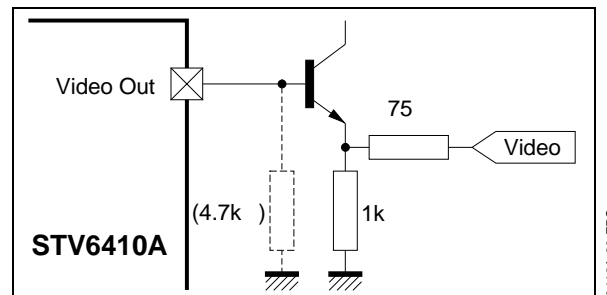


2.b - Outputs

On these devices the video outputs are NOT ABLE to drive 150Ω . That means that external buffers (one simple NPN-Transistor per output) are needed. To reduce the external components, the output DC level have been chosen to allow a direct drive of the base of the output follower (NPN). The emitters of the NPNs will be polarized to ground via $1k\Omega$ resistors (more or less) and will drive the outputs through some 75Ω resistors. Do not forget to bufferize your favourite UHF modulator video input...

Chrominance outputs have a DC of 2.3V (it is an average value) and Luminance type output have a DC of 1.3V (it is a bottom value).

Figure 17 : Video (and Fast Blanking) Outputs



APPLICATION NOTE (continued)**2.c - Fast Blanking**

Fast Blanking signal is used to make an equipment consider its RGB inputs for full-screen display or fast insertion (OSD, etc.). The output of such signal is exactly managed in the same way as RGB (that is important for levels and delays).

The input is DC coupled (insert a few hundreds ohms resistors for external input).

2.d - Slow Blanking

Slow Blanking signal is used to make an equipment consider an external input (e.g. CVBS and SOUND). The input/output of such signal is very simple, DC coupled (insert a few hundreds ohms resistors for external I/O). Notice that this function is requesting a 12V power supply (on Pin V_{CC12}). This pin can be left open (not pulled down) if this function is not used.

3 - I²C Bus**3.a - Address**

You can choose the address of the device by

setting the Pin ADD to ground or to V_{DD}. The former selects 94h and the latter selects 96h. These values correspond to the writeable (or control) registers. Change the lowest bits to '1' (that gives 95h and 97h) to read the readable register of the device. One device will answer (acknowledge) to its both addresses 94h and 95h or 96h and 97h.

3.b - Write Mode

This mode is used to control the device, to select switches positions, gains, etc.

Send a start condition, the address of the device, the address of the register (its number), and the data to put in it. At this point you can send a stop or send the data of the following registers (that is what we call auto-increment).

3.c - Read Mode

This mode is used to read some data such as slow-blanking input signals.

Send a start condition, the address of the device (+1) and then send one byte clock to read the unique data register.

N.B.: Do not forget your favourite ESD protections for I/O signals of plugs.

