

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

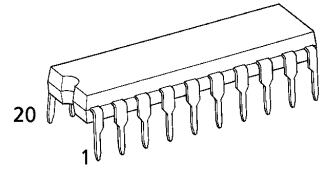
# TC74HC299AP, TC74HC299AF

## 8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

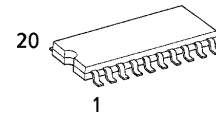
The TC74HC299A is a high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It has four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1). When one or both enable ( $\overline{G1}$ ,  $\overline{G2}$ ) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### FEATURES :

- High Speed.....  $f_{MAX} = 42\text{MHz}(\text{typ.})$  at  $V_{CC} = 5\text{V}$
- Low Power Dissipation.....  $I_{CC} = 4\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity.....  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Output Drive Capability ..... 15 LSTTL Loads For QA~QH  
10 LSTTL Loads For QA', QH'
- Symmetrical Output Impedance...  
 $|I_{OH}| = I_{OL} = 6\text{mA}(\text{min.})$  For QA~QH  
 $|I_{OH}| = I_{OL} = 4\text{mA}(\text{min.})$  For QA', QH'
- Balanced Propagation Delays.....  $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range...  $V_{CC}$  (opr.) = 2V~6V
- Pin and Function Compatible with 74LS299



P (DIP20-P-300-2.54A)  
Weight : 1.30g (Typ.)



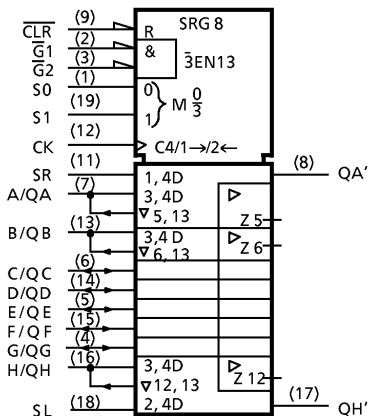
F (SOP20-P-300-1.27)  
Weight : 0.22g (Typ.)

### PIN ASSIGNMENT

S0	1	20	V <sub>CC</sub>
$\overline{G1}$	2	19	S1
$\overline{G2}$	3	18	SL
G/QG	4	17	QH'
E/QE	5	16	H/QH
C/QC	6	15	F/QF
A/QA	7	14	D/QD
QA'	8	13	B/QB
$\overline{CLR}$	9	12	CK
GND	10	11	SR

(TOP VIEW)

### IEC LOGIC SYMBOL



### APPLICATION NOTES

- 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

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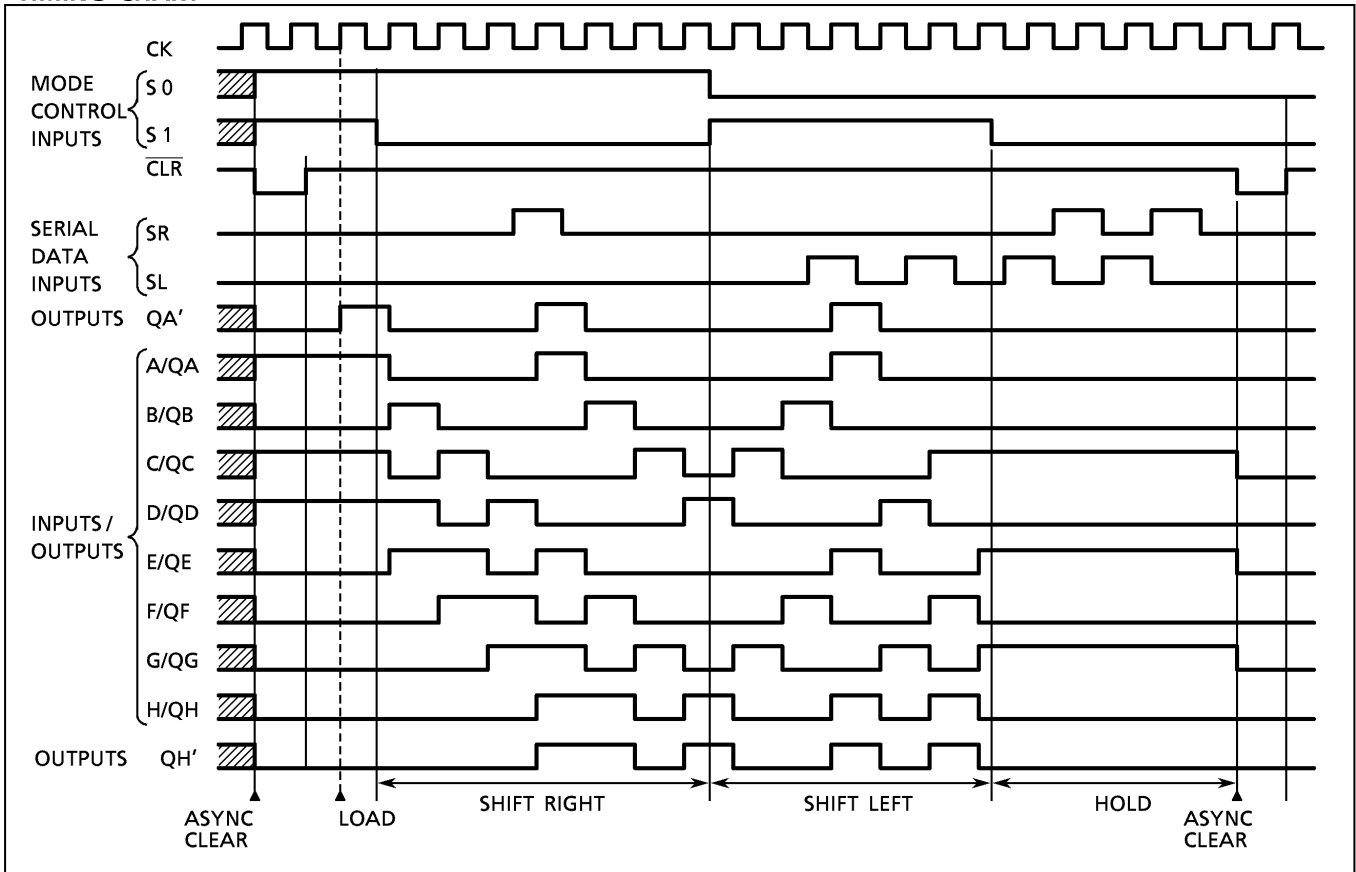
**TRUTH TABLE**

MODE	INPUTS								INPUTS/OUTPUTS		OUTPUTS	
	$\overline{\text{CLR}}$	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{\text{G1}}^*$	$\overline{\text{G2}}^*$		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLR	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT	H	L	H	L	L	$\uparrow$	X	H	H	QGn	H	QGn
RIGHT	H	L	H	L	L	$\uparrow$	X	L	L	QGn	L	QGn
SHIFT	H	H	L	L	L	$\uparrow$	H	X	QBn	H	QBn	H
LEFT	H	H	L	L	L	$\uparrow$	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	$\uparrow$	X	X	a	h	a	h

\* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

- Z : High Impedance
- Qn0 : The level of Qn before the indicated steady - state input conditions were established.
- Qnn : The level of Qn before the most recent active transition indicated by  $\downarrow$  or  $\uparrow$ .
- a, h : The level of the steady - state inputs A, H, respectively.
- X : Don't Care.

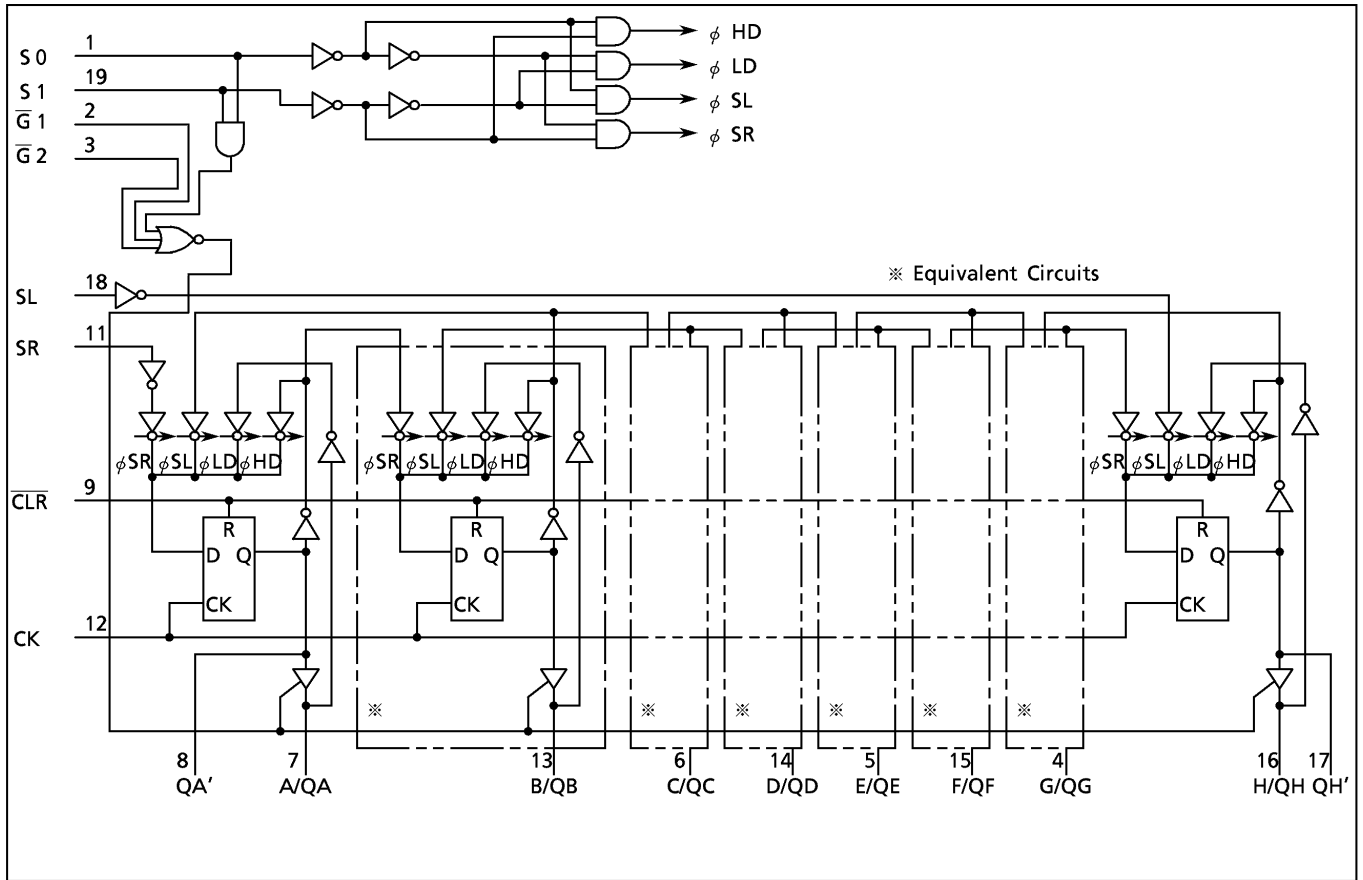
**TIMING CHART**



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SYSTEM DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V <sub>CC</sub>	-0.5~7	V
DC Input Voltage	V <sub>IN</sub>	-0.5~V <sub>CC</sub> +0.5	V
DC Output Voltage	V <sub>OUT</sub>	-0.5~V <sub>CC</sub> +0.5	V
Input Diode Current	I <sub>IK</sub>	±20	mA
Output Diode Current	I <sub>OK</sub>	±20	mA
DC Output Current (Q <sub>H</sub> ') (Q <sub>A</sub> ~Q <sub>H</sub> )	I <sub>OUT</sub>	±25 ±35	mA
DC V <sub>CC</sub> /Ground Current	I <sub>CC</sub>	±75	mA
Power Dissipation	P <sub>D</sub>	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T <sub>stg</sub>	-65~150	°C

\*500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V <sub>CC</sub>	2~6	V
Input Voltage	V <sub>IN</sub>	0~V <sub>CC</sub>	V
Output Voltage	V <sub>OUT</sub>	0~V <sub>CC</sub>	V
Operating Temperature	T <sub>opr</sub>	-40~85	°C
Input Rise and Fall Time	t <sub>r</sub> , t <sub>f</sub>	0~1000 (V <sub>CC</sub> = 2.0V) 0~500 (V <sub>CC</sub> = 4.5V) 0~400 (V <sub>CC</sub> = 6.0V)	ns

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V <sub>IH</sub>		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V <sub>IL</sub>		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OH</sub> = -20µA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
		Q' <sub>A</sub> , Q' <sub>H</sub>   I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
		Q <sub>A</sub> ~Q <sub>H</sub>   I <sub>OH</sub> = -6 mA I <sub>OH</sub> = -7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OL</sub> = 20µA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		Q' <sub>A</sub> , Q' <sub>H</sub>   I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 5.2mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
		Q <sub>A</sub> ~Q <sub>H</sub>   I <sub>OL</sub> = 6 mA I <sub>OL</sub> = 7.8mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3 - State Output Off - State Current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	6.0	—	—	±0.5	—	±5.0	µA
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	—	—	4.0	—	40.0	

TIMING RECOMMENDED OPERATING CONDITIONS ( Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C	UNIT
			V <sub>CC</sub> (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (CLR)	$t_{W(L)}$		2.0	—	75	88	
			4.5	—	15	18	
			6.0	—	12	15	
Minimum Set-up Time ( $\overline{S}$ L, SR, A~H)	$t_s$		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Set-up Time (S0, S1)	$t_s$		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Hold Time (SL, SR, A~H)	$t_h$		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time (S0, S1)	$t_h$		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time ( $\overline{C}$ LR)	$t_{rem}$		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	8	10	
Clock Frequency	f		2.0	—	6	5	
			4.5	—	30	24	
			6.0	—	35	23	

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 15pF, V<sub>CC</sub> = 5V, Ta = 25°C, Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (QA', QH')	$t_{TLH}$ $t_{THL}$		—	4	8	ns
Propagation Delay Time (CK—QA', QH')	$t_{pLH}$ $t_{pHL}$		—	19	30	
Propagation Delay Time ( $\overline{C}$ LR—QA', QH')	$t_{pLH}$ $t_{pHL}$		—	17	30	
Maximum Clock Frequency	$f_{MAX}$		35	73	—	MHz

AC ELECTRICAL CHARACTERISTICS (Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (QA~QH)	$t_{TLH}$ $t_{THL}$		50	2.0	—	25	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Output Transition Time (QA', QH')	$t_{TLH}$ $t_{THL}$		50	2.0	—	30	75	—	95	
				4.5	—	8	15	—	19	
				6.0	—	7	13	—	16	
Propagation Delay Time (CK—QA'QH')	$t_{pLH}$ $t_{pHL}$		50	2.0	—	85	170	—	215	
				4.5	—	23	34	—	43	
				6.0	—	18	29	—	37	
Propagation Delay Time ( $\overline{\text{CLR}}$ —QA'QH')	$t_{pHL}$		50	2.0	—	85	175	—	220	
				4.5	—	24	35	—	44	
				6.0	—	18	30	—	37	
Propagation Delay Time (CK—QA~QH)	$t_{pLH}$ $t_{pHL}$		50	2.0	—	80	160	—	200	
				4.5	—	21	32	—	40	
				6.0	—	17	27	—	34	
			150	2.0	—	100	200	—	250	
				4.5	—	26	40	—	50	
				6.0	—	21	34	—	43	
Propagation Delay Time ( $\overline{\text{CLR}}$ —QA~QH)	$t_{pHL}$		50	2.0	—	85	190	—	240	
				4.5	—	24	38	—	48	
				6.0	—	18	30	—	38	
			150	2.0	—	105	230	—	90	
				4.5	—	29	46	—	58	
				6.0	—	22	36	—	46	
Output Enable time	$t_{pZL}$ $t_{pZH}$	$R_L = 1\text{k}\Omega$	50	2.0	—	60	130	—	165	
				4.5	—	17	26	—	33	
				6.0	—	13	22	—	28	
			150	2.0	—	78	170	—	215	
				4.5	—	23	34	—	43	
				6.0	—	17	29	—	36	
Output Disable time	$t_{pLZ}$ $t_{pHZ}$	$R_L = 1\text{k}\Omega$	50	2.0	—	54	150	—	190	
				4.5	—	19	30	—	38	
				6.0	—	16	26	—	33	
Maximum Clock Frequency	$f_{\text{MAX}}$		50	2.0	6	12	—	5	MHz	
				4.5	30	58	—	24		
				6.0	35	80	—	28		
Input Capacitance	$C_{\text{IN}}$				—	5	10	—	pF	
Output Capacitance	$C_{\text{OUT}}$				—	13	—	—		
Power Dissipation Capacitance	$C_{\text{PD}}(1)$				—	170	—	—		

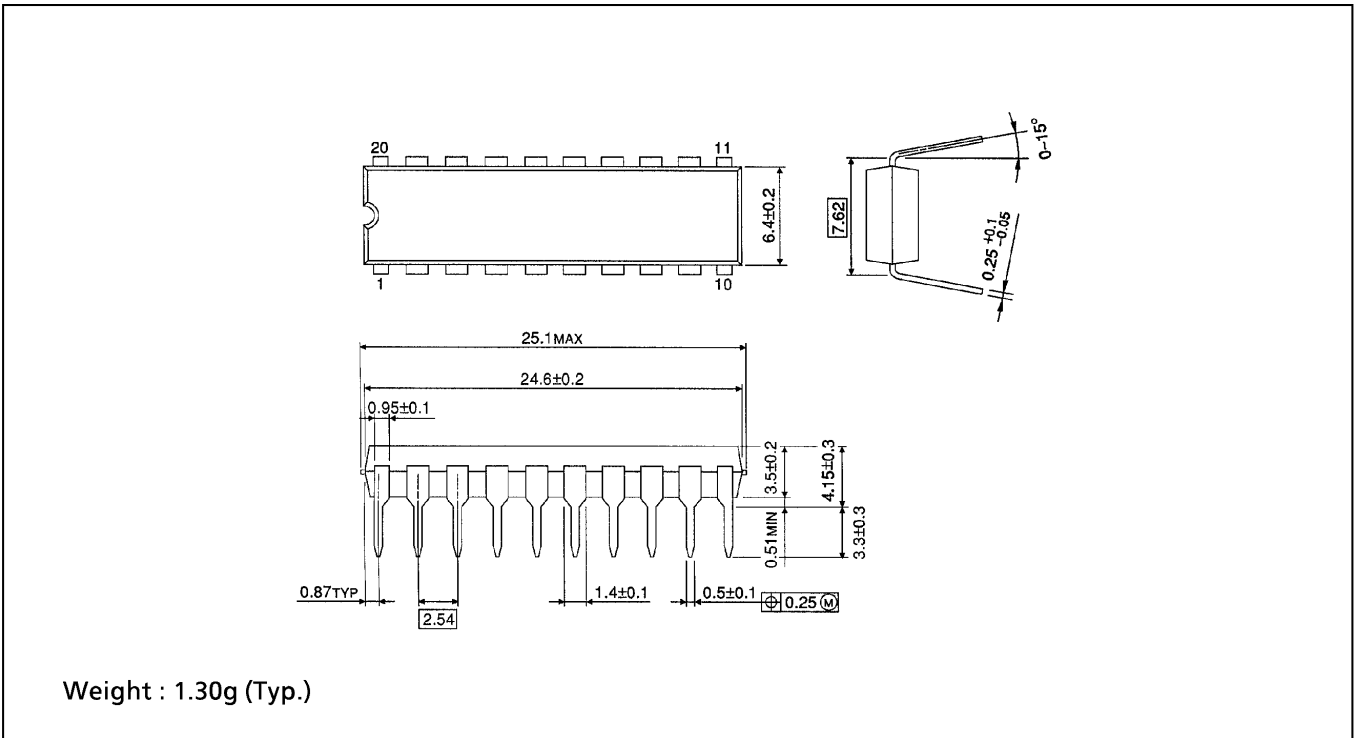
Note (1)  $C_{\text{PD}}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)

Unit in mm



SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)

Unit in mm

