High Performance
256K×16
CMOS DRAM

AS4C256K16E0

# 256K×16 CMOS EDO DRAM

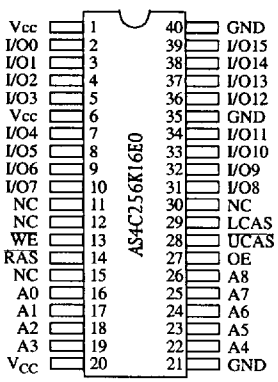
Preliminary information

## Features

- Organization: 262,144 words × 16 bits
- High speed
  - 45/50/60 ns $\overline{RAS}$ access time
  - 17/20/25 ns hyper page cycle time
  - 13/14/15 ns $\overline{CAS}$ access time
- Low power consumption
  - Active: 825 mW max (4C256K16E0-45)
  - Standby: 5.5 mW max, CMOS I/O
- Extended data out
- 512 refresh cycles, 8 ms refresh interval
  - $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh
- Read-modify-write
- TTL-compatible, three-state I/O
- JEDEC standard package and pinout
  - 400 mil, 40-pin SOJ
- 5V power supply

## Pin arrangement

SOJ




## Pin designation

| Pin(s) | Description |
|---|---|
| A0 to A8 | Address inputs |
| $\overline{RAS}$ | Row address strobe |
| I/O0 to I/O15 | Input/output |
| $\overline{OE}$ | Output enable |
| $\overline{WE}$ | Write enable |
| $\overline{UCAS}$ | Column address strobe, upper byte |
| $\overline{LCAS}$ | Column address strobe, lower byte |
| $V_{CC}$ | Power |
| GND | Ground |

## Selection guide

| | Symbol | 4C256K16E0-45 | 4C256K16E0-50 | 4C256K16E0-60 | Unit |
|---|---|---|---|---|---|
| Maximum $\overline{RAS}$ access time | $t_{RAC}$ | 45 | 50 | 60 | ns |
| Maximum column address access time | $t_{AA}$ | 21 | 25 | 30 | ns |
| Maximum $\overline{CAS}$ access time | $t_{CAC}$ | 13 | 14 | 15 | ns |
| Maximum output enable ($\overline{OE}$) access time | $t_{OEA}$ | 12 | 13 | 15 | ns |
| Minimum read or write cycle time | $t_{RC}$ | 74 | 84 | 104 | ns |
| Minimum hyper page mode cycle time | $t_{HPC}$ | 17 | 20 | 25 | ns |
| Maximum operating current | $I_{CC1}$ | 150 | 130 | 110 | mA |
| Maximum CMOS standby current | $I_{CC5}$ | 1.0 | 1.0 | 1.0 | mA |

## Functional description

The AS4C256K16E0 is a high performance 4-megabit CMOS Dynamic Random Access Memory (DRAM) organized as 262,144 words × 16 bits. The AS4C256K16E0 is fabricated using advanced CMOS technology and innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels. The Alliance 4Mb DRAM family is optimized for use as graphics memory in personal and portable PCs, and multimedia applications.

The AS4C256K16E0 features a high speed page mode operation where read and write operations within a single row (or page) can be executed at very high speed by toggling column addresses within that row. Row and column addresses are alternately latched into input buffers using the falling edge of $\overline{RAS}$ and $\overline{xCAS}$ inputs respectively. Also, $\overline{RAS}$ is used to make the column address latch transparent, enabling application of column addresses prior to $\overline{xCAS}$ assertion. The AS4C256K16E0 provides dual $\overline{UCAS}$ and $\overline{LCAS}$ for independent byte control of read and write access.

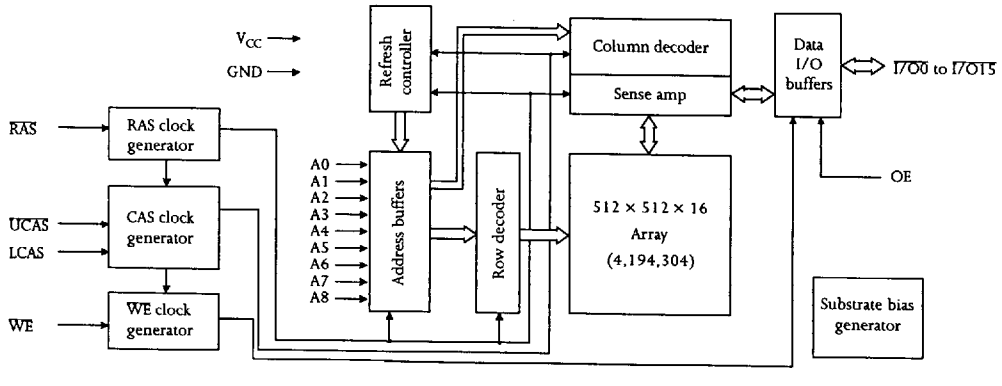
Extended data out (EDO) read mode enables high speed operation. In contrast to 'fast page mode' devices, data remains active on outputs after $\overline{xCAS}$ is de-asserted high, giving system logic more time to latch the data. Use $\overline{OE}$ and $\overline{WE}$ to control output impedance and prevent bus contention during read-modify-write and shared bus applications. Outputs also go to high impedance at the last occurrance of $\overline{RAS}$ and $\overline{xCAS}$ going high.

Refresh on the 512 address combinations of A0 to A8 must be performed every 8 ms using:

- RAS-only refresh: RAS is asserted while xCAS is held high. Each of the 512 rows must be strobed. Outputs remain high impedence.
- Hidden refresh: $\overline{xCAS}$ is held low while $\overline{RAS}$ is toggled. Outputs remain low impedence with previous valid data.
- CAS-before-RAS refresh (CBR): At least one xCAS is asserted prior to RAS. Refresh address is generated internally. Outputs are high-impedence ($\overline{OE}$ and $\overline{WE}$ are don't care).
- Normal read or write cycles refresh the row being accessed.

The AS4C256K16E0 is available in the standard 40-pin plastic SOJ package. The AS4C256K16E0 device operates with a single power supply of 5V ± 0.5V. Both provide TTL compatible inputs and outputs.

## Logic block diagram




## Recommended operating conditions

| Parameter | | Symbol | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | 4C256K16E0 | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | | GND | 0.0 | 0.0 | 0.0 | V |
| Input voltage | 4C256K16E0 | $V_{IH}$ | 2.4 | – | $V_{CC}$ | V |
| | | $V_{IL}$ | −0.5† | – | 0.8 | V |
| Ambient operating temperature | | $T_A$ | 0 | | 70 | °C |

†$V_{IL}$ min -3.0V for pulse widths less than 5 ns.

Recommended operating conditions apply throughout this document unlesss otherwise specified.

## Absolute maximum ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input voltage | $V_{in}$ | -1.0 | +7.0 | V |
| Input voltage (I/Os) | $V_{I/O}$ | -1.0 | $V_{CC}$ + 0.5 | V |
| Power supply voltage | $V_{CC}$ | -1.0 | +7.0 | V |
| Storage temperature (plastic) | $T_{STG}$ | -55 | +150 | °C |
| Soldering temperature × time | $T_{SOLDER}$ | – | 260 × 10 | °C × sec |
| Power dissipation | $P_D$ | – | 1 | W |
| Short circuit output current | $I_{out}$ | – | 50 | mA |

## DC electrical characteristics

| | | | -45 | | -50 | | -60 | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Test conditions | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Input leakage current | $I_{IL}$ | $0V \le V_{in} \le +5.5V$, Pins not under test = 0V | -5 | +5 | -5 | +5 | -5 | +5 | µA | |
| Output leakage current | $I_{OL}$ | $D_{OUT}$ disabled, $0V \le V_{out} \le +5.5V$ | -5 | +5 | -5 | +5 | -5 | +5 | µA | |
| Operating power supply current | $I_{CC1}$ | $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling; $t_{RC}$=min | – | 150 | – | 130 | – | 110 | mA | 1,2 |
| TTL standby power supply current | $I_{CC2}$ | $\overline{RAS} = \overline{UCAS} = \overline{LCAS} \ge V_{IH}$ | – | 2.0 | – | 2.0 | – | 2.0 | mA | |
| Average power supply current, $\overline{RAS}$ refresh mode | $I_{CC3}$ | $\overline{RAS}$ cycling, $\overline{UCAS} = \overline{LCAS} \ge V_{IH}$, $t_{RC}$ = min | – | 150 | – | 130 | – | 110 | mA | 1 |
| Hyper page mode average power supply current | $I_{CC4}$ | $\overline{RAS} = V_{IL}$, $\overline{UCAS}$ or $\overline{LCAS}$, address cycling: $t_{HPC}$ = min | – | 125 | – | 120 | – | 100 | mA | 1, 2 |
| CMOS standby power supply current | $I_{CC5}$ | $\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{CC}$ - 0.2V | – | 1.0 | – | 1.0 | – | 1.0 | mA | |
| Output voltage | $V_{OH}$ | $I_{OUT}$ = -5.0 mA | 2.4 | – | 2.4 | – | 2.4 | – | V | |
| | $V_{OL}$ | $I_{OUT}$ = 4.2 mA | – | 0.4 | – | 0.4 | – | 0.4 | V | |
| $\overline{CAS}$ before $\overline{RAS}$ refresh current | $I_{CC6}$ | $\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling, $t_{RC}$ = min of $\overline{RAS}$ low after $\overline{XCAS}$ low. | – | 150 | – | 130 | – | 110 | mA | |

## AC parameters common to all waveforms

| | | -45 | | -50 | | -60 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Unit | Notes |
| $t_{RC}$ | Random read or write cycle time | 74 | – | 84 | – | 104 | – | ns | |
| $t_{RP}$ | $\overline{RAS}$ precharge time | 25 | – | 30 | – | 40 | – | ns | |
| $t_{RAS}$ | $\overline{RAS}$ pulse width | 45 | 10K | 50 | 10K | 60 | 10K | ns | |
| $t_{CAS}$ | $\overline{CAS}$ pulse width | 7 | 10K | 8 | 10K | 10 | 10K | ns | |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ delay time | 14 | 31 | 15 | 35 | 15 | 43 | ns | 6 |
| $t_{RAD}$ | $\overline{RAS}$ to column address delay time | 9 | 22 | 10 | 25 | 12 | 30 | ns | 7 |
| $t_{RSH}$ | $\overline{CAS}$ to $\overline{RAS}$ hold time | 8 | – | 10 | – | 10 | – | ns | |
| $t_{CSH}$ | $\overline{RAS}$ to $\overline{CAS}$ hold time | 35 | – | 40 | – | 40 | – | ns | |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ precharge time | 5 | – | 5 | – | 5 | – | ns | |
| $t_{ASR}$ | Row address setup time | 0 | – | 0 | – | 0 | – | ns | |
| $t_{RAH}$ | Row address hold time | 7 | – | 8 | – | 10 | – | ns | |
| $t_T$ | Transition time (rise and fall) | 2 | 50 | 2 | 50 | 2 | 50 | ns | 4,5 |
| $t_{REF}$ | Refresh period | – | 8 | – | 8 | – | 8 | ms | 3 |
| $t_{CP}$ | CAS precharge time | 7 | – | 8 | – | 10 | – | ns | |
| $t_{RAL}$ | Column address to $\overline{RAS}$ lead time | 23 | – | 25 | – | 30 | – | ns | |
| $t_{ASC}$ | Column address setup time | 0 | – | 0 | – | 0 | – | ns | |
| $t_{CAH}$ | Column address hold time | 7 | | 8 | | 10 | | ns | |

## Read cycle

| | | -45 | | -50 | | -60 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Unit | Notes |
| $t_{RAC}$ | Access time from $\overline{RAS}$ | – | 45 | – | 50 | – | 60 | ns | 6 |
| $t_{CAC}$ | Access time from $\overline{CAS}$ | – | 13 | – | 14 | – | 15 | ns | 6,13 |
| $t_{AA}$ | Access time from address | – | 22 | – | 25 | – | 30 | ns | 7,13 |
| $t_{RCS}$ | Read command setup time | 0 | – | 0 | – | 0 | – | ns | |
| $t_{RCH}$ | Read command hold time to $\overline{CAS}$ | 0 | – | 0 | – | 0 | – | ns | 9 |
| $t_{RRH}$ | Read command hold time to $\overline{RAS}$ | 0 | – | 0 | – | 0 | – | ns | 9 |

## Write cycle

| | | -45 | | -50 | | -60 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Unit | Notes |
| $t_{WCS}$ | Write command setup time | 0 | – | 0 | – | 0 | – | ns | 11 |
| $t_{WCH}$ | Write command hold time | 7 | – | 8 | – | 10 | – | ns | 11 |
| $t_{WP}$ | Write command pulse width | 7 | – | 8 | – | 10 | – | ns | |
| $t_{RWL}$ | Write command to $\overline{RAS}$ lead time | 8 | – | 10 | – | 12 | – | ns | |
| $t_{CWL}$ | Write command to $\overline{CAS}$ lead time | 7 | – | 8 | – | 10 | – | ns | |
| $t_{DS}$ | Data-in setup time | 0 | – | 0 | – | 0 | – | ns | 12 |
| $t_{DH}$ | Data-in hold time | 7 | – | 8 | – | 10 | – | ns | 12 |

## Read-modify-write cycle

| | | -45 | | -50 | | -60 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Unit | Notes |
| $t_{RWC}$ | Read-write cycle time | 105 | – | 113 | – | 137 | – | ns | |
| $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ delay time | 61 | – | 67 | – | 77 | – | ns | 11 |
| $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ delay time | 30 | – | 31 | – | 32 | – | ns | 11 |
| $t_{AWD}$ | Column address to $\overline{WE}$ delay time | 38 | – | 42 | – | 47 | – | ns | 11 |

## Refresh cycle

| | | -45 | | -50 | | -60 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Unit | Notes |
| $t_{CSR}$ | $\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$) | 5 | – | 5 | – | 5 | – | ns | 3 |
| $t_{CHR}$ | $\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$) | 8 | – | 8 | – | 10 | – | ns | 3 |
| $t_{RPC}$ | $\overline{RAS}$ precharge to $\overline{CAS}$ hold time | 0 | – | 0 | – | 0 | – | ns | |
| $t_{CPT}$ | $\overline{CAS}$ precharge time (CBR counter test) | 10 | | 10 | | 10 | | ns | |

## Hyper page mode cycle

| Symbol | Parameter | -45 Min | -45 Max | -50 Min | -50 Max | -60 Min | -60 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| $t_{CPWD}$ | $\overline{CAS}$ precharge to $\overline{WE}$ delay time | 41 | – | 45 | – | 52 | – | ns | |
| $t_{CPA}$ | Access time from $\overline{CAS}$ precharge | – | 25 | – | 28 | – | 35 | ns | 13 |
| $t_{RASP}$ | $\overline{RAS}$ pulse width | 45 | 100K | 50 | 100K | 60 | 100K | ns | |
| $t_{DOH}$ | Previous data hold time from CAS | 3 | – | 3 | – | 5 | – | ns | |
| $t_{REZ}$ | Output buffer turn off delay from $\overline{RAS}$ | 0 | 13 | 0 | 13 | 0 | 13 | ns | |
| $t_{WEZ}$ | Output buffer turn off delay from $\overline{WE}$ | 0 | 13 | 0 | 13 | 0 | 13 | ns | |
| $t_{OEZ}$ | Output buffer turn off delay from $\overline{OE}$ | 0 | 13 | 0 | 13 | 0 | 13 | ns | |
| $t_{HPC}$ | Hyper page mode cycle time | 17 | – | 20 | – | 25 | – | ns | |
| $t_{HPRWC}$ | Hyper page mode RMW cycle | 52 | – | 57 | – | 66 | – | ns | |
| $t_{RHCP}$ | $\overline{RAS}$ hold time from $\overline{CAS}$ | 26 | – | 28 | – | 35 | – | ns | |

## Output enable

| Symbol | Parameter | -45 Min | -45 Max | -50 Min | -50 Max | -60 Min | -60 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| $t_{CLZ}$ | $\overline{CAS}$ to output in Low Z | 0 | – | 0 | – | 0 | – | ns | 8 |
| $t_{ROH}$ | $\overline{RAS}$ hold time referenced to $\overline{OE}$ | 8 | – | 8 | – | 10 | – | ns | |
| $t_{OEA}$ | $\overline{OE}$ access time | – | 13 | – | 13 | – | 13 | ns | |
| $t_{OED}$ | $\overline{OE}$ to data delay | 13 | – | 13 | – | 13 | – | ns | |
| $t_{OEZ}$ | Output buffer turnoff delay from $\overline{OE}$ | 0 | 13 | 0 | 13 | 0 | 13 | ns | 8 |
| $t_{OEH}$ | $\overline{OE}$ command hold time | 10 | – | 10 | – | 10 | – | ns | |
| $t_{OLZ}$ | $\overline{OE}$ to output in Low Z | 0 | – | 0 | – | 0 | – | ns | |
| $t_{OFF}$ | Output buffer turn-off time | 0 | 13 | 0 | 13 | 0 | 13 | ns | 8,10 |

## Notes

1 $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, and $I_{CC6}$ are dependent on frequency.

2 $I_{CC1}$ and $I_{CC4}$ depend on output loading. Specified values are obtained with the output open.

3 An initial pause of 200 µs is required after power-up followed by any 8 RAS cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).

4 AC Characteristics assume $t_T$ = 2 ns. All AC parameters are measured with a load equivalent to two TTL loads and 100 pF, $V_{IL}$ (min) ≥ GND and $V_{IH}$ (max) ≤ $V_{CC}$.

5 $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.

6 Operation within the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.

7 Operation within the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met. $t_{RAD}$ (max) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.

8 Assumes three state test load (5 pF and a 380 Ω Thevenin equivalent).

9 Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

10 $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels. $t_{OFF}$ is referenced from rising edge of RAS or CAS, whichever occurs last.

11 $t_{WCS}$, $t_{WCH}$, $t_{RWD}$, $t_{CWD}$ and $t_{AWD}$ are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.

12 These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-write cycles.

13 Access time is determined by the longest of $t_{CAA}$ or $t_{CAC}$ or $t_{CPA}$

14 $t_{ASC} \geq t_{CP}$ to achieve $t_{PC}$ (min) and $t_{CPA}$ (max) values.

15 These parameters are sampled and not 100% tested.

16 These characteristics apply to AS4C256K16E0 5V devices.

## AC test conditions

- Access times are measured with output reference levels of $V_{OH}$ = 2.2V and $V_{OL}$ = 0.8V, $V_{IH}$ = 2.4V and $V_{IL}$ = 0.8V
- Input rise and fall times: 2 ns

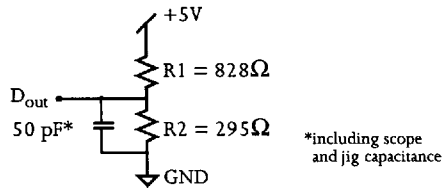
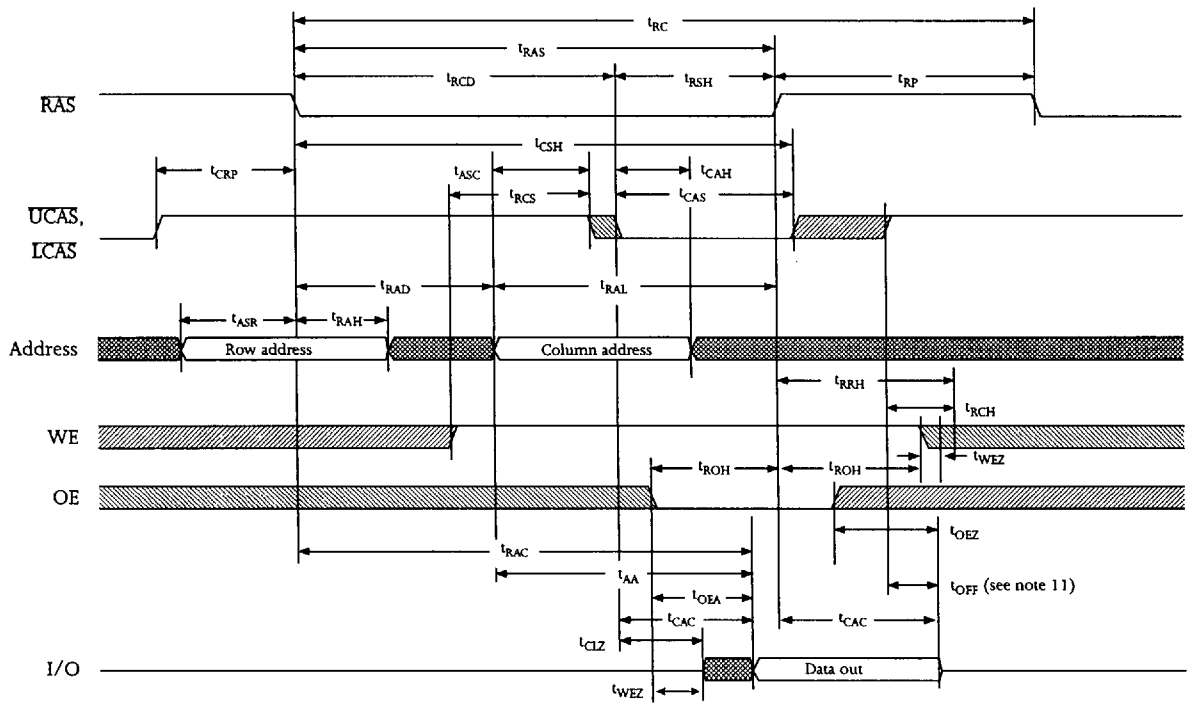



Figure A: Equivalent output load

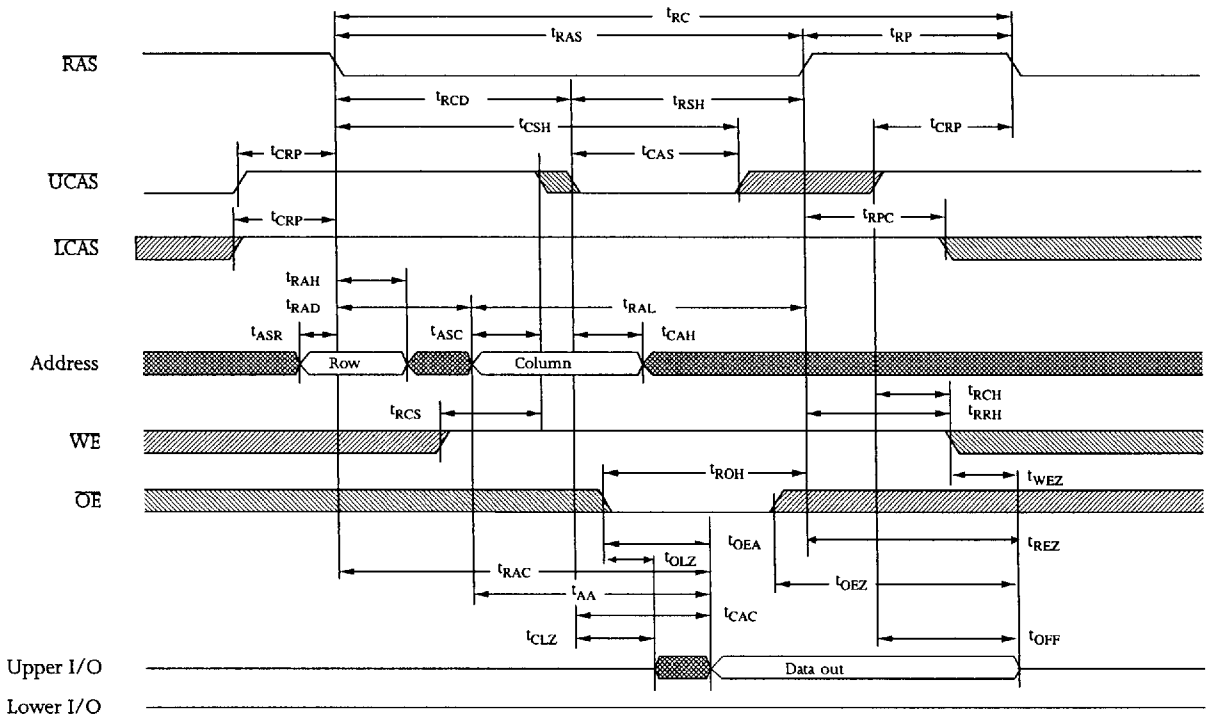
## Key to switching waveforms

Rising input  Falling input  Undefined output/don't care

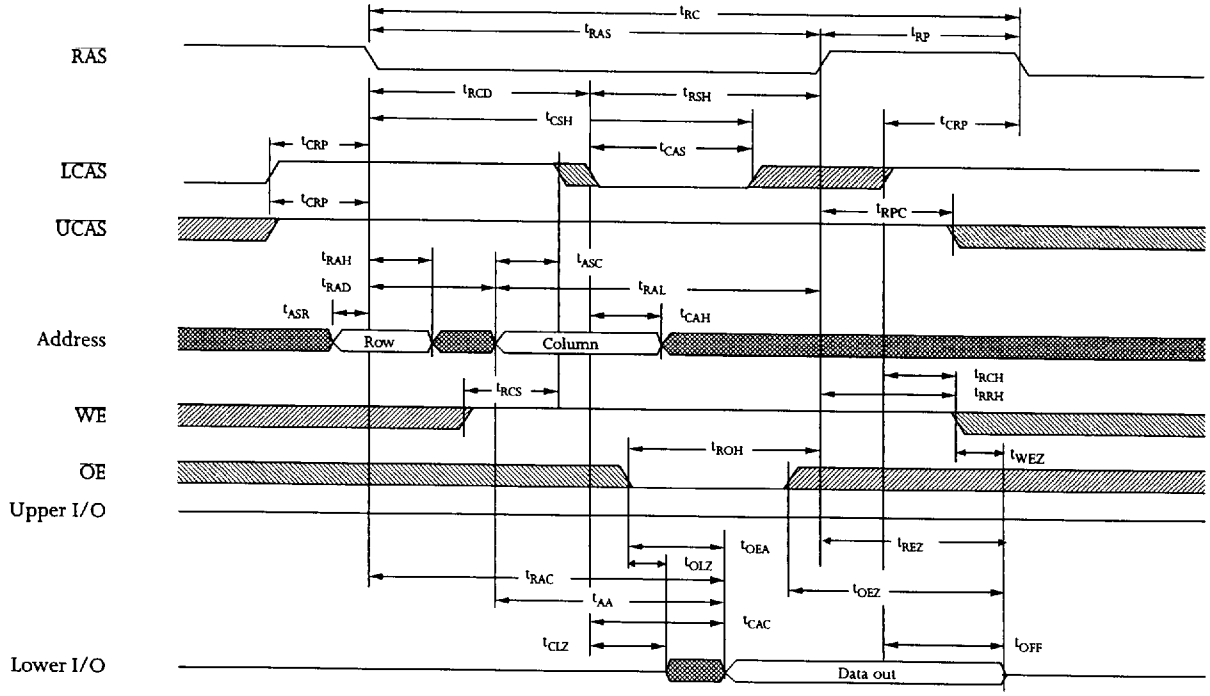
## Read waveform



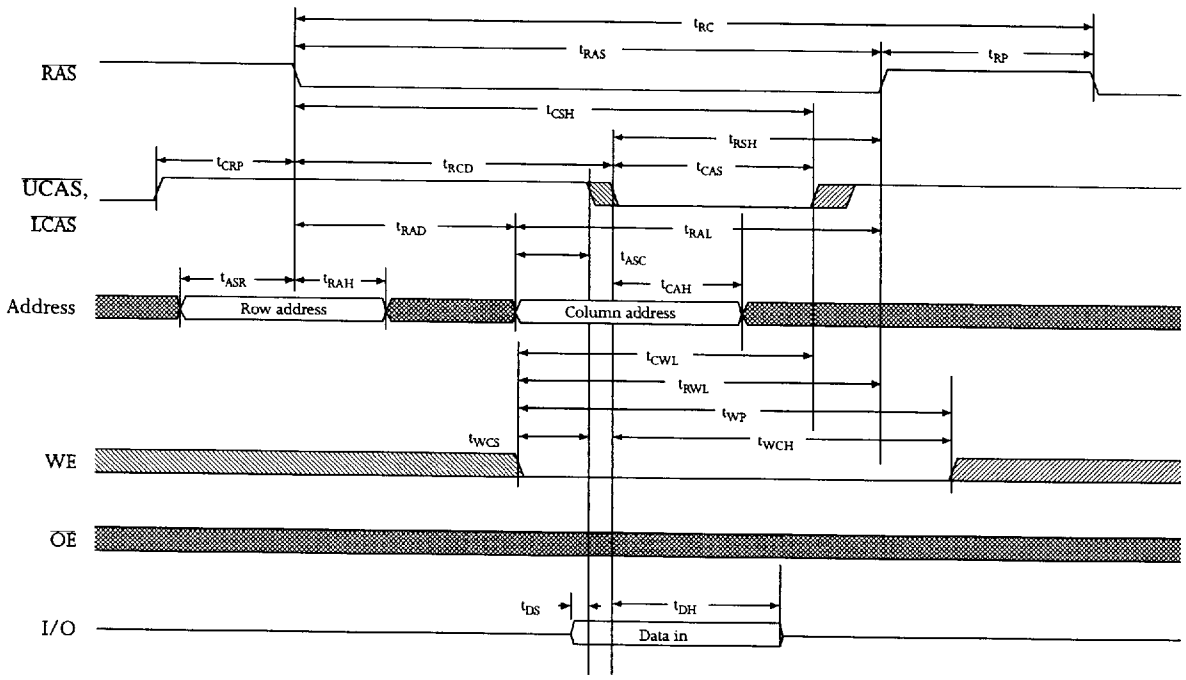

## Upper byte read waveform



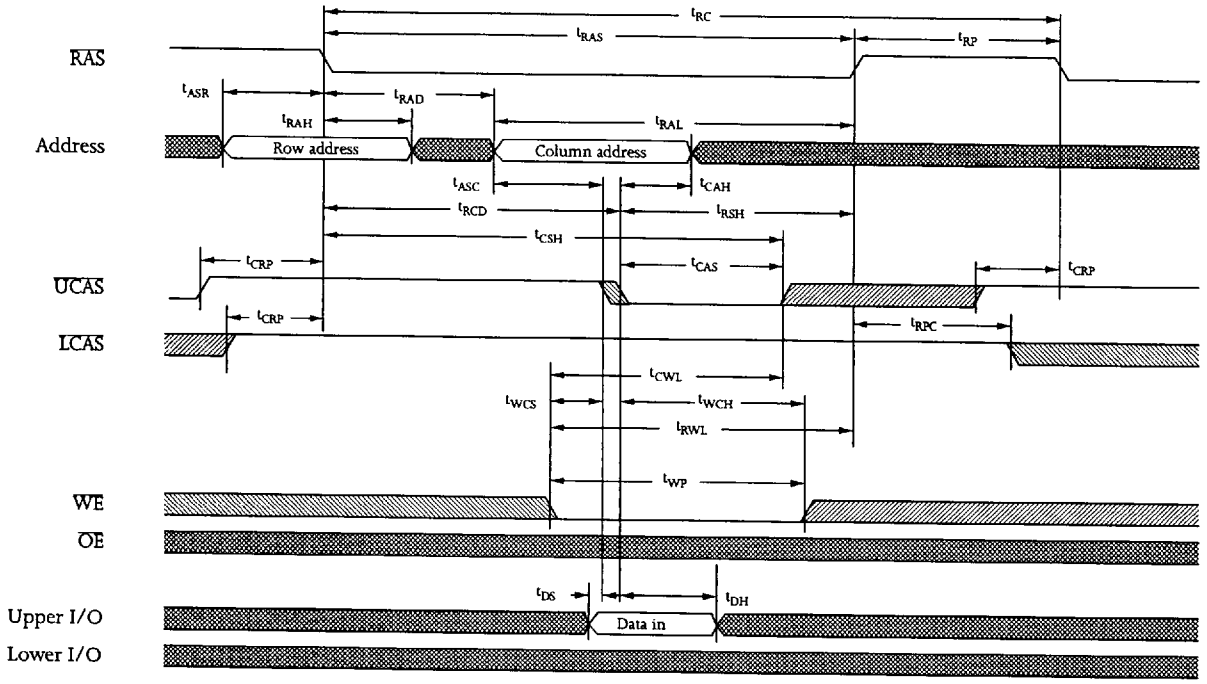
## Lower byte read waveform



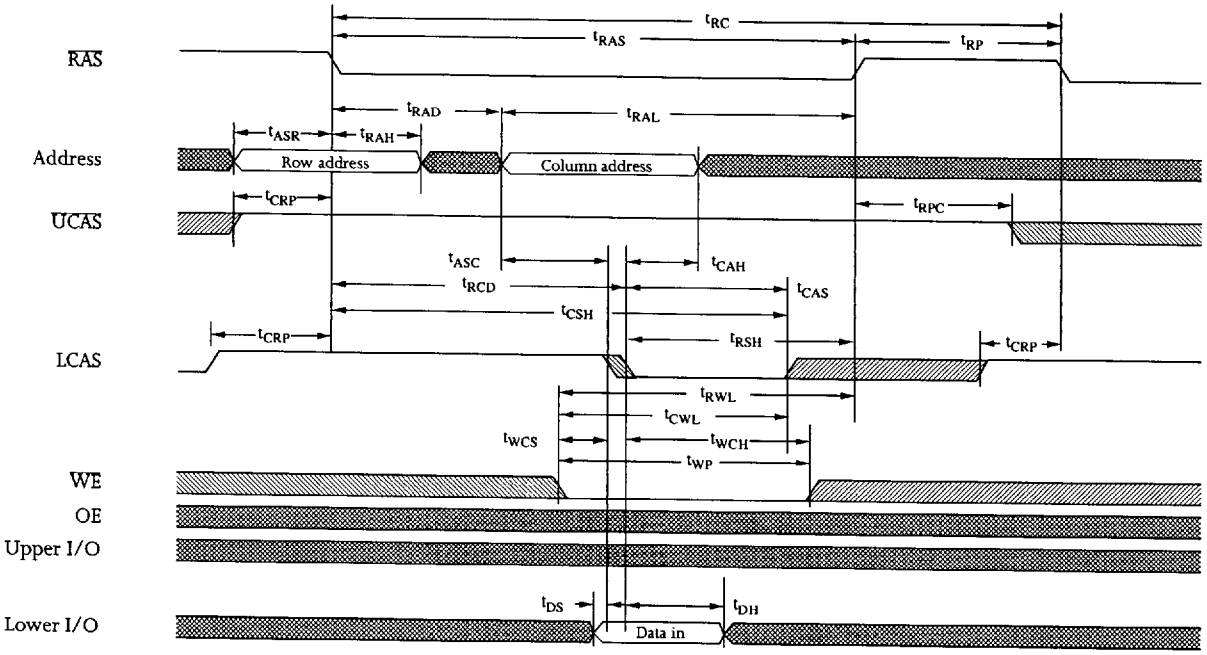

## Early write waveform



## Upper byte early write waveform

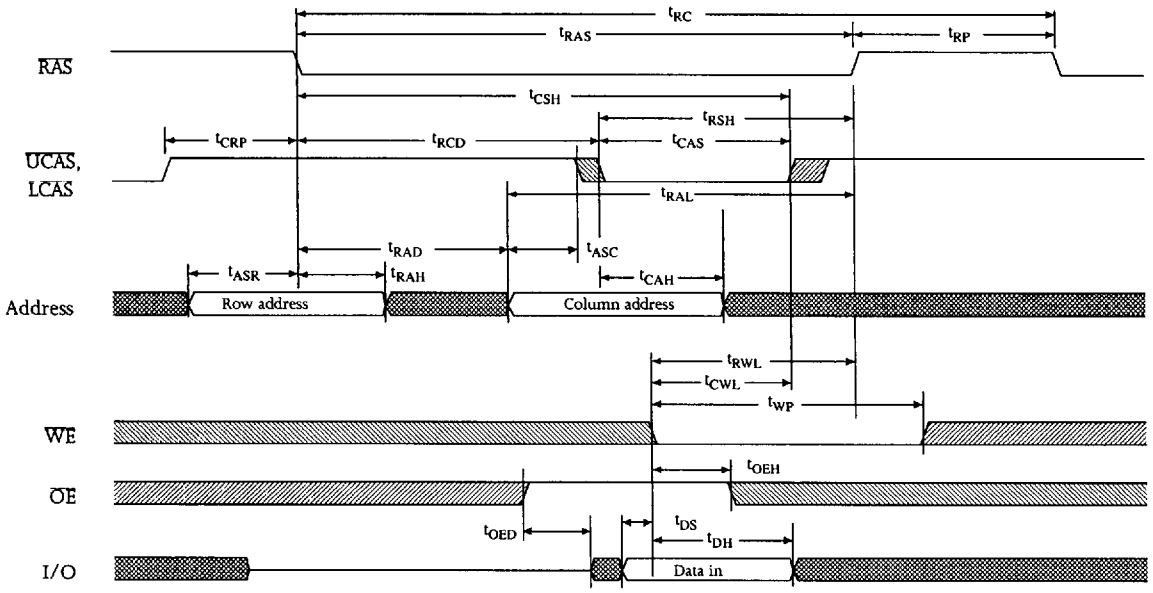



## Lower byte early write waveform



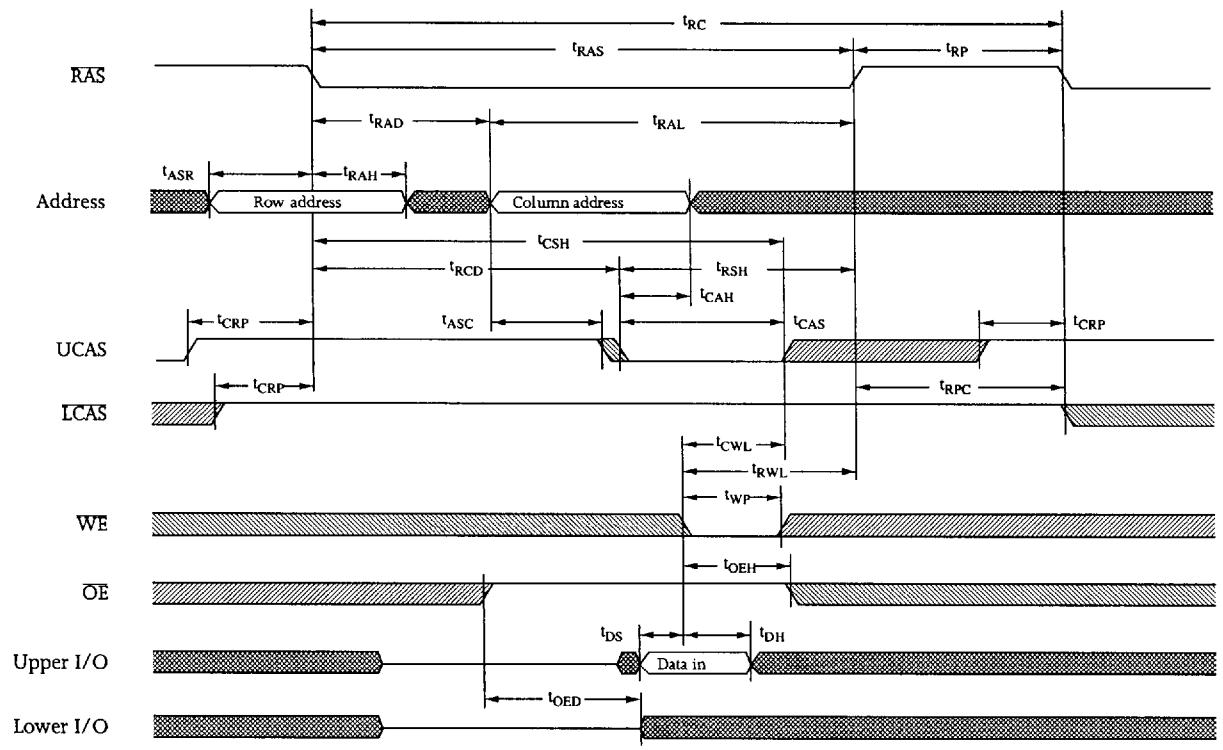
## Write waveform

$\overline{OE}$ controlled



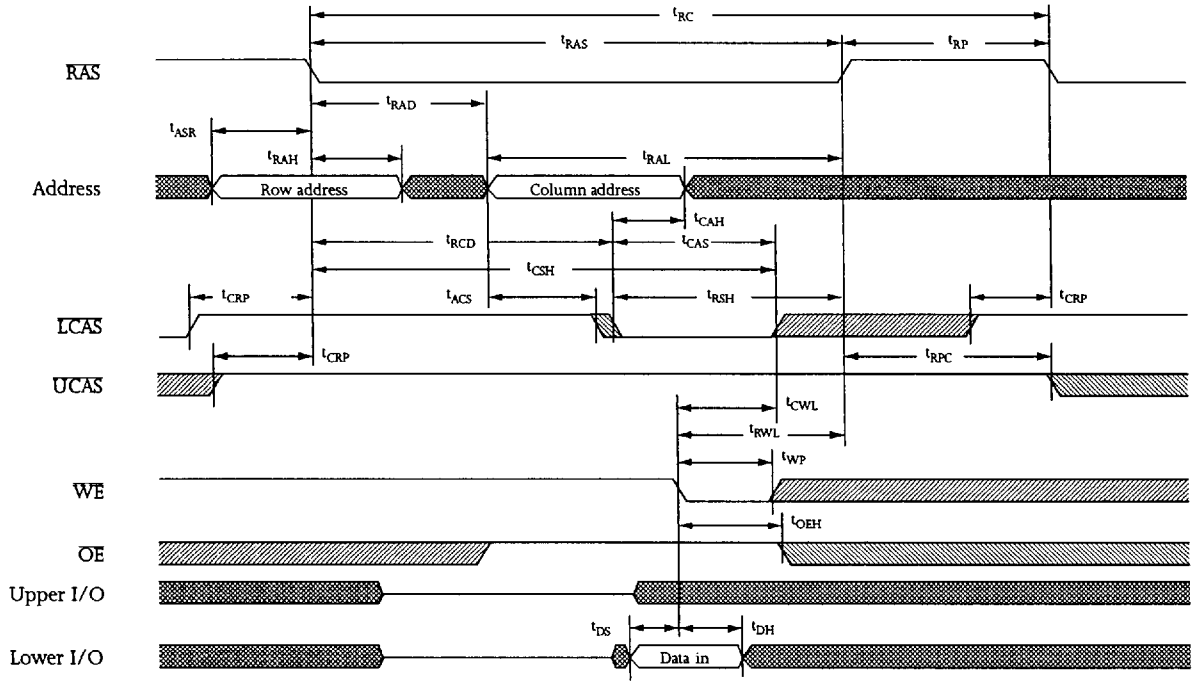

## Upper byte write waveform

$\overline{OE}$ controlled

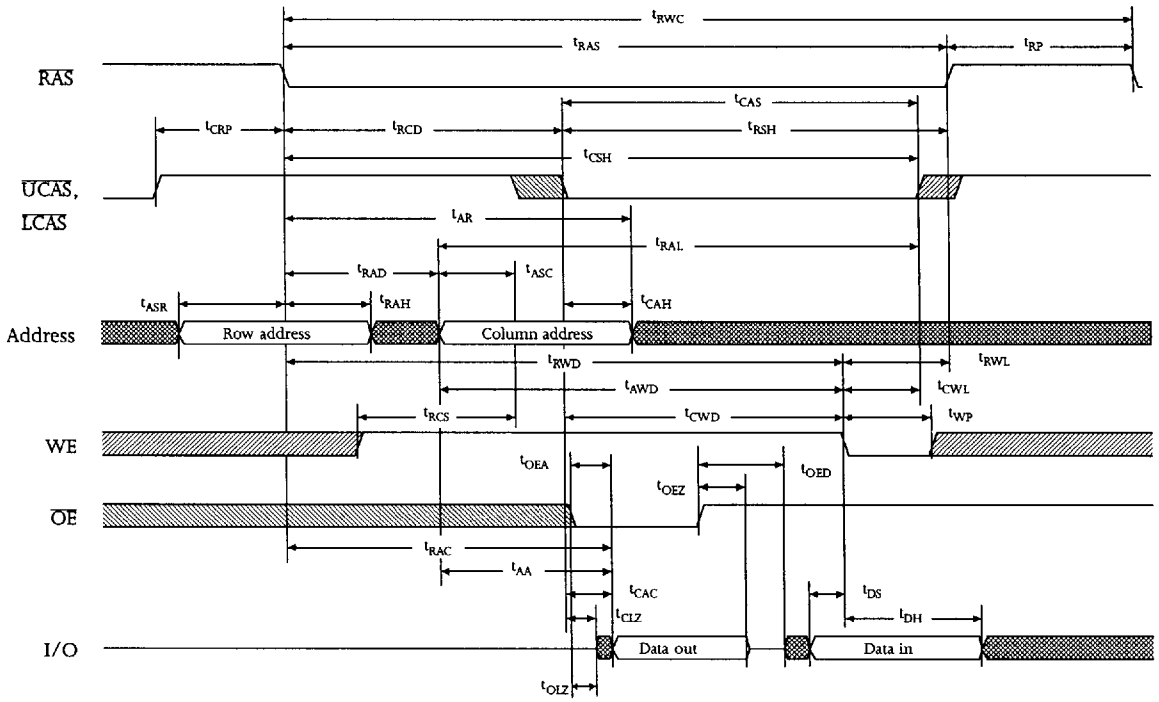


## Lower byte write waveform

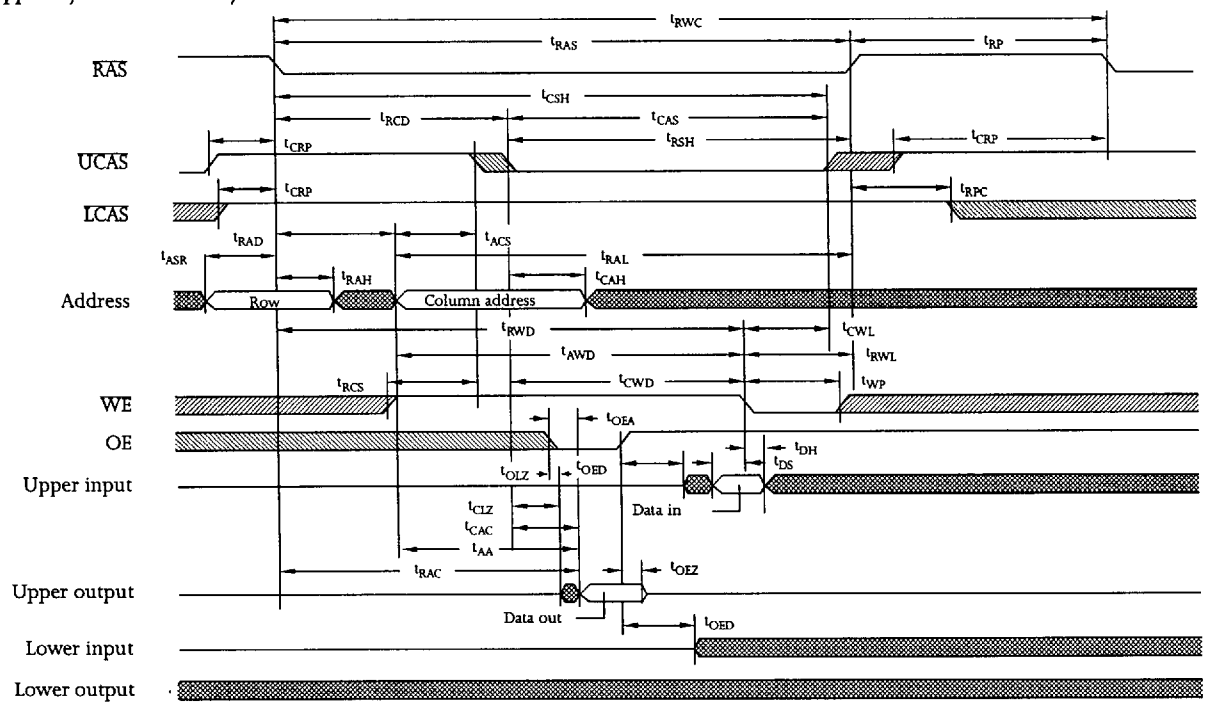
$\overline{OE}$ controlled



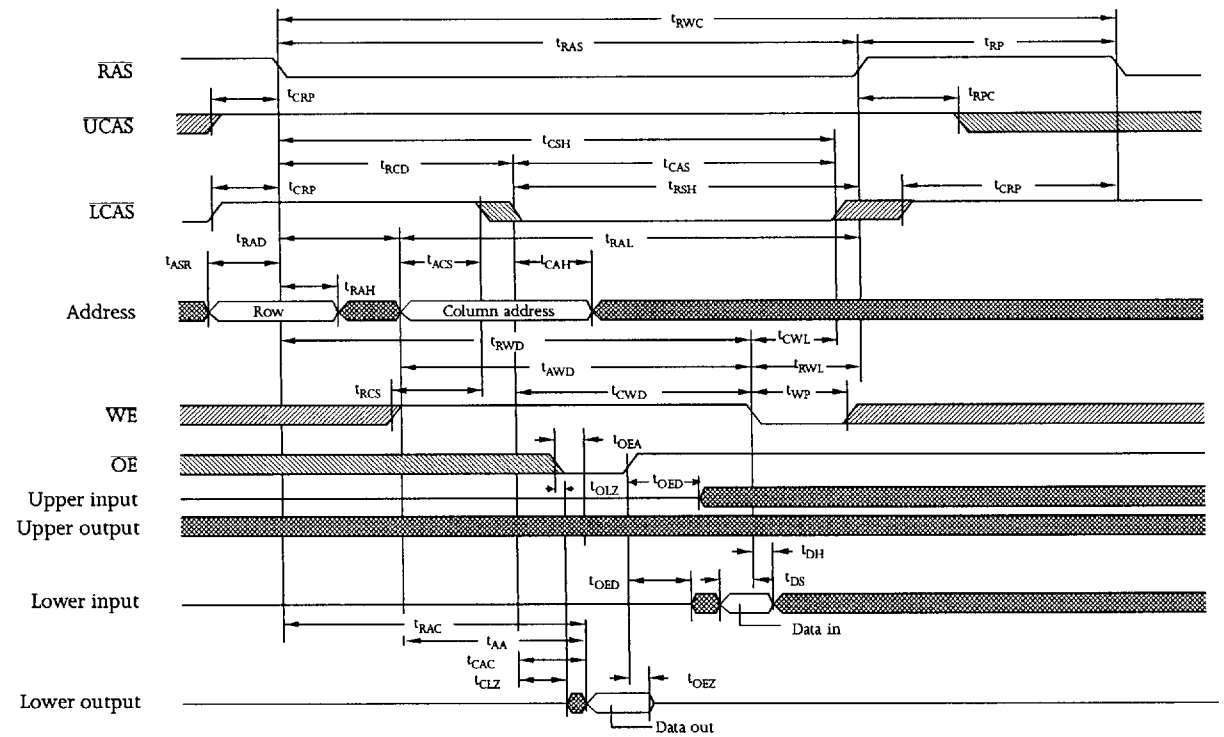

## Read-modify-write waveform



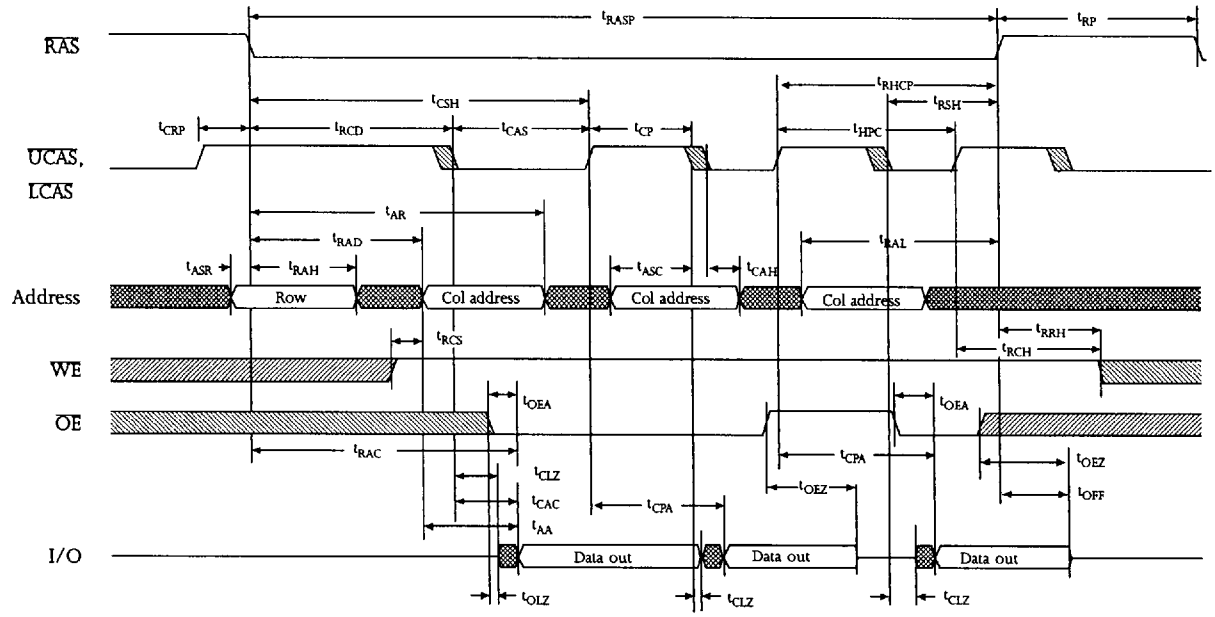
## Upper byte read-modify-write waveform



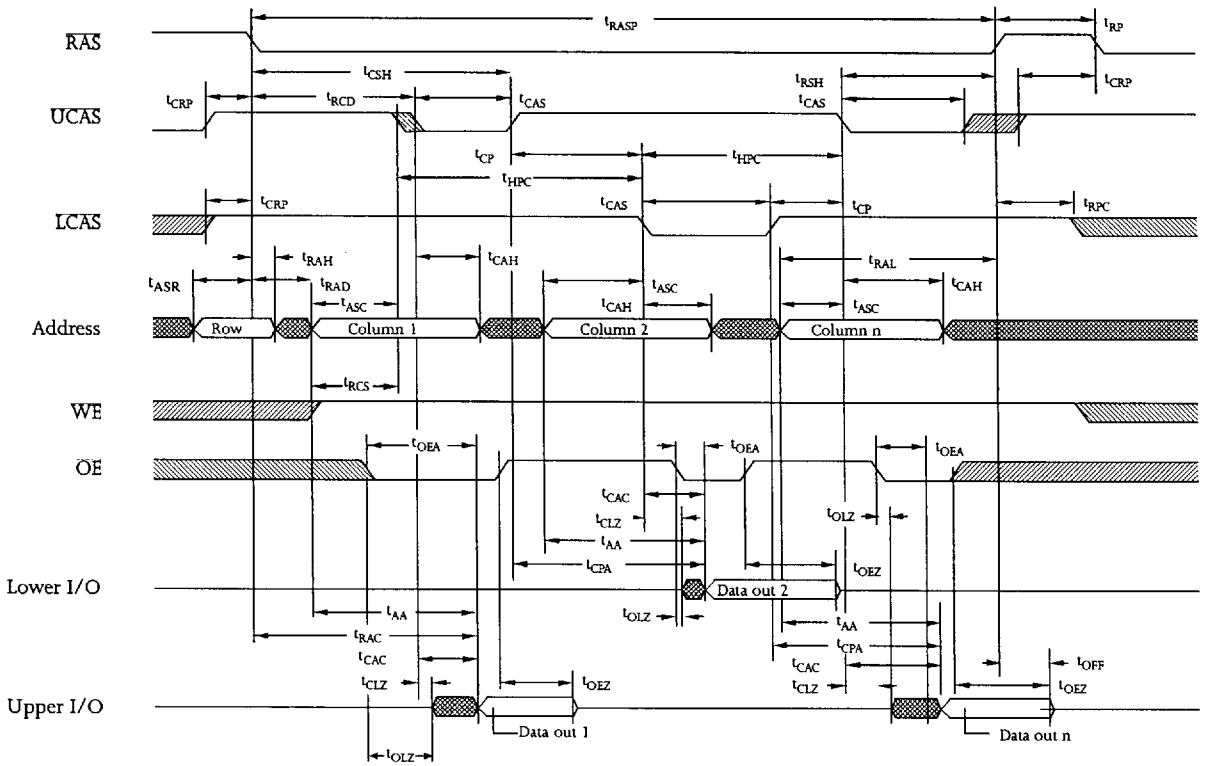

## Lower byte read-modify-write waveform



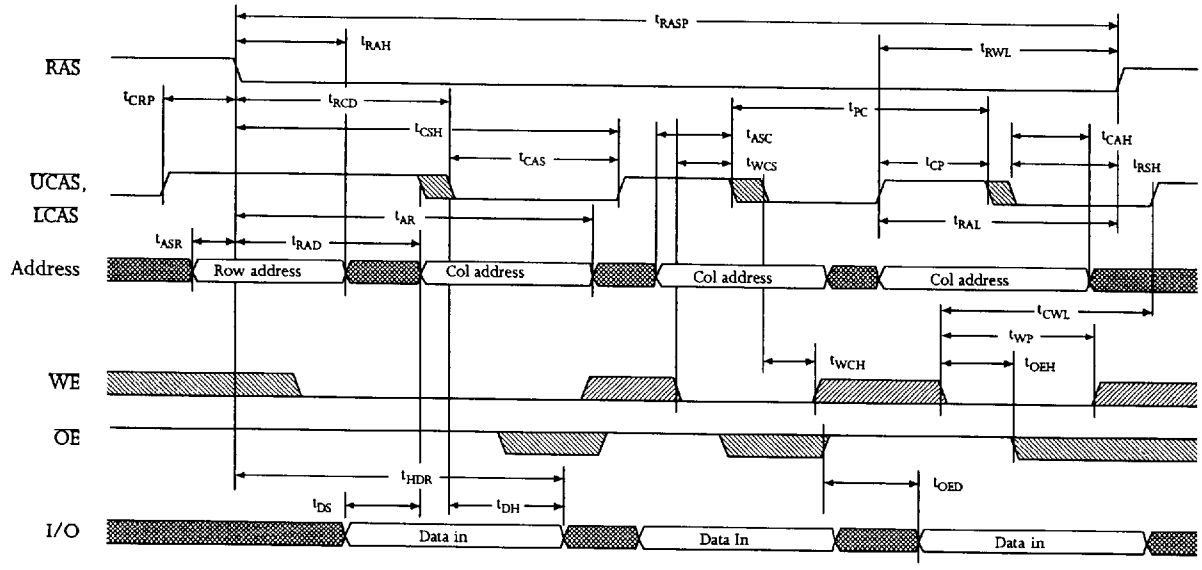
## Hyper page mode read waveform



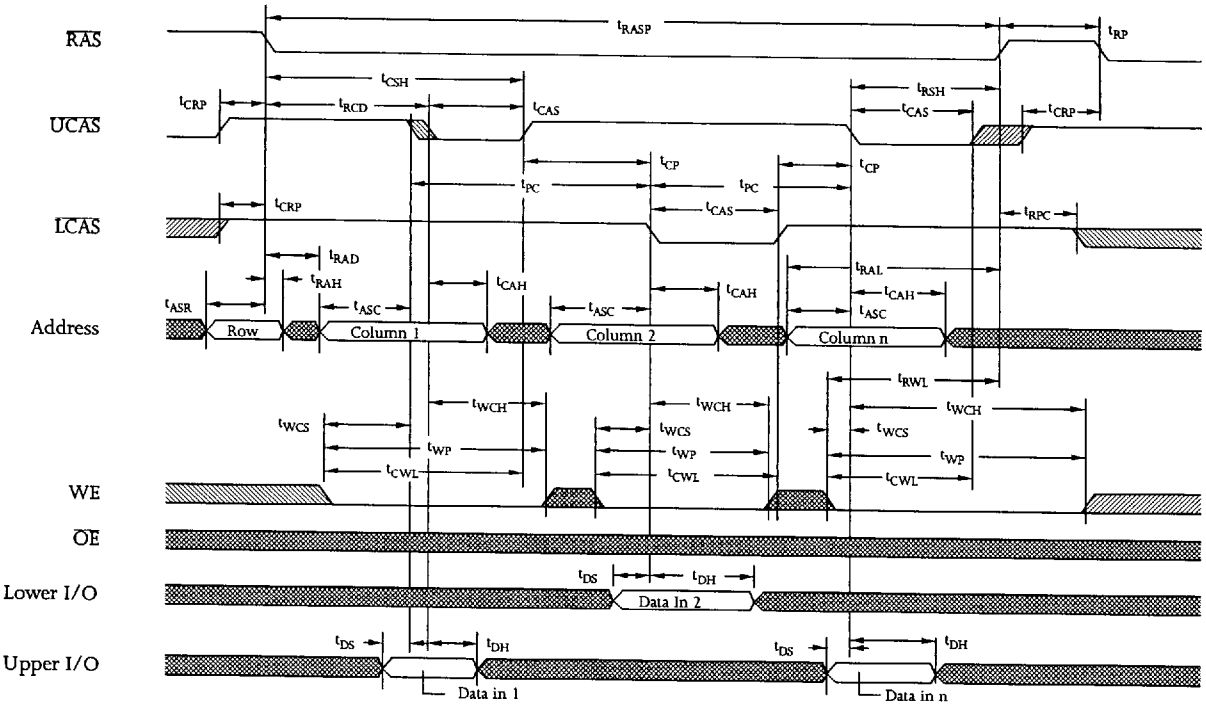

## Hyper page mode byte read waveform



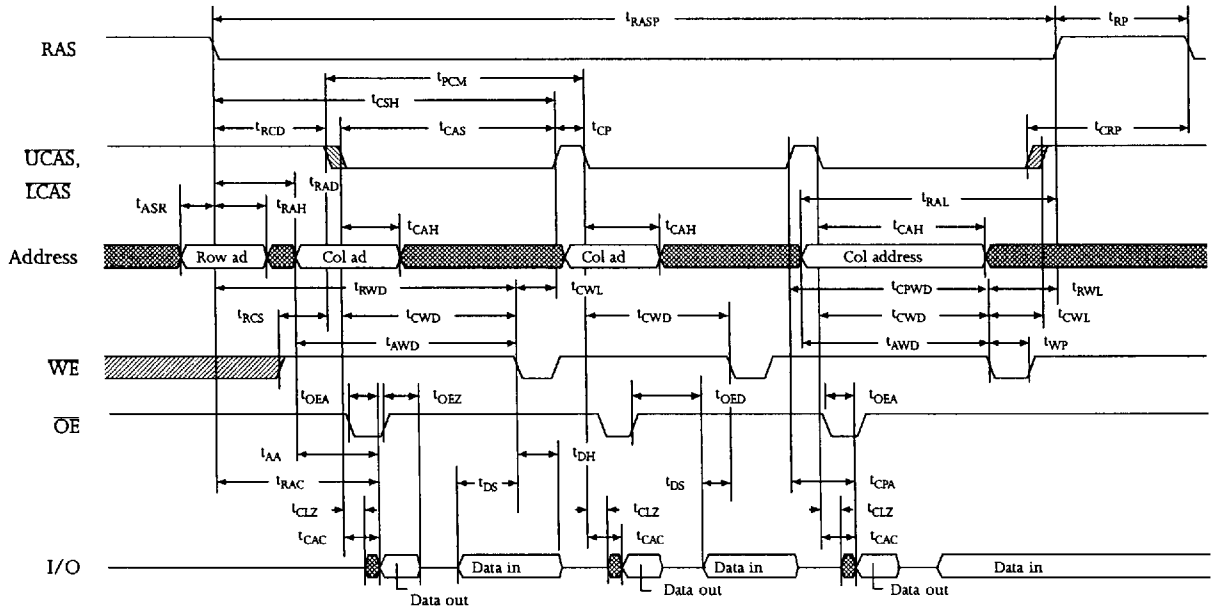
## Hyper page mode early write waveform




## Hyper page mode byte early write waveform

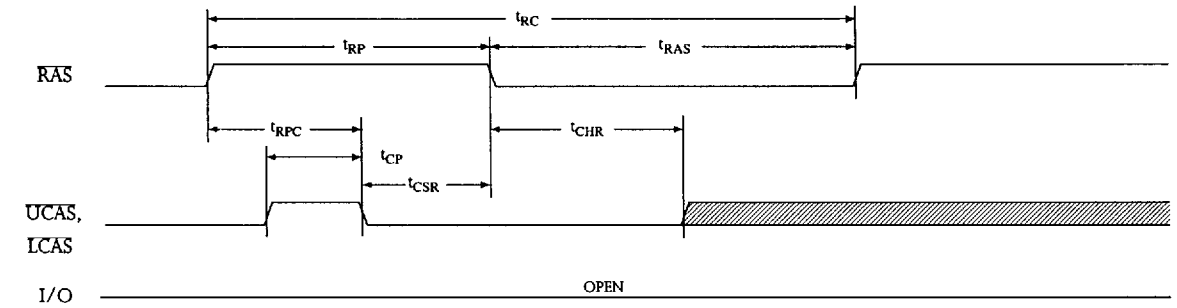


## Hyper page mode read-modify-write waveform



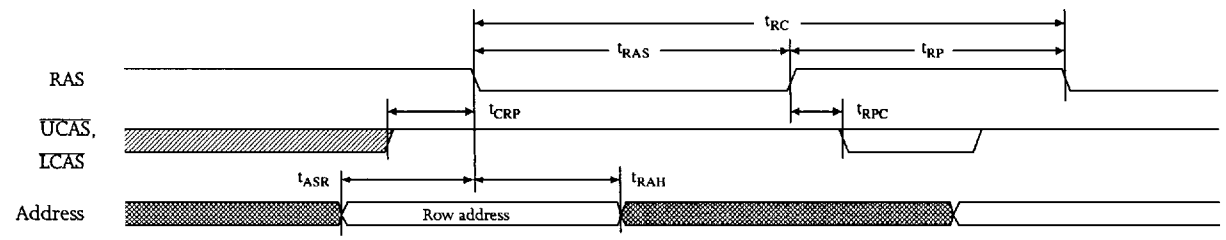

## CAS before RAS refresh waveform

$\overline{WE}$ = A = $V_{IH}$ or $V_{IL}$

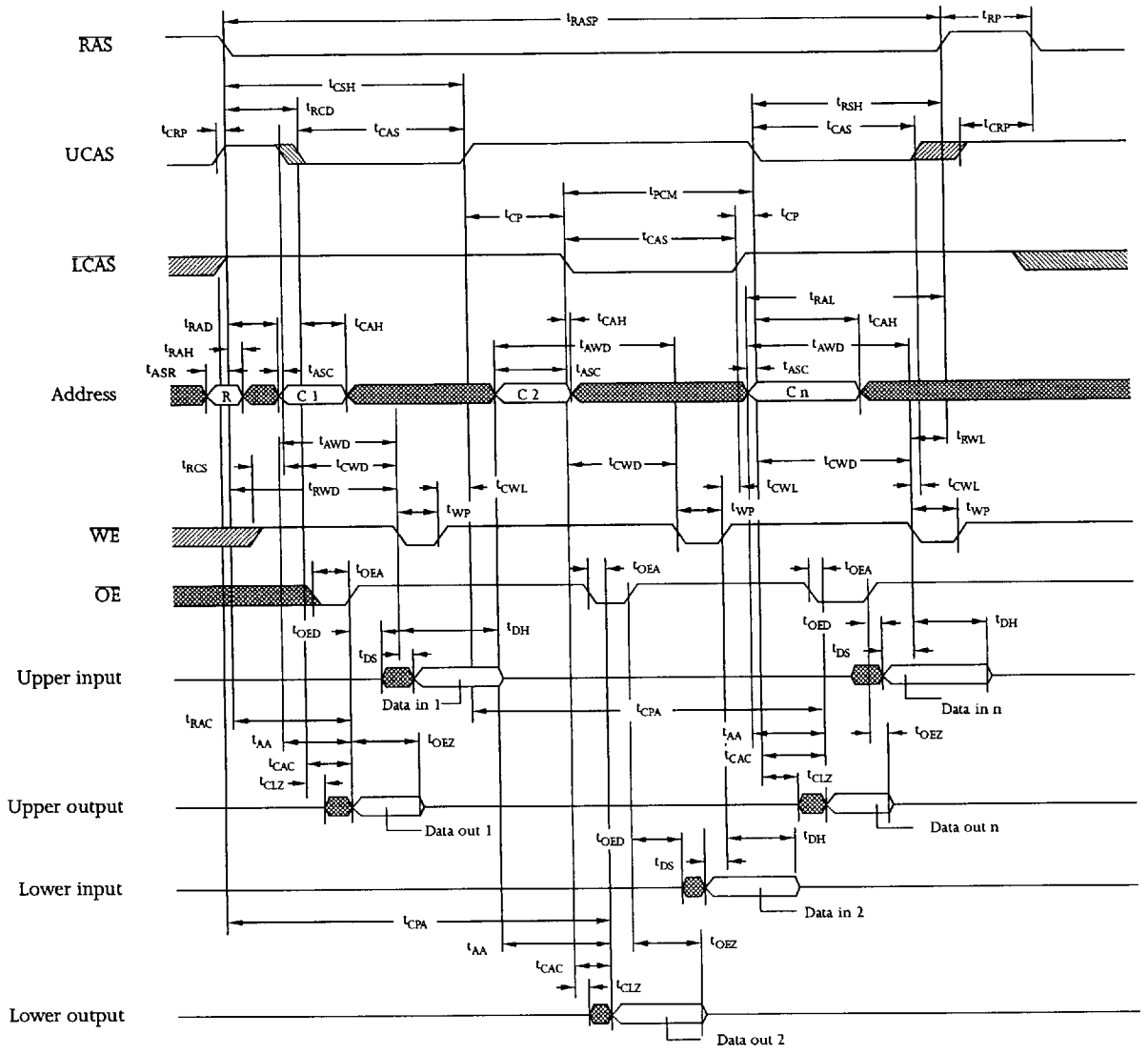



## RAS only refresh waveform

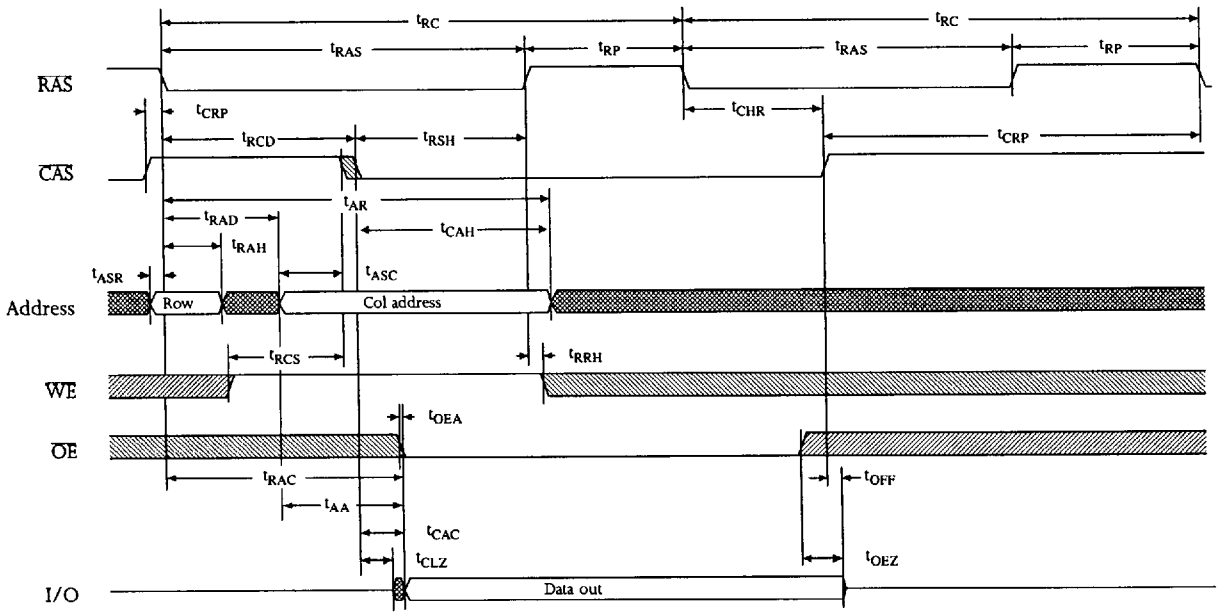
$\overline{WE}$ = $\overline{OE}$ = $V_{IH}$ or $V_{IL}$



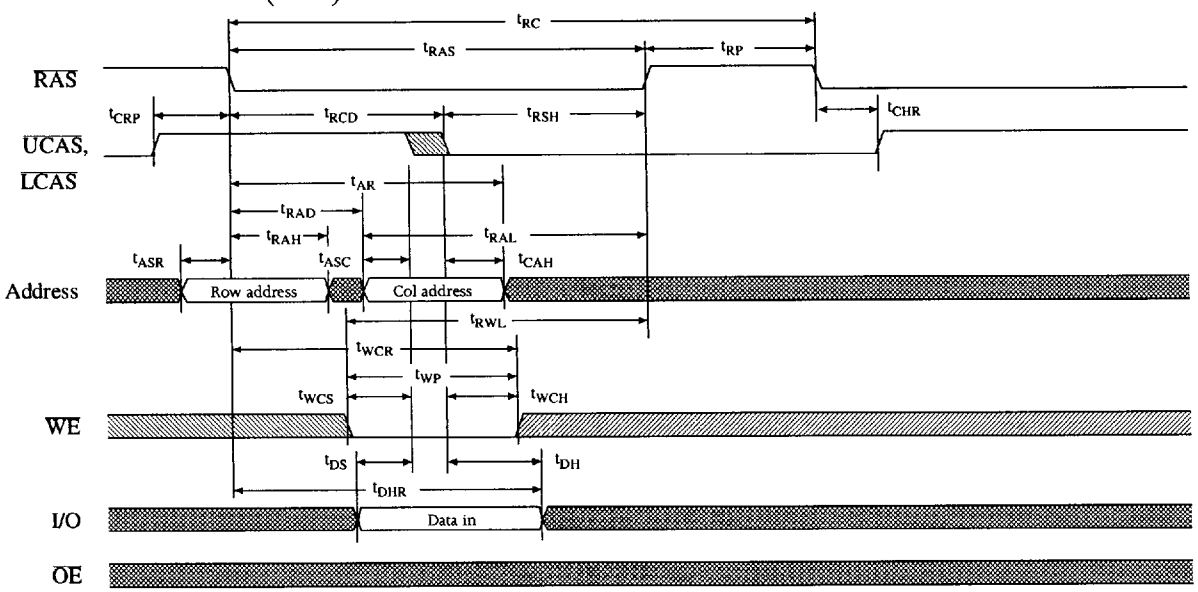
## Hyper page mode byte read-modify-write waveform



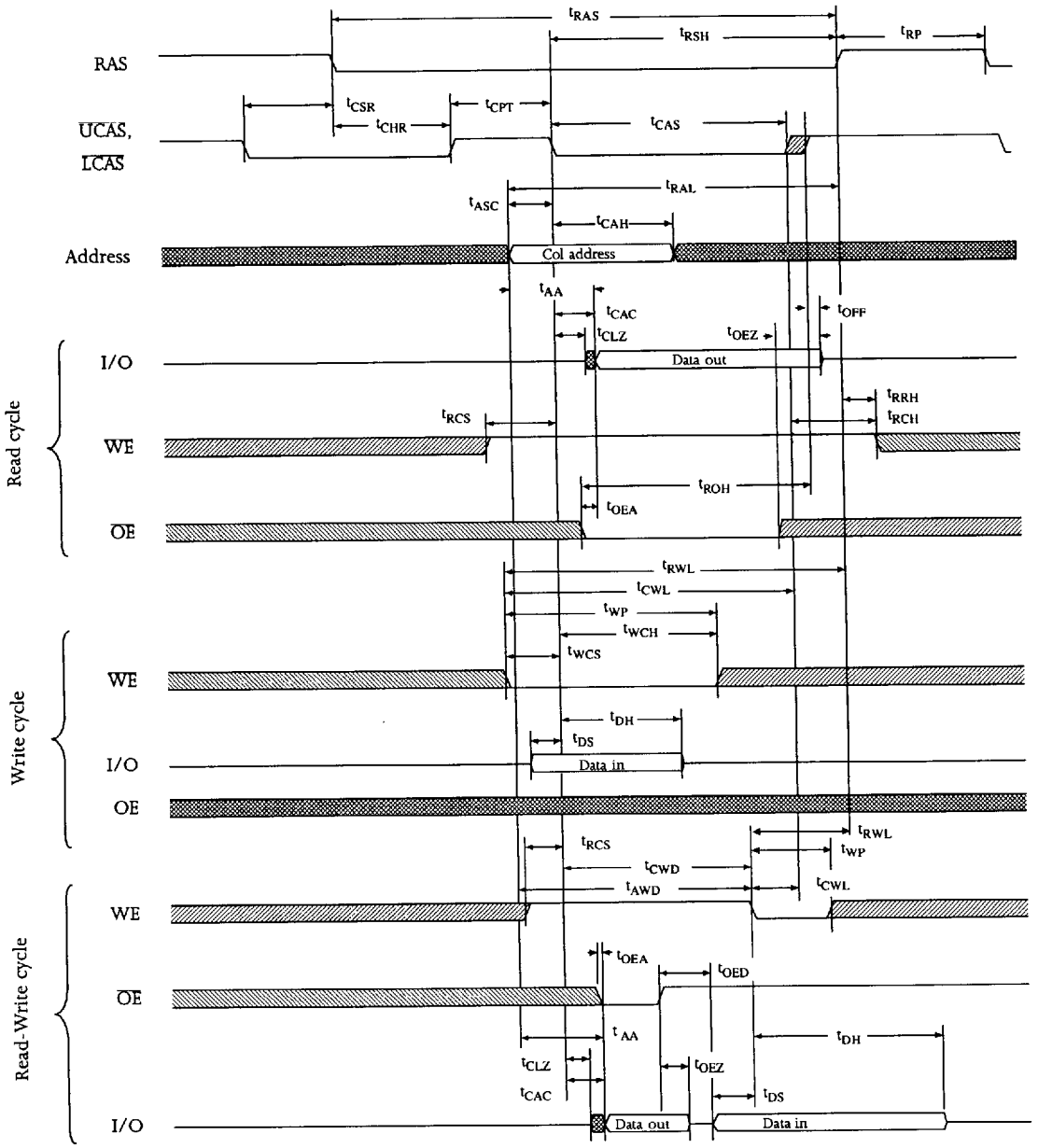
## Hidden refresh waveform (read)




## Hidden refresh waveform (write)



## $\overline{CAS}$ before $\overline{RAS}$ refresh counter test waveform



## Capacitance [15]

$f$ = 1 MHz, $T_a$ = Room temperature

| Parameter | Symbol | Signals | Test conditions | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN1}$ | A0 to A8 | $V_{in}$ = 0V | 5 | p |
| | $C_{IN2}$ | $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$ | $V_{in}$ = 0V | 7 | p |
| I/O capacitance | $C_{I/O}$ | I/O0 to I/O15 | $V_{in}$ = $V_{out}$ = 0V | 7 | pF |

## AS4C256K16E0 ordering information

| Package \ $\overline{RAS}$ access time | | 45 ns | 50 ns | 60 ns |
|---|---|---|---|---|
| Plastic SOJ, 400 mil, 42-pin | 5V | AS4C256K16E0-45JC | AS4C256K16E0-50JC | AS4C256K16E0-60JC |

## AS4C256K16E0 part numbering system

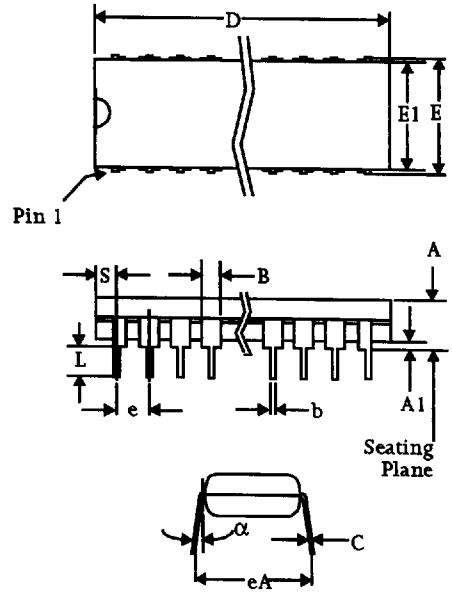
| AS4C | C | 256K16E0 | –XX | X | C |
|---|---|---|---|---|---|
| DRAM prefix | C = 5V CMOS | Device number | $\overline{RAS}$ access time | Package:<br>J = 40-pin SOJ 400 mil | Commercial temperature range, 0°C to 70 °C |

Package diagrams

## Plastic dual in-line package (PDIP)

| | 20-pin 300 mil | | 28-pin 300 mil | | 32-pin 300 mil | | 32-pin 400 mil | |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max |
| A | - | 0.175 | - | 0.175 | - | 0.180 | - | 0.200 |
| A1 | 0.010 | - | 0.010 | - | 0.015 | - | 0.015 | - |
| B | 0.046 | 0.054 | 0.058 | 0.064 | 0.045 | 0.055 | 0.045 | 0.065 |
| b | 0.018 | 0.024 | 0.016 | 0.022 | 0.015 | 0.021 | 0.014 | 0.022 |
| C | 0.008 | 0.014 | 0.008 | 0.014 | 0.008 | 0.012 | 0.009 | 0.015 |
| D | - | 0.980 | - | 1.400 | - | 1.571 | - | 1.620 |
| E | 0.290 | 0.310 | 0.295 | 0.320 | 0.300 | 0.325 | 0.390 | 0.425 |
| E1 | 0.263 | 0.293 | 0.278 | 0.298 | 0.280 | 0.295 | 0.340 | 0.390 |
| e | 0.100 BSC | | 0.100 BSC | | 0.100 BSC | | 0.100 BSC | |
| eA | 0.310 | 0.350 | 0.330 | 0.370 | 0.330 | 0.370 | 0.430 | 0.470 |
| L | 0.110 | 0.130 | 0.120 | 0.140 | 0.110 | 0.142 | 0.118 | 0.162 |
| α | 0° | 15° | 0° | 15° | 0° | 15° | 0° | 15° |
| S | - | 0.040 | - | 0.055 | - | 0.043 | - | 0.065 |

Dimensions in inches




## Plastic small outline J-bend (SOJ)

| | 20/26-pin 300 mil | | 28-pin 300 mil | | 32-pin 300 mil | | 28-pin 400 mil | | 32-pin 400 mil | | 36-pin 400 mil | | 40-pin 400 mil | | 42-pin 400 mil | | 44-pin 400 mil | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| A | - | 0.140 | - | 0.140 | - | 0.145 | 0.132 | 0.146 | - | 0.145 | - | - | - | 0.145 | 0.128 | 0.148 | 0.128 | 0.148 |
| A1 | 0.020 | - | 0.025 | - | 0.025 | - | 0.062 | - | 0.025 | - | - | - | 0.025 | - | 0.025 | - | 0.025 | - |
| A2 | 0.095 | 0.105 | 0.095 | 0.105 | 0.086 | 0.105 | 0.105 | 115 | 0.086 | 0.115 | 0.102 NOM | | 0.086 | 0.115 | 1.105 | 1.115 | 1.105 | 1.115 |
| B | 0.025 | 0.032 | 0.028 TYP | | 0.026 | 0.032 | 0.024 | 0.032 | 0.026 | 0.032 | - | 0.032 | 0.026 | 0.032 | 0.026 | 0.032 | 0.026 | 0.032 |
| b | 0.016 | 0.022 | 0.018 TYP | | 0.014 | 0.020 | 0.013 | 0.021 | 0.015 | 0.020 | 0.013 | 0.021 | 0.015 | 0.022 | 0.015 | 0.020 | 0.015 | 0.020 |
| c | 0.008 | 0.014 | 0.010 TYP | | 0.006 | 0.013 | 0.005 | 0.012 | 0.007 | 0.013 | - | - | 0.007 | 0.014 | 0.007 | 0.013 | 0.007 | 0.013 |
| D | - | 0.686 | - | 0.730 | 0.820 | 0.830 | 0.720 | 0.729 | 0.820 | 0.830 | 0.920 | 0.930 | 1.015 | 1.035 | 1.070 | 1.080 | 1.120 | 1.130 |
| E | 0.327 | 0.347 | 0.327 | 0.347 | 0.330 | 0.340 | 0.430 | 0.440 | 0.435 | 0.445 | 0.350 | 0.390 | 0.435 | 0.445 | 0.370 NOM | | 0.370 NOM | |
| E1 | 0.295 | 0.305 | 0.295 | 0.305 | 0.292 | 0.305 | 0.395 | 0.405 | 0.395 | 0.405 | 0.400 NOM | | 0.395 | 0.405 | 0.395 | 0.405 | 0.395 | 0.405 |
| E2 | 0.245 | 0.285 | 0.245 | 0.285 | 0.250 | 0.275 | 0.354 | 0.378 | 0.360 | 0.380 | 0.435 | 0.445 | 0.348 | 0.390 | 0.435 | 0.445 | 0.435 | 0.445 |
| e | 0.050 BSC | | 0.050 BSC | | 0.050 BSC | | 0.050 BSC | | 0.050 BSC | | 0.045 | 0.055 | 0.050 BSC | | 0.050 NOM | | 0.050 NOM | |

Dimensions in inches