AU9360
USB Multiple Slots
Flash Memory Card Reader
Controller TRM

Revision 1.2

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1.0 Introduction

1.1 Description

The AU9360 is a single chip USB flash memory reader controller which supports not only the widely used flash memory cards, such as Compact Flash (CF) card, Micro Drive (MD), SmartMedia Card (SMC), XD Picture Card, Memory Stick (MS), Memory Stick Duo, Memory Stick PRO, Secure Digital (SD) and Multimedia Card (MMC), but also supports NAND type flash as a USB flash disk. It can be used as removable storage disks in enormous data exchange applications between PC and PC or PC and various consumer electronic appliances.

The AU9360 reads digital data saved on memory card while users manipulating electronic devices such as digital cameras, MP3 players, PDAs and mobile phones… etc. By the AU9360, users can transfer information such as data, graphics, texts or digital images from one electronic device to another quickly and easily. With AU9360, users' knowledge will be further enhanced by the Plug-and-Play nature built into latest operation systems such as Windows 2000/XP and Mac OS X.

By integrating of various analog components, the AU9360 is the most powerful and most effective solution for various flash memory reader.

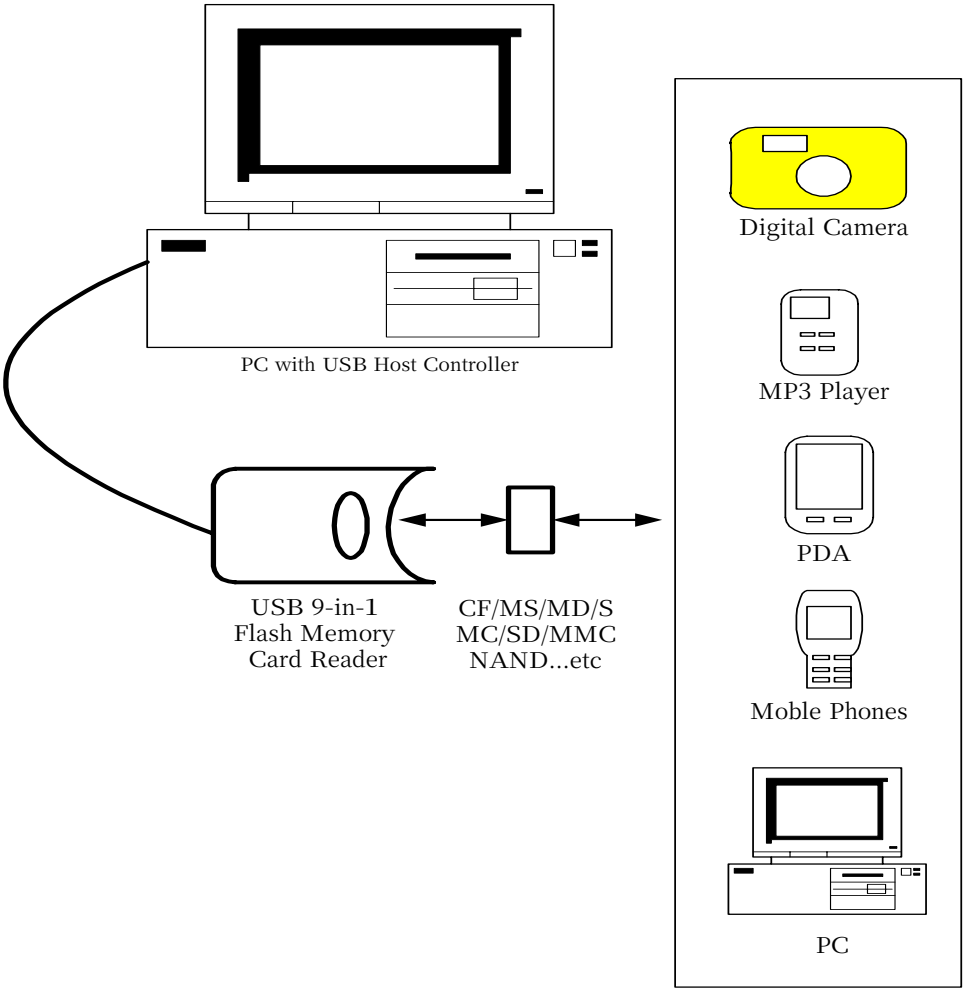
1.2 Features

- Fully compliant with USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Fully compliant with Compact Flash (CF) v1.4 Specification
- Fully compliant with Secure Digital (SD) v1.0 Specification.
- Fully compliant with Memory Stick (MS) v1.3 Specification.
- Fully compliant with Memory Stick PRO v1.0 Specification.
- Fully compliant with Memory Stick ROM Format v1.0 Specification.
- Fully compliant with Memory Stick Duo Format v1.01 Specification.
- Fully compliant with Smart Media Card (SMC) Standard 2000 Specification.
- Support 1 piece NAND type flash memory up to 2Gbit capacity.
- Support Mask ROM Card capacity from 2MB to 256MB.
- Work with default driver from Windows ME, Windows XP, Mac OS 9, and Mac OS X. Windows 98, Windows 2000 are supported by vendor driver from Alcor.

- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer to 4GB to optimize performance
- Support optional external EEPROM for USB VID, PID and string customization
- Support slot to slot read/write operation.
- Support auto-detecting slot with card inserted on Win 2000 without driver.
- Capable of handling 8 sets of built-in PID, VID and strings to minimize inventory control and improve lead production lead time
- Support 5 different LEDs for bus activity indication of 5 separated slots.
- Each slot can be enables/disabled by 5 independent pins to fit all the different card readers' combinations requirement.
- Integrated 4 power switches and power management circuit for each slot to meet USB 500uA power consumption during suspend with card in the slot.
- Runs at 12MHz, built-in 48 MHz PLL
- Built-in 3.3V regulator
- 100-pin LQFP package

2.0 Application Block Diagram

Following is the application diagram of a typical flash memory card reader using AU9360. By connecting the reader to a PC through USB bus, the AU9360 is acting as a bridge between the flash memory card from digital camera, MP3 player, PDA or mobile phone and PC.



3.0Pin Assignment

The AU9360 is packed in 100-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

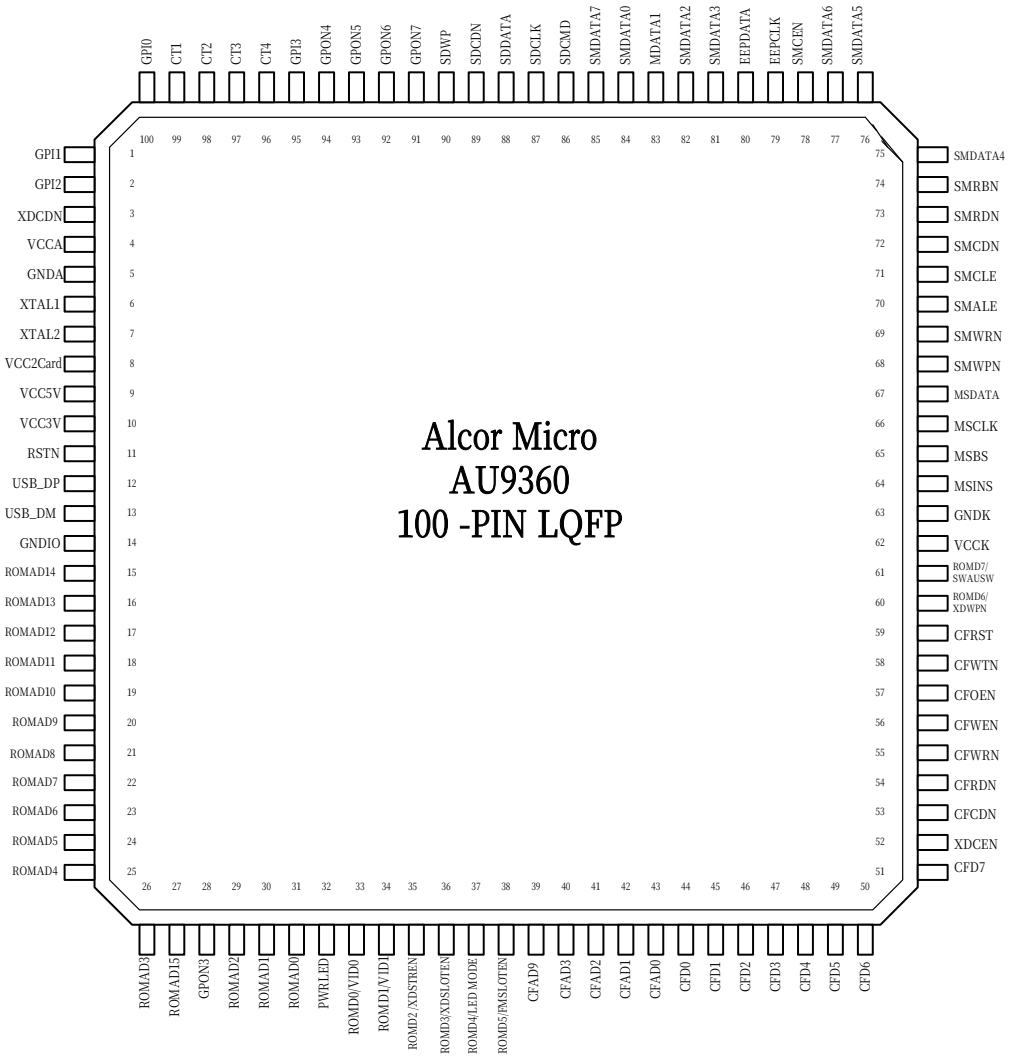


Table 3-1. Pin Descriptions

Pin	Pin Name	I/O Type	Description
1	GPI1	I	CF card slot enable
2	GPI2	I	SM card slot enable
3	XDCDN	I	Connect to XD Card Detect
4	VCCA	PWR	Analog 3.3V input
5	GNDA	PWR	Ground
6	XTAL1	I	Crystal Oscillator Input (12MHz)
7	XTAL2	O	Crystal Oscillator Output (12MHz)
8	VCC2Card	O	Connect to Card Power
9	VCC5V	PWR	5V power supply
10	VCC3V	PWR	Regular 3.3V output/ IO 3.3V input
11	RSTN	Input	Hardware reset (Active Low)
12	USB_DP	I/O	USB D+
13	USB_DM	I/O	USB D-
14	GNDIO	PWR	Ground
15	ROMAD14	O	Connect to External ROM Addr14
16	ROMAD13	O	Connect to External ROM Addr13
17	ROMAD12	O	Connect to External ROM Addr12
18	ROMAD11	O	Connect to External ROM Addr11
19	ROMAD10	O	Connect to External ROM Addr10
20	ROMAD9	O	Connect to External ROM Addr9
21	ROMAD8	O	Connect to External ROM Addr8
22	ROMAD7	O	Connect to External ROM Addr7
23	ROMAD6	O	Connect to External ROM Addr6
24	ROMAD5	O	Connect to External ROM Addr5
25	ROMAD4	O	Connect to External ROM Addr4
26	ROMAD3	O	Connect to External ROM Addr3
27	ROMAD15	O	Connect to External ROM Addr15
28	GPON3	O	General Purpose Output pin, used as activity LED / XD card Access LED blink
29	ROMAD2	O	Connect to External ROM Addr2
30	ROMAD1	O	Connect to External ROM Addr1
31	ROMAD0	O	Connect to External ROM Addr0
32	PWRLED	O	General Purpose Output pin, used as activity LED / Power LED
33	ROMD0 / VID0	I/O	Connect to External ROM D0 / Selection VID/PID
34	ROMD1 / VID1	I/O	Connect to External ROM D1 / Selection VID/PID
35	ROMD2 / XDSTREN	I/O	Connect to External ROM D2 / XD String Enable
36	ROMD3/ XDSLOTEN	I/O	Connect to External ROM D3 / XD card slot enable

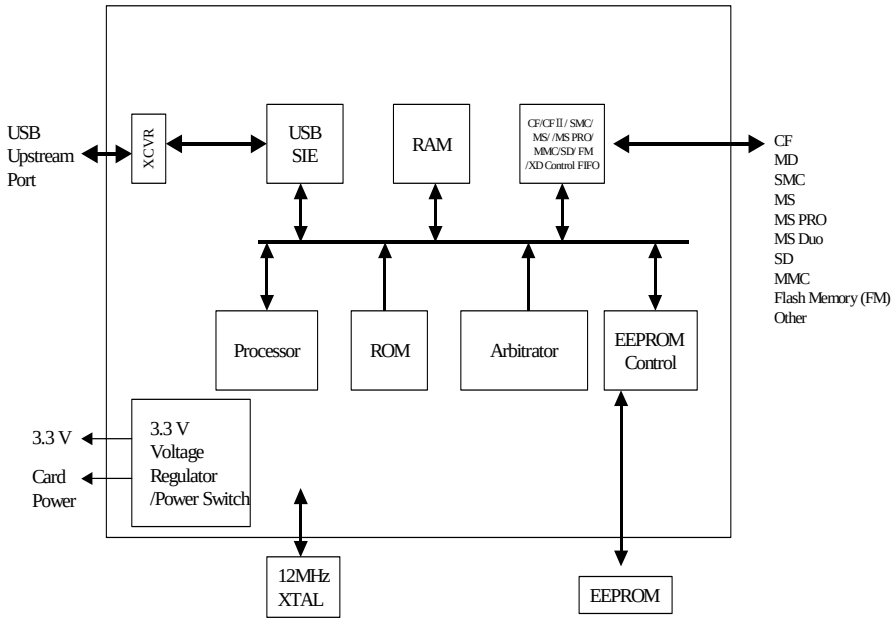
37	ROMD4/ LED MODE	I/O	Connect to External ROM D4/ LED Mode Selection
38	ROMD5/ FMSLOTEN	I/O	Connect to External ROM D5/ Flash Slot Enable
39	CFAD9	O	Connect to CF Card Addr9
40	CFAD3	O	Connect to CF Card Addr3
41	CFAD2	O	Connect to CF Card Addr2
42	CFAD1	O	Connect to CF Card Addr1
43	CFAD0	O	Connect to CF Card Addr0
44	CFD0	I/O	Connect to CF Card Data0
45	CFD1	I/O	Connect to CF Card Data1
46	CFD2	I/O	Connect to CF Card Data2
47	CFD3	I/O	Connect to CF Card Data3
48	CFD4	I/O	Connect to CF Card Data4
49	CFD5	I/O	Connect to CF Card Data5
50	CFD6	I/O	Connect to CF Card Data6
51	CFD7	I/O	Connect to CF Card Data7
52	XDCEN	O	Connect to XD Card Enable
53	CFCDN	I	Connect to CF Card Card Detect
54	CFRDN	O	Connect to CF Card IORD
55	CFWRN	O	Connect to CF Card IOWR
56	CFWEN	O	Connect to CF Card WE
57	CFOEN	O	Connect to CF Card OE
58	CFWTN	I	Connect to CF Card WAIT
59	CFRST	O	Connect to CF Card Reset
60	ROMD6/ XDWPN	I/O	Connect to External ROM D6 / XD Write protection (protect=0, not protect=1)
61	ROMD7/ SWAUSW	I/O	Connect to External ROM D7/ Software auto switch disk for win 2000 (Enable=0, Disable=1).
62	VCCK	PWR	Core 3.3V Input
63	GNDK	PWR	Ground
64	MSINS	I	Connect to MemoryStick Card INS
65	MSBS	O	Connect to MemoryStick Card BS
66	MSCLK	O	Connect to MemoryStick Card SCLK
67	MSDATA	I/O	Connect to MemoryStick Card DATA
68	SMWPN	I	Connect to SmartMedia Card Write Protect
69	SMWRN	O	Connect to SmartMedia Card Write Enable
70	SMALE	O	Connect to SmartMedia Card Address Latch Enable
71	SMCLE	O	Connect to SmartMedia Card Command Latch Enable
72	SMCDN	I	Connect to SmartMedia Card Card Detect
73	SMRDN	O	Connect to SmartMedia Card Read Enable
74	SMRBN	I	Connect to SmartMedia Card Ready/Busy Output
75	SMDATA4	I/O	Connect to SmartMedia Card Data 4

76	SMDATA5	I/O	Connect to SmartMedia Card Data5
77	SMDATA6	I/O	Connect to SmartMedia Card Data 6
78	SMCEN	O	Connect to SM Card Enable
79	EEPCLK	O	Connect to EEPROM Serial Clock
80	EEPDATA	I/O	Connect to EEPROM Serial Data
81	SMDATA3	I/O	Connect to SmartMedia Card Data 3
82	SMDATA2	I/O	Connect to SmartMedia Card Data 2
83	SMDATA1	I/O	Connect to SmartMedia Card Data 1
84	SMDATA0	I/O	Connect to SmartMedia Card Data 0
85	SMDATA7	I/O	Connect to SmartMedia Card Data 7
86	SDCMD	I/O	Connect to SD CMD
87	SDCLK	O	Connect to SD CLK
88	SDDATA	I/O	Connect to SD Data
89	SDCDN	I	Connect to SD Card Detect
90	SDWP	I	Connect to SD Write Protect
91	GPON7	O	General Purpose Output pin, used as activity LED / MS card Access
92	GPON6	O	General Purpose Output pin, used as activity LED / SM card Access
93	GPON5	O	General Purpose Output pin, used as activity LED / CF card Access
94	GPON4	O	General Purpose Output pin, used as activity LED / SD card Access
95	GPI3	I	MS card slot enable
96	CT4	I	ECC Selection ('0'=Disable, '1'=Enable)
97	CT3	I	Connect to ground
98	CT2	I	ROM Selection ('0' = Internal ROM, '1'=External ROM)
99	CT1	I	Connect to ground
100	GPI0	I	SD card slot enable

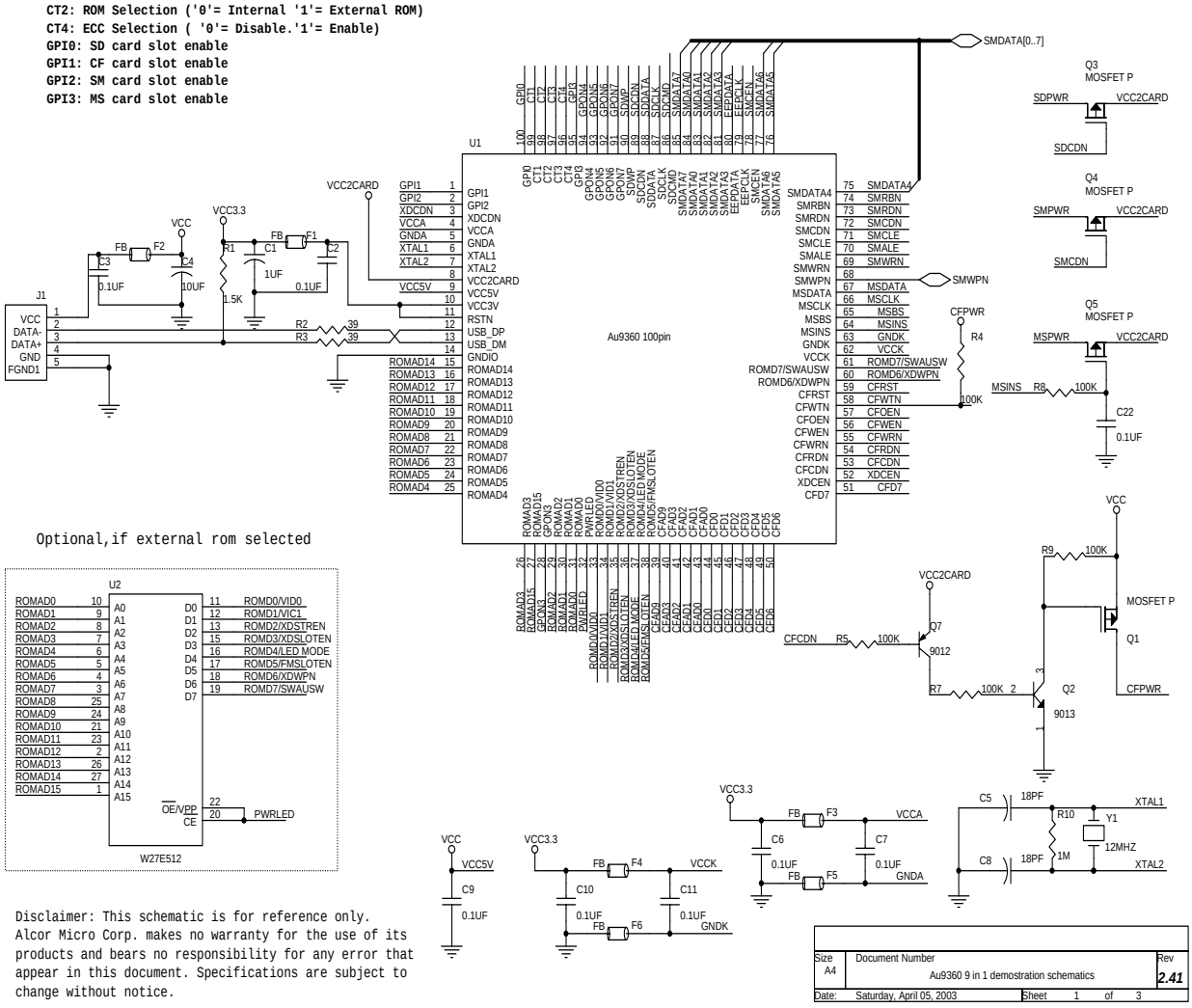
4.0 System Architecture and Reference Design

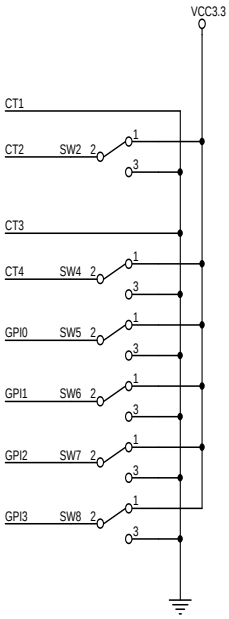
4.1 AU9360 Block Diagram

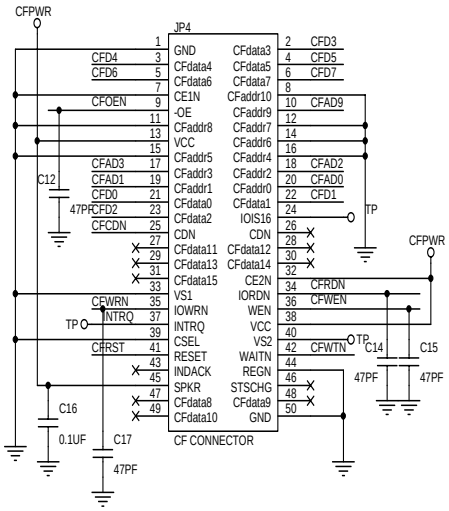
Alcor Micro – AU9360
Flash Memory Card Reader Controller Chip Block Diagram

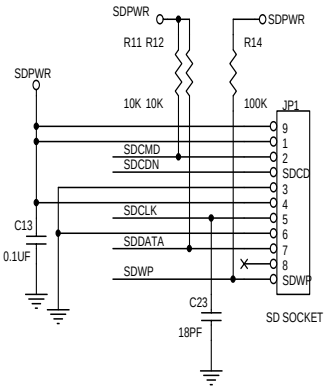


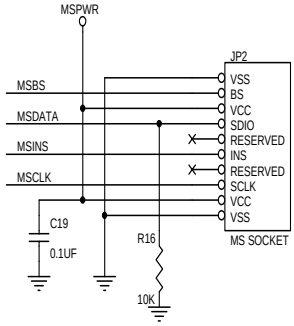
4.2 Sample Schematics











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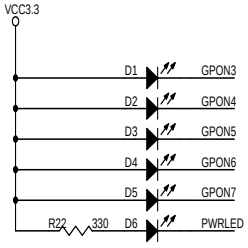

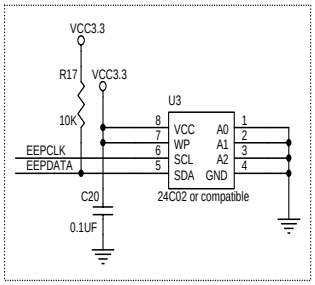

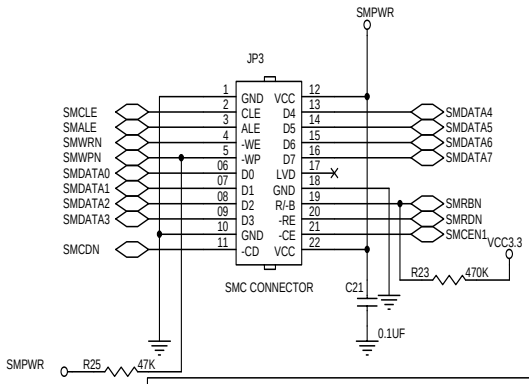

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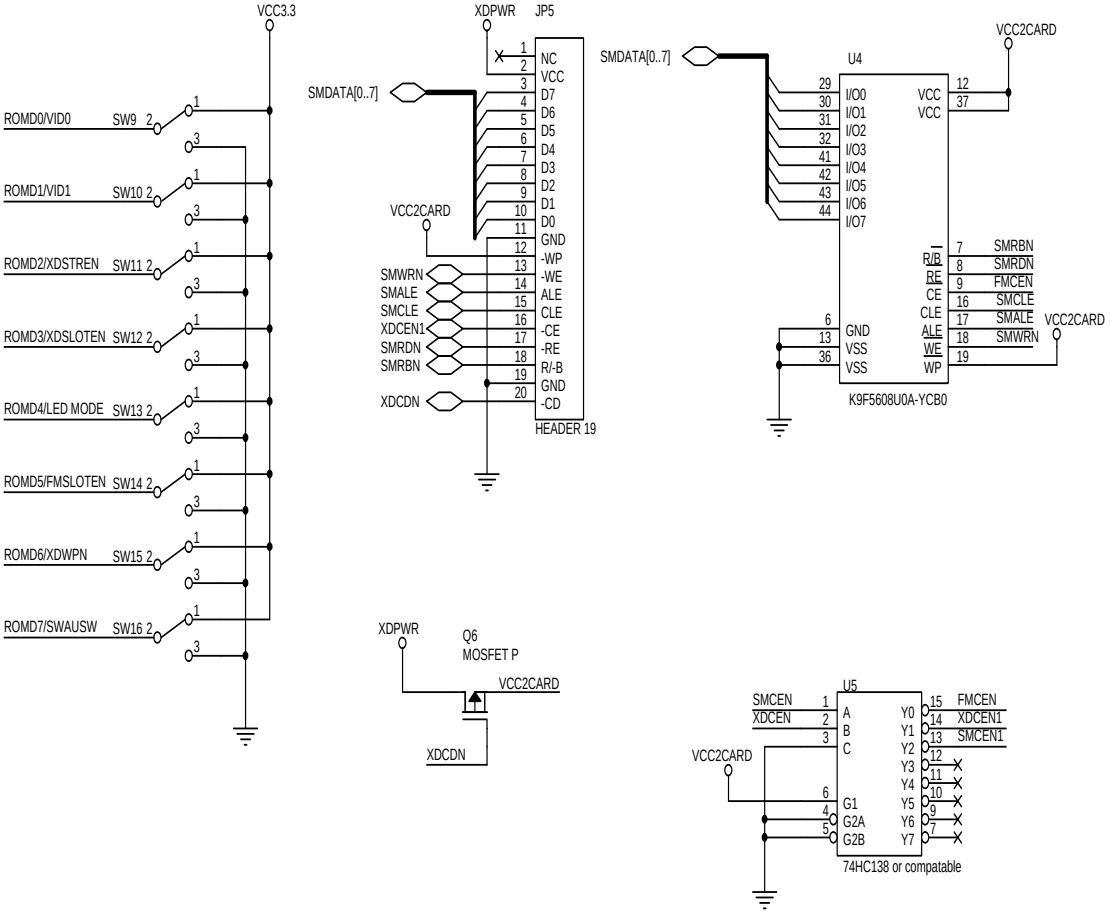
Size	Document Number	Rev
A4	Au9360 9 in 1 demostration schematics	2.41
Date: Saturday, April 05, 2003	Sheet 2 of 3	



Internal ROM only

VID0: Selection VID/PID
VID1: Selection VID/PID
XDSTREN: XD slot string enable (disable=0, enable=1)
XDSLOTEN: XD card slot enable
LED MODE: LED Mode Enable(Single LED=1, 5 LED=0)
FMSLOTEN: Flash slot enable (disable=0, enable=1)
XDWPN: XD Write protect (proect=0, not protect=1)
SWAUSW: Software auto switch disk for win 2000 (Enable=0, Disable=1)

Pin 16 connect to vcc2card
Pin 8 connect to GND

Size	Document Number	Rev
A	Au9360 9 in 1 demostration schematics	2.41
Date: Friday, April 11, 2003	Sheet 3 of 3	

5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply	-0.3 to 6.0	V
V_{IN}	Input Voltage	-0.3 to VCC+0.3	V
V_{OUT}	Output Voltage	-0.3 to VCC+0.3	V
T_{STG}	Storage Temperature	-40 to 125	°C

5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.5	5.0	5.5	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	-5		85	°C

5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	µA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	µA
I_{OZ}	Tri-state leakage current		-10		10	µA
C_{IN}	Input capacitance			4		ρF
C_{OUT}	Output capacitance			4		ρF
C_{BID}	Bi-directional buffer capacitance			4		ρF

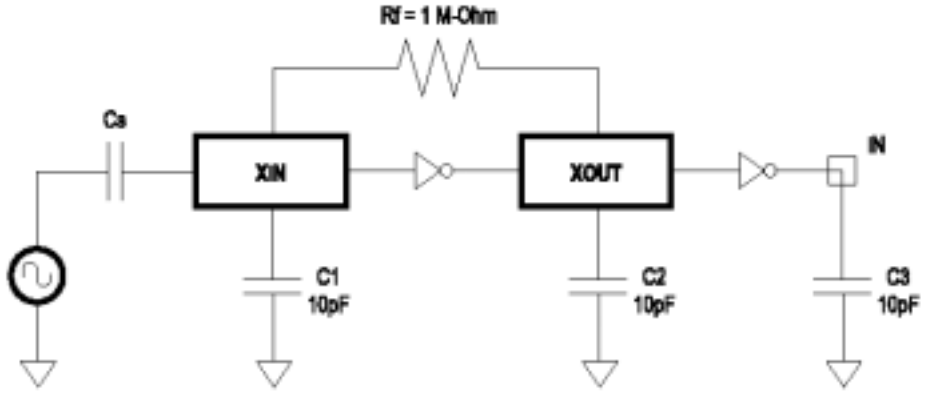
5.4 DC Electrical Characteristics for 5 volts operation

(Under Recommended Operating Conditions and V_{CC}=4.5v ~ 5.5v , Tj= -40°C to + 85°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	TTL			0.8	V
V_{IL}	Input Low Voltage	CMOS			0.3*V_{CC}	V
V_{IL}	Schmitt input Low Voltage	TTL		1.10		V
V_{IL}	Schmitt input Low Voltage	CMOS		1.84		V
V_{IH}	Input High Voltage	TTL	2.2			V
V_{IH}	Input Hight Voltage	CMOS	0.7*V_{CC}			V
V_{IH}	Schmitt input High Voltage	TTL		1.87		V
V_{IH}	Schmitt input High Voltage	CMOS		3.22		V
V_{OL}	Output low voltage	I_{OL}=2, 4, 8, 12, 16, 24 mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=2, 4, 8, 12, 16, 24 mA	3.5			V
R_I	Input Pull-up/down Resistance	Vil=0_V or Vih=V_{CC}		50		KΩ

5.5 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.



5.6 USB Transceiver Characteristics

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		3.0	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{AMB}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	0	70	°C

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

In accordance with the Absolute Maximum Rating System, Voltages are referenced to GND (Ground=0v)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		-0.5	+6.5	V
I_{IK}	DC input diode current	Vi<0		-50	mA
V_I	DC input voltage	Note 3	-0.5	+5.5	V
$V_{I/O}$	DC input voltage range for I/Os		-0.5	Vcc +0.5	V
I_{OK}	DC output diode current	Vo> Vcc or Vo<0		+/-50	mA
V_O	DC output voltage	Note 3	-0.5	Vcc +0.5	V
I_O	DC output source sink current for VP/VM and RCV pins	Vo=0 to Vcc		+/-15	mA
I_O	DC output source or sink current for D+/D- pins	Vo= 0 to Vcc		+/-50	mA
I_{CC}, I_{GND}	DC Vcc or GND current			+/-100	mA
T_{STO}	Storage temperature range		-60	+150	°C
P_{TOT}	Power dissipation per package				mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The performance capability of a high performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (Ground=0V).

SYMBOL	PARAMETER	TEST CONDI 'IONS	L] MITS -40°C to +85°C			UNIT
			MIN	TYP	MAX	
VHYS	Hysteresis on inputs	Vcc=3.0V to 3.(V (Note 3)	0.3	0.4	0.5	V
VIH	HIGH level input	Vcc=3.0V to 3.(V (Note 3)		1.5	2.0	V
VIL	LOW level input	Vcc=3.0V to 3.(V (Note 3)	0.8	1.1		V
RoH	Output impedance (IIGH state)	Note 2	28	34	43	ohm
RoL	Output impedance (.OW state)	Note 2	28	35	43	ohm
VOH	HIGH level output (Note 3)	Vcc=3.0V Io=6 nA Vcc=3.0V Io=4 nA Vcc=3.0V Io=1 0µA	2.2 2.4 2.8	2.7		V
VOL	LOW level output (Note 3)	Vcc=3.0V Io=6 nA Vcc=3.0V Io=4 nA Vcc=3.0V Io=1 0µA		0.3	0.7 0.4 0.2	V
IQ	Quiescent supply cu rent	Vcc=3.6V VI=' cc or GND Io=0		330	600	µA
Isup	Supply current in su pend	Vcc=3.6V VI=' cc or GND Io=0			70	µA
IFS	Active supply curre t (Full Speed)	Vcc=3.3V		9	14	mA
ILS	Active supply curre t (Low Speed)	Vcc=3.3V		2		mA
ILeak	Input leakage curre :	Vcc=3.6V VI=5 5V or GND, not for I/O Pins		+/- 0.1	+/-0.5	µA
IOFF	3-state output OFF- tate current	Vi=Vih or ViL; 7o=Vcc or GND			+/-10	µA

NOTES:

1. All typical values are at Vcc=3.3V and Tamb=25°C.
2. This value includes an external resistor of 24 ohm +/-1%. See "Load D+ and D-" diagram for testing details.
3. All signals except D+ and D-.

AC ELECTRICAL CHARACTERISTICS

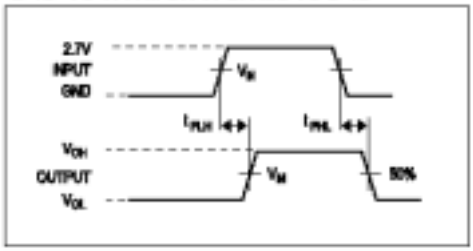
GND=0V, $t_R = t_F$ =3.0 ns; C_L =50 pF; RL=500 Ohms

SYMBOL	PARAM ETER	V AVEFORM	LIMITS (T_{AMB})					UNIT
			0°C ɔ +25°C			0°C ɔo +70°C		
			MIN	TYP	MAX	MIN	MAX	
tpLH tpHL	VMO/VI O to D+/D- Full Spe d	1	0 0		12 12	0 0	14 14	ns
trise tfall	Rise and Fall Times Full Spe d	2	4 4	9 9	20 20	4 4	20 20	ns
tRFM	Rise and Fall Time Matchin Full Spe d		90		110	90	110	%
tpLH tpHL	VMO/VI O to D+/D- Low Spe d	1		120 120	300 300		300 300	ns
trise tfall	Rise and Fall Times Low Spe d	2	75 75		300 200	75 75	300 200	ns
tRFM	Rise and Fall Time Matchin Low Spe d		70		130	70	130	%
tpLH tpHL	D+/D- tc RCV	3		9 9	16 16		16 16	ns
tpLH tpHL	D+/D- tc VP/VM	1		4 4	8 8		8 8	ns
tpHZ tpZH tpLZ tpZL	OE# to I +/D- RL = 500ohm	4			12 12 10 10		12 12 10 10	ns
tsu	Setup fo SPEED	5	0					ns
Vcr	Crossov point[1]	3	1.3		2.0	1.3	2.0	V

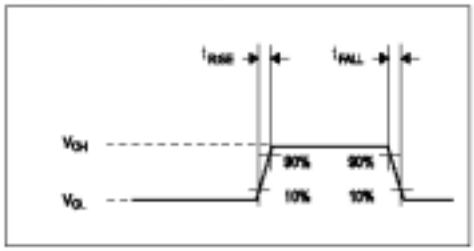
NOTES:

1. The crossover point is in the range of 1.3V to 2.5V for the low speed mode with a 50 pF capacitance.

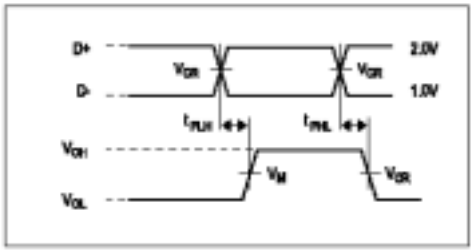
AC WAVEFORM 1.
D+/D- TO VP/VM OR VPO/VMO TO D+/D-



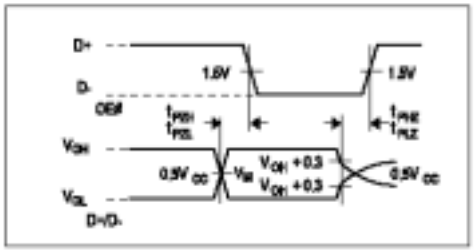
AC WAVEFORM 2.
RISE AND FALL TIMES



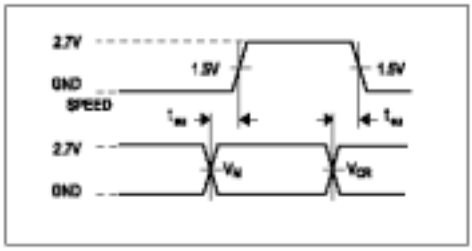
AC WAVEFORM 3.
D+/D- TO RCV



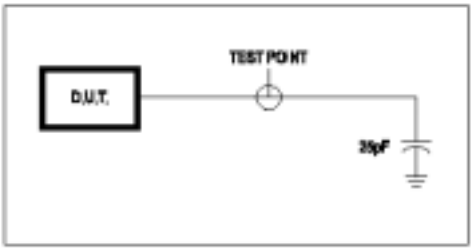
AC WAVEFORM 4.
OE# TO D+/D-



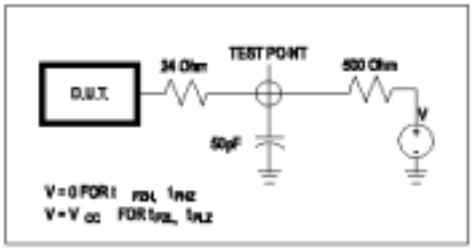
AC WAVEFORM 5.
SETUP FOR SPEED



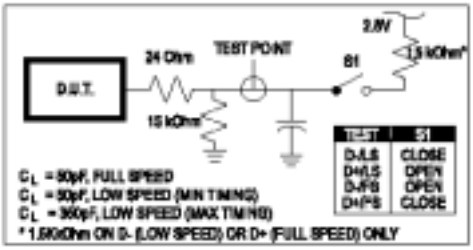
TEST CIRCUIT 1.
LOAD FOR VM/VP AND RCV



TEST CIRCUIT 2.
LOAD FOR ENABLE AND DISABLE TIMES



TEST CIRCUIT 3.
LOAD FOR D+/D-



	S1
D-/LS	CLOSE
D+/LS	OPEN
D-/FS	OPEN
D+/FS	CLOSE

5.7 ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body-Model (HBM) and Machine-Model (MM), according to MIL-STD 883 and EIAJ IC-121 respectively.

- Human-Body-Model stresses devices by sudden application of a high voltage supplied by a 100pF capacitor through 1.5k-ohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200pF capacitor through very low (0 ohm) resistance.

Test Circuit & Condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

ESD Data

Model	Mode	#/S	Target	Results
HBM	Vdd, Vss, I/O	5	6000V	PASS
MM	Vdd, Vss, I/O	5	200V	PASS

5.8 Latch-Up Test Results

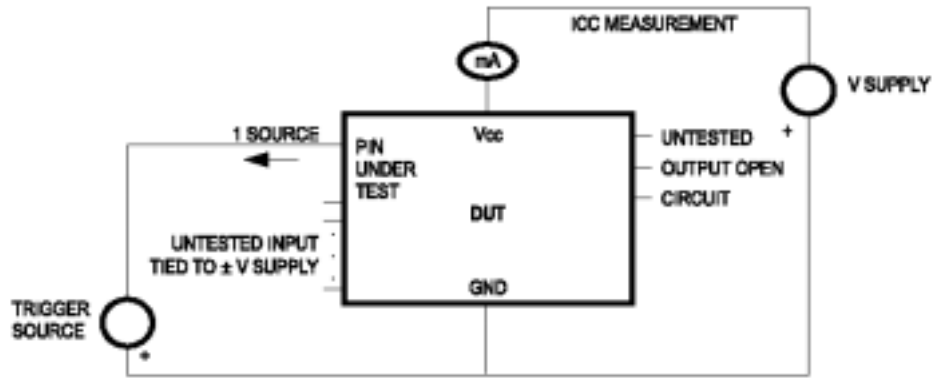
Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5Volts and ground respectively.

Testing was started at 5.0V (Positive) or 0V (Negative), and the DUT was biased for 0.5 seconds.

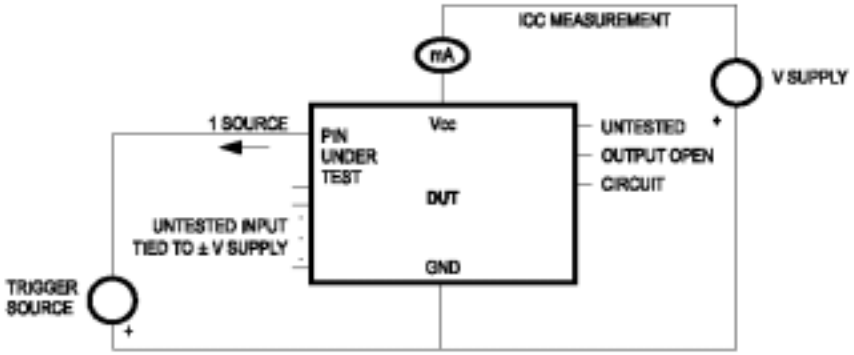
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=00mA, Icc=100mA), then the voltage was increased by 0.1Volts and the pin was tested again.

This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

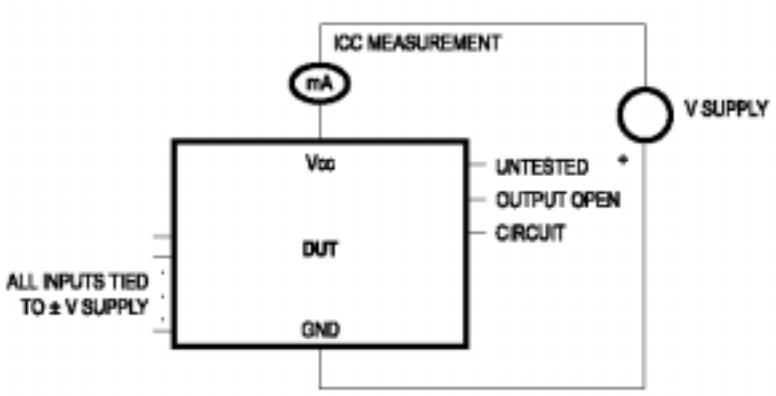
Notes:
1. DUT: The device under test.
2. PUT: The pin under test.



Test Circuit: Positive Input/Output Overvoltage/Overcurrent



Test Circuit: Negative Input/Output Overvoltage/Overcurrent



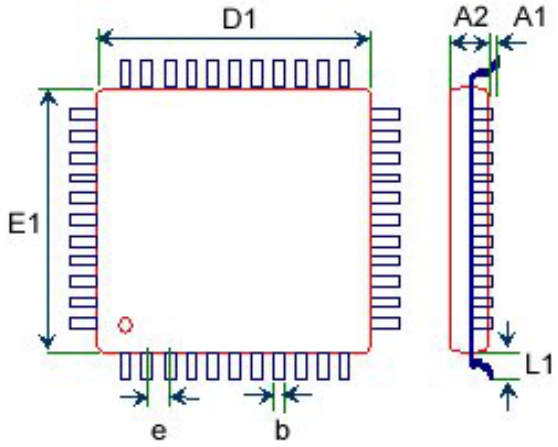
Supply Overvoltage Test

Latch-Up Data

Mo e		Voltage (V)/C rrent (mA)	S/S	Re: ults
Voltage	+	11.0	5	Pa: ;
	-	11.0	5	Pa: ;
Current	+	200	5	Pa: ;
	-	200	5	Pa: ;
Vd - Vxx		9.0	5	Pa: ;

6.0 Mechanical Information

Following table shows the dimensions of the AU9360 100-pin LQFP. Measurements are in inches. The illustration is just an example for LQFP but not for AU9360 real size.



body size		lead	A1	A2	L1	b	c	e
D1	E1	count						
14	14	100	0.1	1.4	1	0.2	0.127	0.5

A1	stand-off
A2	body thickness
L1	lead length
b	lead width
c	lead thickness
e	lead pitch

7.0 Errata

Record History

12/23/2002	CT3 should change connection from high to low. Shuttle 9360 chip using 24 MHz is not working, so we let the CT3 connect to high for using 12 MHz. After firmware changed (code: 911218), 24 MHz is working fine and we used 24MHz to tape out. So the schematic should change to use 24 MHz. Data book updated to version1.1
03/26/2003	AU9360 controller chip improved to support Memory Stick PRO. Data book was then updated the version to 1.2 to add information on Memory Stick PRO. Modified parts are descriptions, features, pin names, diagrams and schematics.