TOSHIBA Insulated Gate Bipolar Transistor Silicon N Channel MOS Type

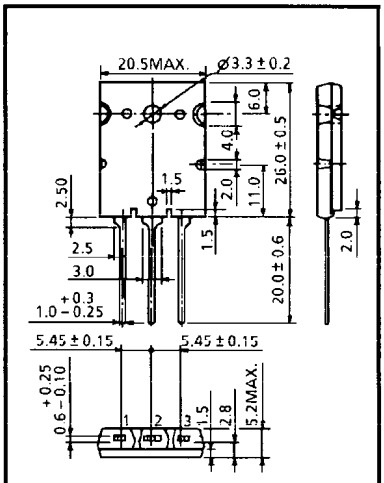
G T 6 0 N 3 2 1

High Power Switching Applications

The 4th Generation

- FRD Included Between Emitter and Gollector
- Enhancement-Mode
- High Speed IGBT : t_f = 0.25 μs (typ.) (@I_C = 60 A)
  FRD : t_{rr} = 0.8 μs (typ.) (@di/dt = –20 A/μs)
- Low Saturation Voltage $V_{CE\ (sat)}$ = 2.3 V (typ.) (I_C = 60 A)

Unit in mm



1. GATE
2. COLLECTOR (HEAT SINK)
3. EMITTER

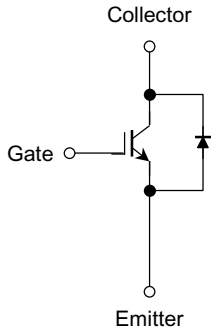
JEDEC	—
EIAJ	—
TOSHIBA	2-21F2C

Weight : 9.75g

Maximum Ratings (Ta = 25°C)

Characteristics		symbol	Rating	Unit
Collector-Emitter Voltage		V_{CES}	1000	V
Gate-Emitter Voltage		V_{GES}	±25	V
Collector Current	DC	I_C	60	A
	1 ms	I_{CP}	120	
Emitter-Collector Forward Current	DC	I_{ECF}	15	A
	1 ms	I_{ECFP}	120	
Collector Power Dissipation (Tc = 25°C)		P_C	170	W
Junction Temperature		T_j	150	°C
Storage Temperature		T_{stg}	–55~150	°C
Screw Torque		—	0.8	N·m

Equivalent Circuit



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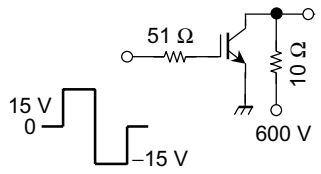
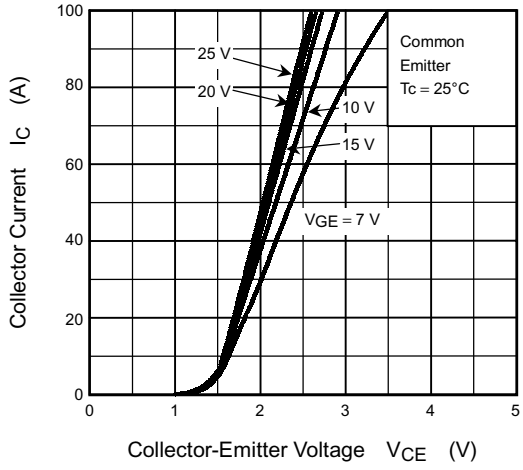
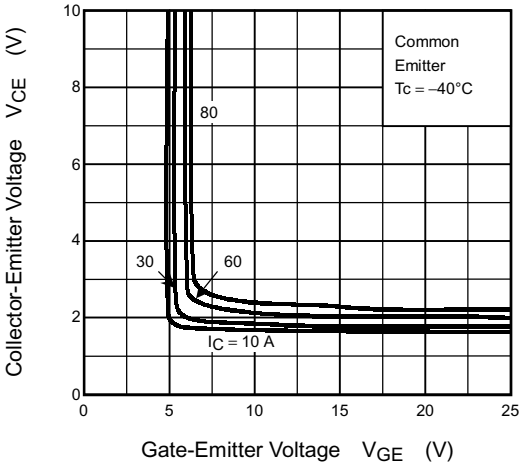
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate Leakage Current		I_{GES}	V_{GE} = ±25 V, V_{CE} = 0	—	—	±500	nA
Collector Cut-off Current		I_{CES}	V_{CE} = 1000 V, V_{GE} = 0	—	—	1.0	mA
Gate-Emitter Cut-off Voltage		$V_{GE\ (OFF)}$	I_C = 60 mA, V_{CE} = 5 V	3.0	—	6.0	V
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$ (1)	I_C = 10 A, V_{GE} = 15 V	—	1.6	2.3	V
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$ (2)	I_C = 60 A, V_{GE} = 15 V	—	2.3	2.8	V
Input Capacitance		C_{ies}	V_{CE} = 10 V, V_{GE} = 0, f = 1 MHz	—	4000	—	pF
Switching Time	Rise Time	t_r		—	0.23	—	µs
	Turn-on Time	t_{on}		—	0.33	—	
	Fall Time	t_f		—	0.25	0.40	
	Turn-off Time	t_{off}		—	0.70	—	
Emitter-Collector Forward Voltage		V_{ECF}	I_{EC} = 15 A, V_{GE} = 0	—	1.5	2.0	V
Reverse Recovery Time		t_{rr}	I_F = 15 A, V_{GE} = 0, di/dt = –20 A/µs	—	0.8	2.5	µs
Thermal Resistance		$R_{th(j-c)}$	—	—	—	0.74	°C/W
Thermal Resistance		$R_{th(j-c)}$	—	—	—	4.0	°C/W

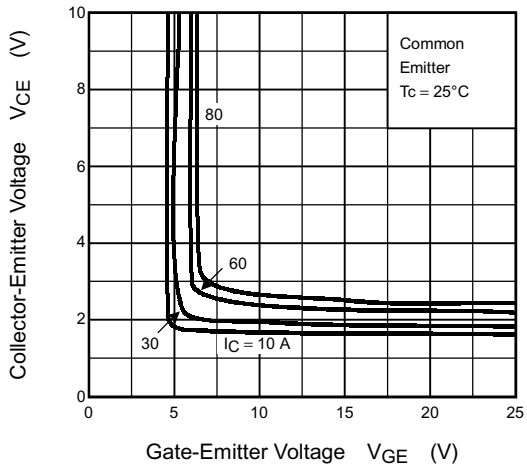
$I_C - V_{CE}$



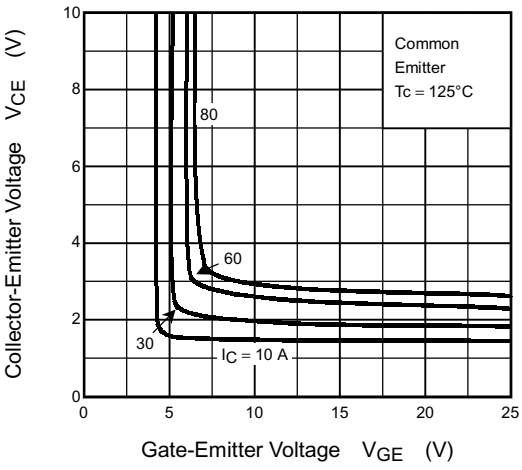
$V_{CE} - V_{GE}$



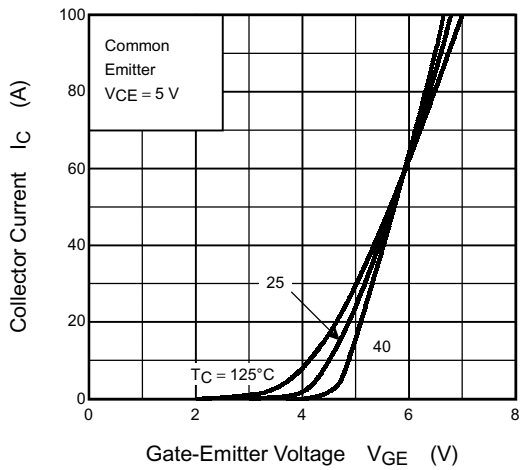
$V_{CE} - V_{GE}$



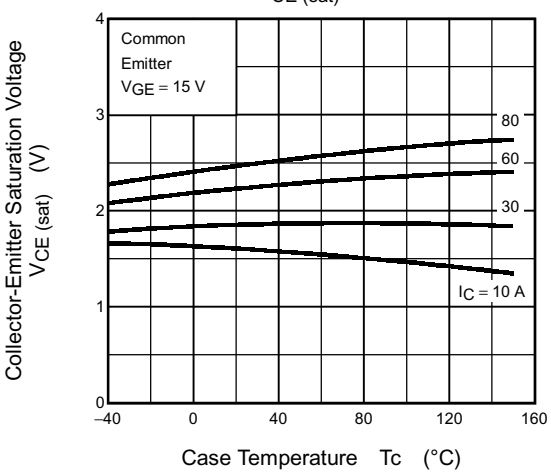
$V_{CE} - V_{GE}$



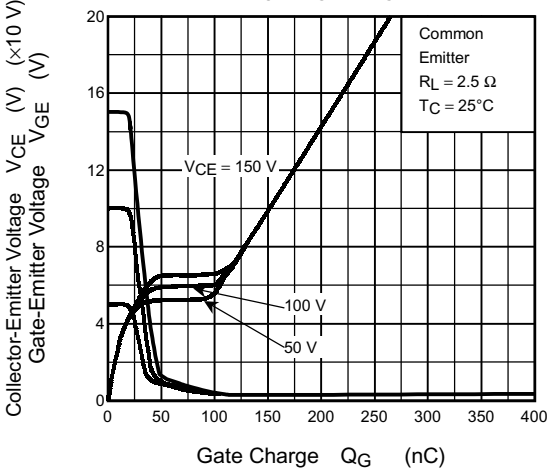
$I_C - V_{GE}$



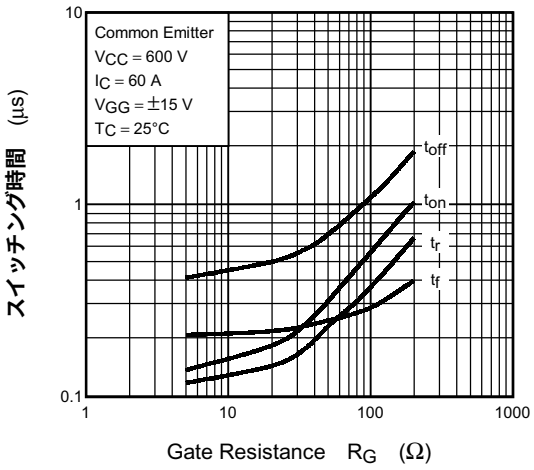
$V_{CE\ (sat)} - Tc$



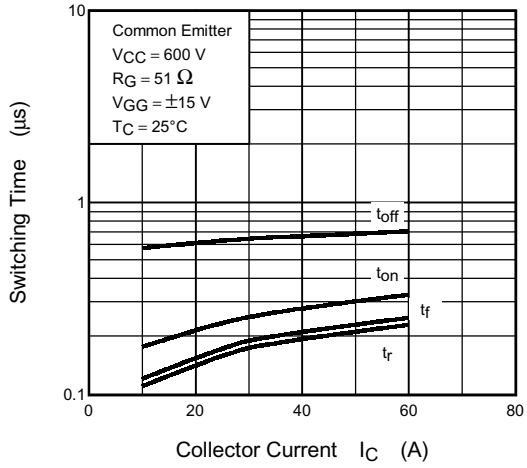
V_{CE}, V_{GE} – Q_G



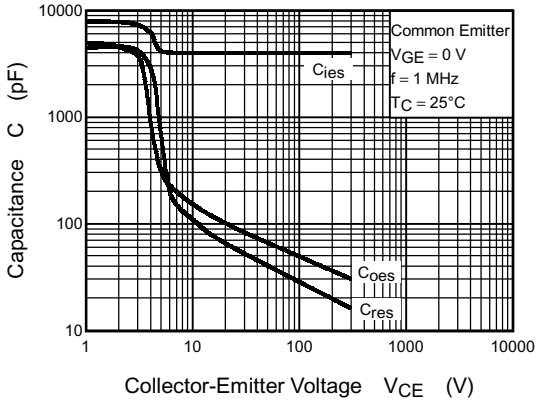
Switching Time – R_G



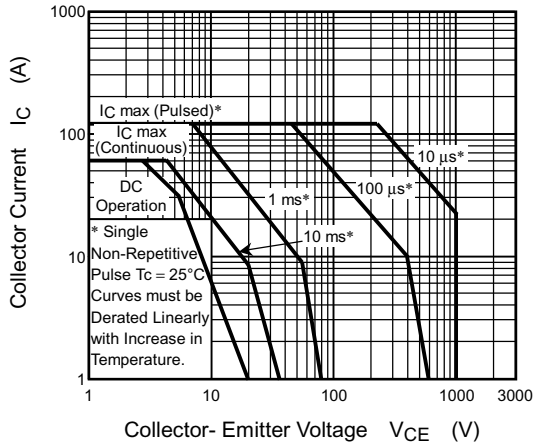
Switching Time – I_C



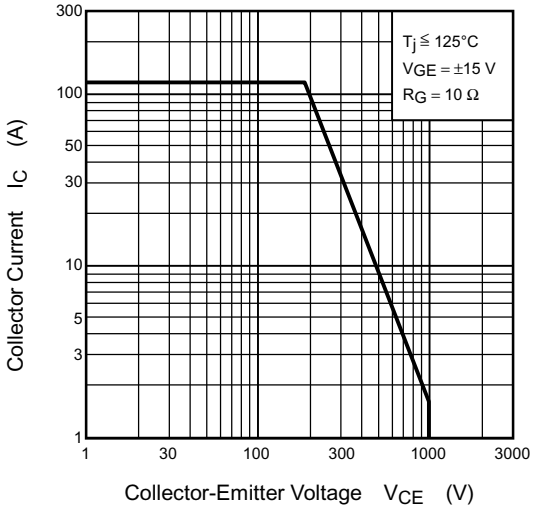
C – V_{CE}



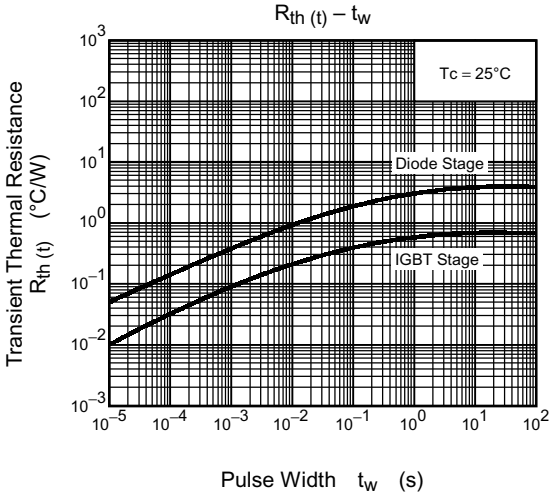
Safe Operating Area



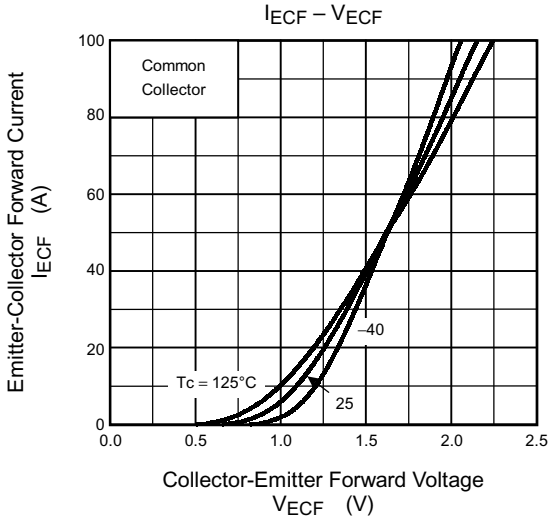
Reverse Bias SOA



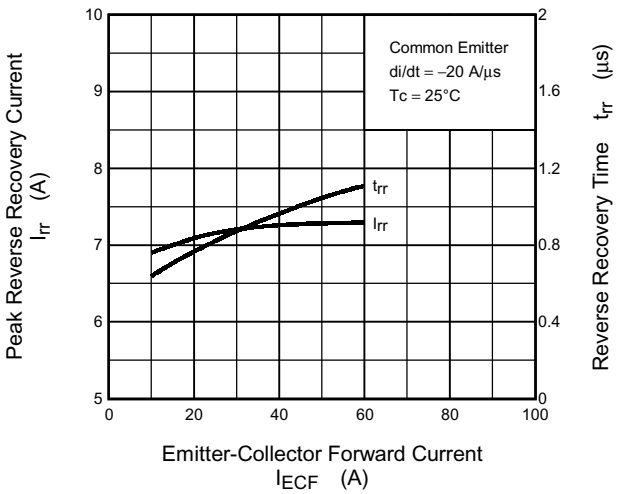
$R_{th\ (t)} - t_w$



$I_{ECF} - V_{ECF}$



$I_{rr}, t_{rr} - I_{ECF}$



$I_{rr}, t_{rr} - di/dt$