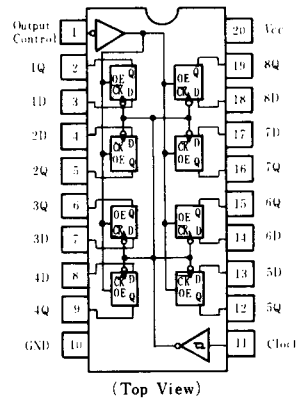


# HD74LS374 ● Octal D-type Edge-triggered Flip-Flops (with three-state outputs)

The HD74LS374, 8-bit registers features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

## ■ PIN ARRANGEMENT

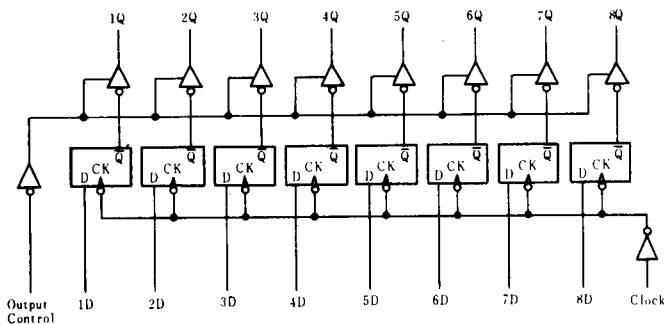


## ■ FUNCTION TABLE

Inputs			Output
Output control	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

Notes: H = high level, L = low level,  
X = irrelevant  
↑ = transition from low to high level  
Q<sub>0</sub> = level of Q before the indicated steady-state input conditions were established  
Z = off (high-impedance) state of a three-state output

## ■ BLOCK DIAGRAM



## ■ RECOMMENDED OPERATING CONDITION

Item	Symbol	min	typ	max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output voltage	V <sub>OH</sub>	—	—	5.5	V
Output current	I <sub>OH</sub>	—	—	-2.6	mA
	I <sub>OL</sub>	—	—	24	mA
Clock pulse width	"H" level	15	—	—	ns
	"L" level	15	—	—	
Data setup time	t <sub>su</sub>	20 ↑	—	—	ns
Data hold time	t <sub>h</sub>	3 ↑	—	—	ns

Note) ↑ : The arrow indicates the rising edge of clock pulse.

## ■ ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	$V_{IH}$		2.0	—	—	V	
	$V_{IL}$		—	—	0.8	V	
Output voltage	$V_{OH}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-2.6\text{mA}$	2.4	—	—	V	
	$V_{OL}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$				V	
Off-state output current	$I_{OZH}$	$V_{CC}=5.25\text{V}, V_{IH}=2\text{V}$	$I_{OL}=12\text{mA}$	—	—	0.4	$\mu\text{A}$
	$I_{OZL}$		$I_{OL}=24\text{mA}$	—	—	0.5	
Input current	$I_{IH}$	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	—	—	20	$\mu\text{A}$	
	$I_{IL}$	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	—	—	-0.4		
	$I_I$	$V_{CC}=5.25\text{V}, V_I=7\text{V}$	—	—	0.1		
Short-circuit output current	$I_{OS}$	$V_{CC}=5.25\text{V}$	-30	—	-130	$\text{mA}$	
Supply current	$I_{CC}$	$V_{CC}=5.25\text{V}, V_I=4.5\text{V}$ (Output control)	—	27	40	$\text{mA}$	
Input clamp voltage	$V_{IK}$	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	-1.5	V	

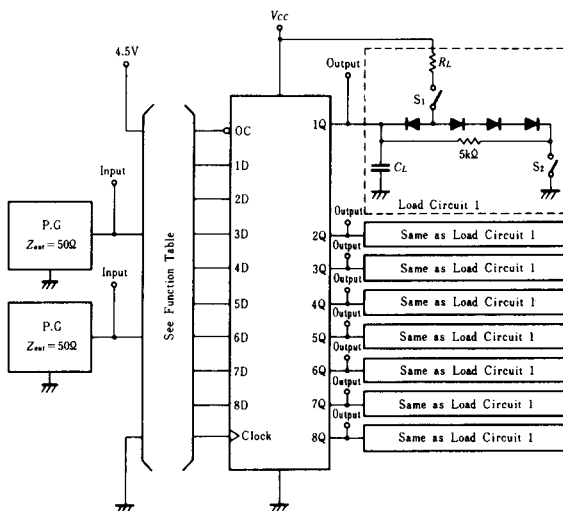
\*  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

## ■ SWITCHING CHARACTERISTICS ( $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$ )

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	$f_{max}$	Clock	Q	$C_L=45\text{pF}$ $R_L=667\Omega$	35	50	—	MHz
Propagation delay time	$t_{PLH}$	Clock	Q		—	15	28	
	$t_{PHL}$				—	19	28	
Output enable time	$t_{ZH}$	OC	Q		—	20	28	
	$t_{ZL}$			—	21	28		
Output disable time	$t_{HZ}$	OC	Q	$C_L=5\text{pF}$ $R_L=667\Omega$	—	12	20	
	$t_{LZ}$			—	14	25		

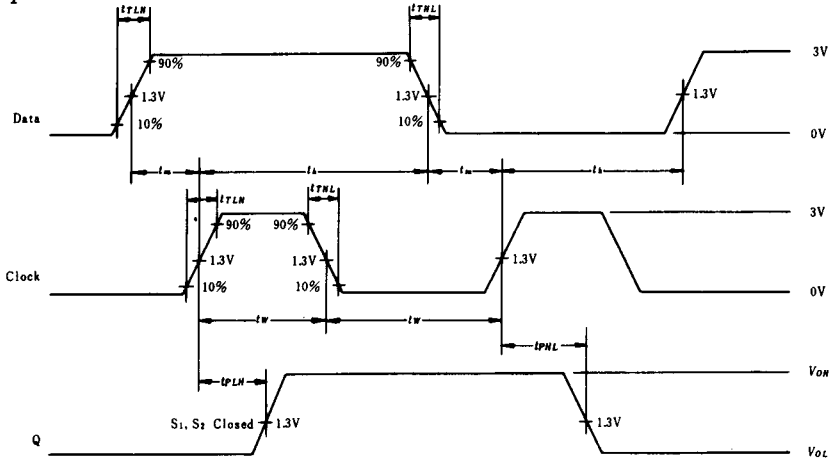
## ■ TESTING METHOD

Test Circuit



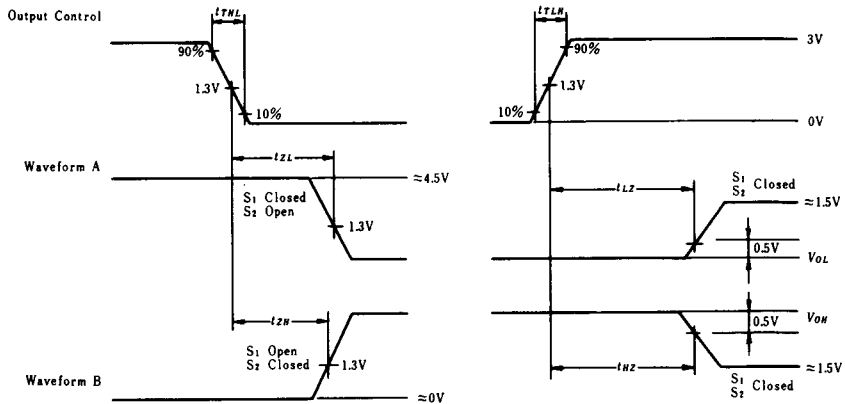
# HD74LS374

Waveform-1



- Notes:
1. Input pulse;  $t_{TLH} = 15\text{ns}$ ,  $t_{TFL} = 6\text{ns}$   
 Clock input;  $PRR = 1\text{MHz}$ , duty cycle 50%  
 Data input;  $PRR = 500\text{kHz}$ , duty cycle 50%
  2.  $f_{max}$ ;  $t_{TLH} = 2.5\text{ns}$ ,  $t_{TFL} = 2.5\text{ns}$

Waveform-2



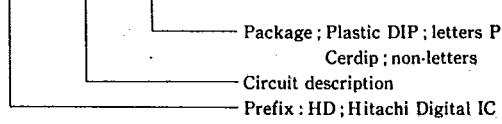
- Notes:
1. Input pulse;  $t_{TLH} = 15\text{ns}$ ,  $t_{TFL} = 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , duty cycle 50%
  2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

# PACKAGING INFORMATION

T-90-20

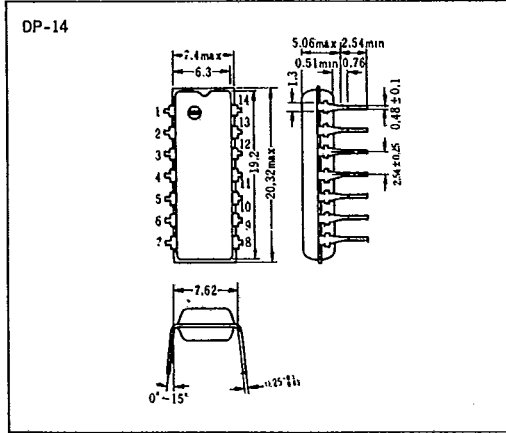
Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

## HD 74LS00 P

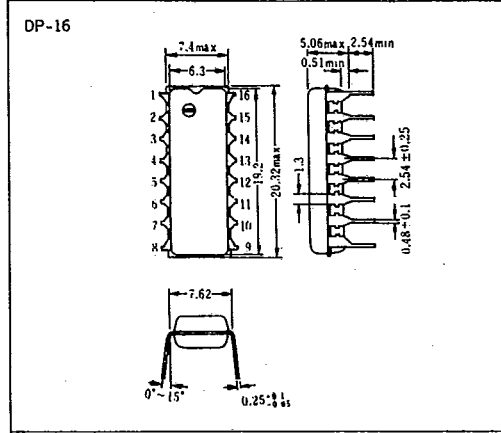


### ■ Plastic DIP

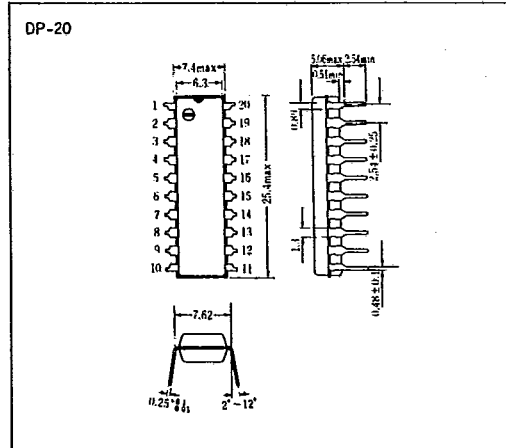
#### ● 14 Pin



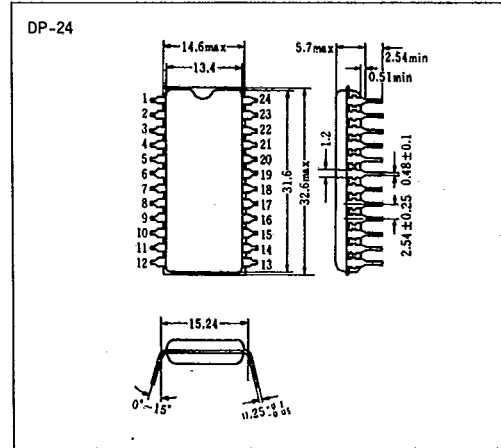
#### ● 16 Pin



#### ● 20 Pin



#### ● 24 Pin

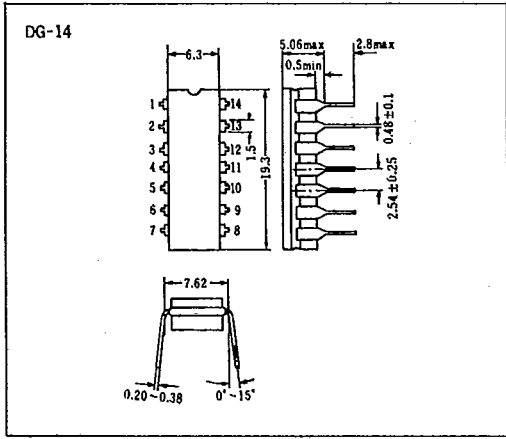


T-90-20

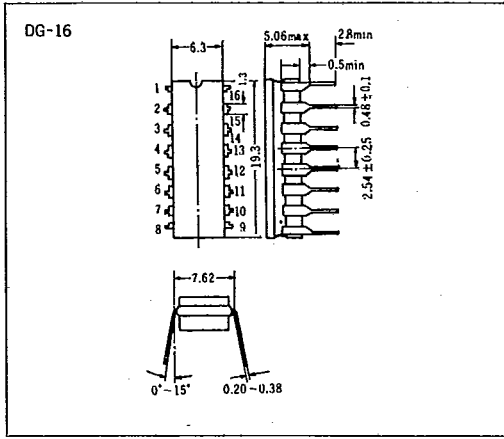
PACKAGING INFORMATIONS

■ Cerdip

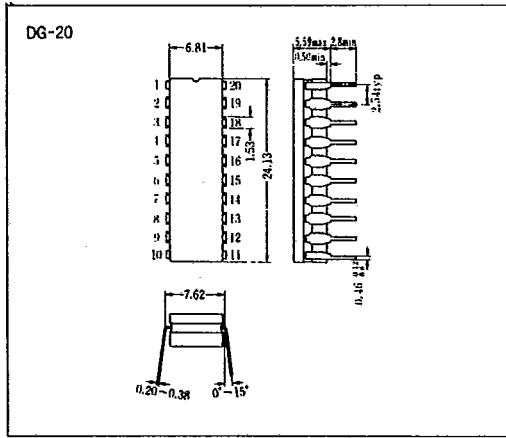
● 14 Pin



● 16 Pin



● 20 Pin



● 24 Pin

