1kHz - 68MHz Serial Port Programmable Oscillator

FEATURES

- **1kHz to 68MHz Square Wave Output**
- **0.5% (Typ) Initial Frequency Accuracy**
- **Frequency Error <1.1% Over All Settings**
- 0.1% Resolution
- 1.7mA Typical Supply Current (f < 1MHz, V_S = 3V)
- 3V to 5.5V Single Supply Operation
- Jitter <0.4% Typical 1kHz to 8MHz
- Easy to Use SPI (LTC6903) or I^2C (LTC6904) Serial Interface
- Output Enable Pin
- MS8 Package

APPLICATIONS

- Precision Digitally Controlled Oscillator
- Power Management
- Direct Digital Frequency Synthesis (DDS) Replacement
- Replacement for DAC and VCO
- Switched Capacitor Filter Clock

DESCRIPTION

The LTC®6903/LTC6904 are low power self contained digital frequency sources providing a precision frequency from 1kHz to 68MHz, set through a serial port. The LTC6903/LTC6904 require no external components other than a power supply bypass capacitor, and they operate over a single wide supply range of 3V to 5.5V.

The LTC6903/LTC6904 feature a proprietary feedback loop that linearizes the relationship between digital control setting and frequency, resulting in a very simple frequency setting equation:

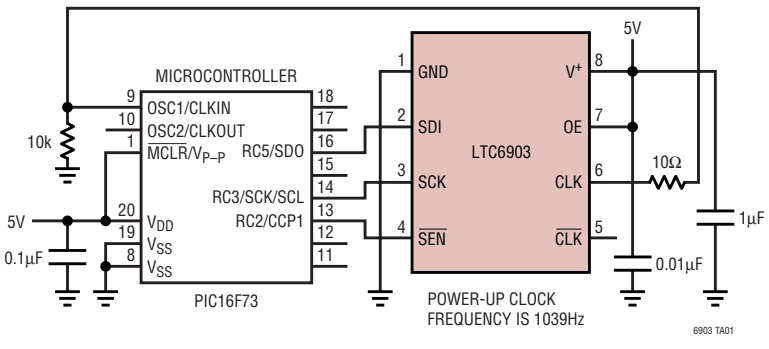
$$f = 2^{OCT} \bullet \frac{2078(Hz)}{\left(2 - \frac{DAC}{1024}\right)}; 1kHz < f < 68MHz$$

Where OCT is a 4-bit digital code and DAC is a 10-bit digital code.

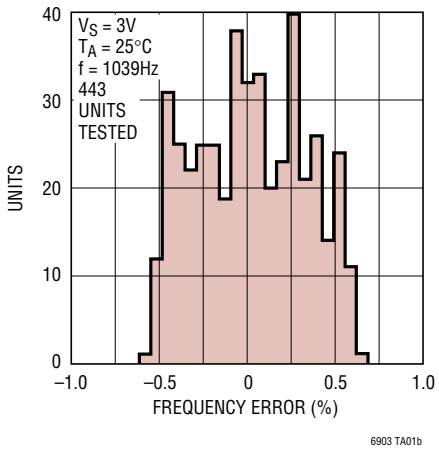
The LTC6903 is controlled by a convenient SPI compatible serial interface. The LTC6904 uses an industry standard I^2C compatible interface.

TYPICAL APPLICATION

A Microcontroller Controlling Its Clock



LTC6903 Frequency Error Distribution

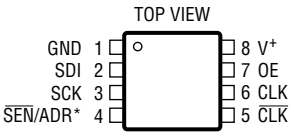


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to GND) 6V
Maximum Voltage on any Pin
..... (GND – 0.3V) ≤ VPIN ≤ (V^+ + 0.3V)
Output Short Circuit Duration (Note 2) ..... Indefinite
Operating Temperature Range
LTC6903CMS8/LTC6904CMS8 ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 200°C/W

* SEN (LTC6903)
ADR (LTC6904)

ORDER PART NUMBER
LTC6903CMS8 LTC6904CMS8
MS8 PART MARKING
LTABM LTAER

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V^+ = 3V, GND = 0V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Δfi	Initial Frequency Accuracy	f = 1.039kHz, V^+ = 3V, C_{LOAD} = 5pF				±0.75	%
Δf	Total Frequency Accuracy	Single Output Active					
		Over All Settings, V^+ = 3V, C_{LOAD} = 5pF	●		±0.5	±2	%
		Over All Settings, V^+ = 5.5V, C_{LOAD} = 5pF	●		±0.5	±2.25	%
		Over All Settings, V^+ = 3V			±0.5	±1.1	%
		Over All Settings, V^+ = 5.5V			±0.5	±1.6	%
f_{MAX}	Maximum Operating Frequency				68		MHz
f_{MIN}	Minimum Operating Frequency				1.039		kHz
Δf/ΔT	Frequency Drift Over Temperature				0.02		%/°C
Δf/ΔV	Frequency Drift Over Supply				0.05		%/V
	Long Term Frequency Stability				300		ppm/√kHr
	Timing Jitter (See Graph)	1.039kHz to 8.5MHz			0.4		%
		1.039kHz to 68MHz			1		%
	Duty Cycle	1.039kHz to 1MHz	●	49	50	51	%
		1.039kHz to 68MHz			50		%
R_{OUT}	Output Resistance	CLK, $\overline{CLK}$ Pins, V^+ = 3V			45		Ω
V_{OH}	High Level Output Voltage	V^+ = 5.5V, 4mA Load	●	4.8	5.3		V
		V^+ = 3V, 4mA Load	●	2.3	2.6		V
		V^+ = 5.5V, 1mA Load	●	5.2	5.45		V
		V^+ = 3V, 1mA Load	●	2.6	2.85		V
V_{OL}	Low Level Output Voltage	V^+ = 5.5V, 4mA Load	●		0.15	0.3	V
		V^+ = 3V, 4mA Load	●		0.25	0.4	V
		V^+ = 5.5V, 1mA Load	●		0.05	0.15	V
		V^+ = 3V, 1mA Load	●		0.05	0.2	V
t_r	Output Rise Time (10% - 90%)	V^+ = 5.5V, R_{LOAD} = ∞, C_{LOAD} = 5pF			1		ns
		V^+ = 3V, R_{LOAD} = ∞, C_{LOAD} = 5pF			1		ns
t_f	Output Fall Time (10% - 90%)	V^+ = 5.5V, R_{LOAD} = ∞, C_{LOAD} = 5pF			1		ns
		V^+ = 3V, R_{LOAD} = ∞, C_{LOAD} = 5pF			1		ns

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V^+ = 3V, GND = 0V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_S	Supply Voltage	Applied Between V^+ and GND	●	3		5.5	V
I_S, SHDN	V^+ Supply Current, Shutdown	V_S = 3V V_S = 5.5V	● ●		0.25 0.6	0.6 2.2	mA mA
I_S, DC	V^+ Supply Current, Single Output Enabled	f = 68MHz, 5pF Load, V^+ = 3V f < 1MHz, V^+ = 3V f = 68MHz, 5pF Load, V^+ = 5.5V f < 1MHz, V^+ = 5.5V	● ● ● ●		3.6 1.7 7 1.9	7 3.1 15 4.2	mA mA mA mA

SERIAL PORT ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V^+ = 3V, GND = 0V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Min High Level Input Voltage $\overline{SEN}$, SCK, SDI Pins		●			0.67 V^+	V
V_{IL}	Max Low Level Input Voltage $\overline{SEN}$, SCK, SDI Pins		●	0.33 V^+			V
I_{IN}	Digital Input Leakage $\overline{SEN}$, SCK, SDI Pins		●			10	µA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, GND = 0V

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
LTC 6903 (Notes 2, 3)						
f_{SCK}	Serial Port Clock Frequency	●			20	MHz
t_{CKHI}	Min Clock High Time	●			25	ns
t_{CKLO}	Min Clock Low Time	●			25	ns
t_{su}	Min Setup Time - SDI to SCK	●			10	ns
t_{hLD}	Min Hold Time - SCK to SDI	●			10	ns
t_{LCH}	Min Latch Time - $\overline{SEN}$ to $\overline{SEN}$	●			400	ns
t_{FCK}	Min First Clock - $\overline{SEN}$ to SCK	●			20	ns
LTC 6904 (Notes 2, 3)						
f_{SMB}	SMBus Operating Frequency	●	10		100	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	●	4.7			µs
$t_{HD, STA}$	Hold Time After (Repeated) Start Condition	●	4.0			µs
$t_{SU, STA}$	Repeated Start Condition Setup Time	●	4.7			µs
$t_{SU, STO}$	Stop Condition Setup Time	●	4.0			µs
$t_{HD, DAT}$	Data Hold Time	●	300			ns
$t_{SU, DAT}$	Data Setup Time	●	250			ns
t_{LOW}	Clock Low Period	●	4.7			µs
t_{HIGH}	Clock High Period	●	4.0		50	µs
t_f	Clock, Data Fall Time	●			300	ns
t_r	Clock, Data Rise Time	●			1000	ns

TIMING CHARACTERISTICS

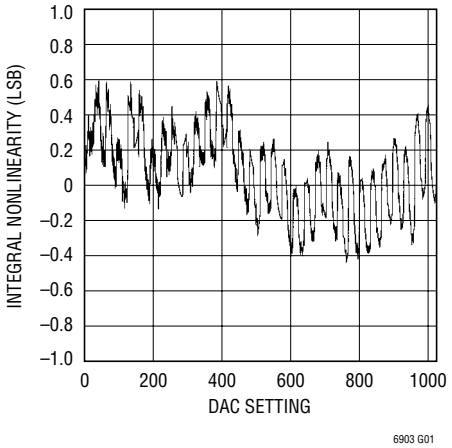
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All values are referenced to V_{IH} and V_{IL} levels.

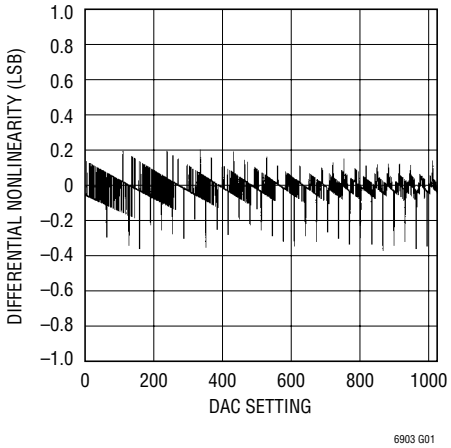
Note 3: Guaranteed by design and not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

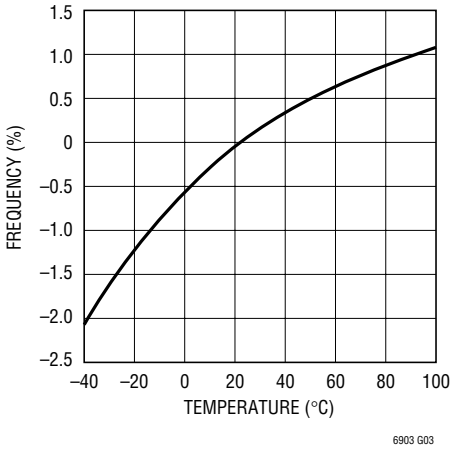
Integral Nonlinearity



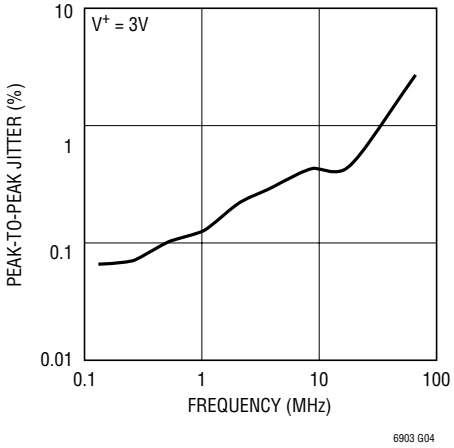
Differential Nonlinearity



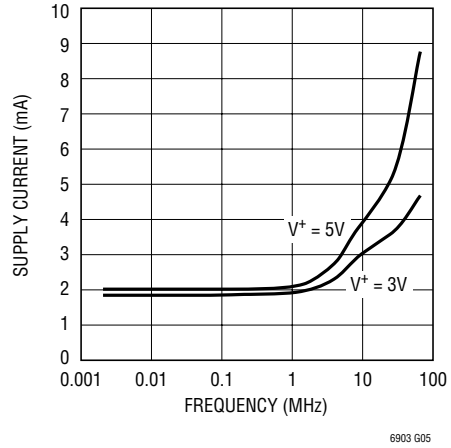
Frequency Variation over Temperature



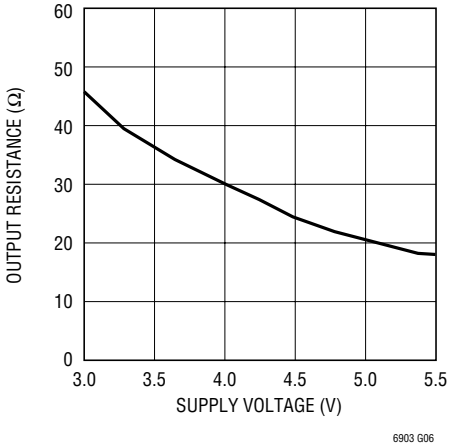
Peak-to-Peak Jitter vs Frequency



Supply Current vs Output Frequency

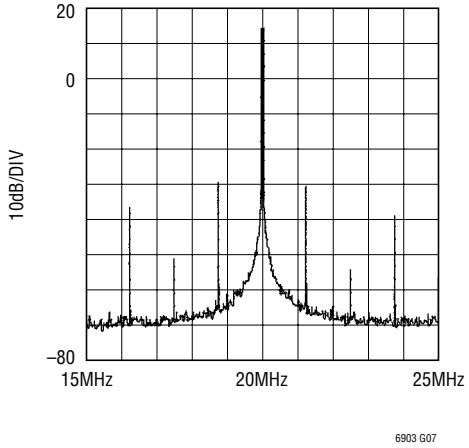


Output Resistance vs Supply Voltage

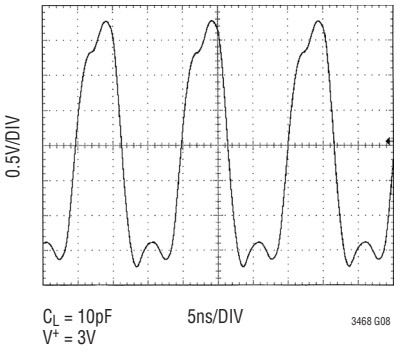


TYPICAL PERFORMANCE CHARACTERISTICS

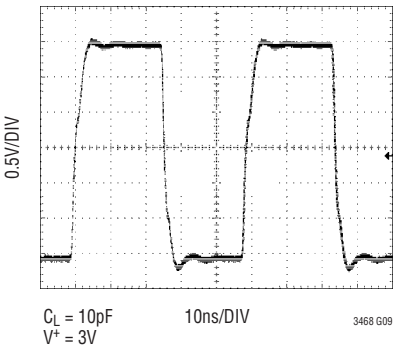
Output Spectrum at 20MHz



Output Waveform at 68MHz



Output Waveform at 20MHz



PIN FUNCTIONS

GND (Pin 1): Negative Power Supply (Ground). Should be tied directly to a ground plane for best performance.

SDI (Pin 2): Serial Data Input. Data for serial transfer is presented on this pin.

SCK (Pin 3): Serial Port Clock. Input, positive edge triggered. Clocks serial data in on rising edge.

$\overline{SEN}$ (Pin 4): Serial Port Enable (6903 Only). Input, active LOW. Initiates serial transaction when brought LOW, finalizes transaction when brought HIGH after 16 clocks.

ADR (Pin 4): Serial Port Address (6904 Only). Sets the I^2C serial port address.

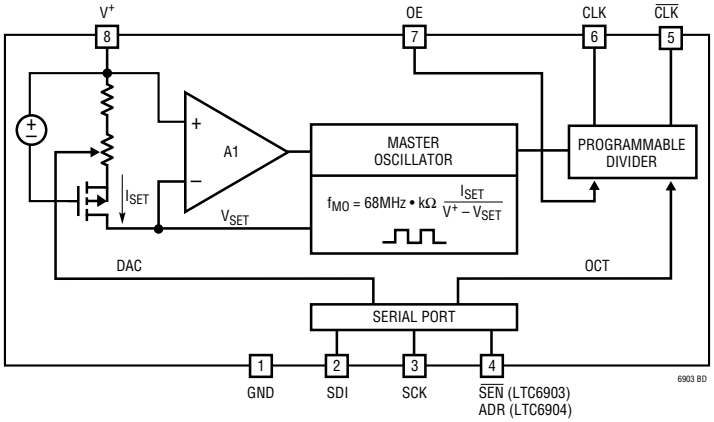
$\overline{CLK}$ (Pin 5): Auxiliary Clock Output. Frequency set by serial port.

CLK (Pin 6): Main Clock Output. Frequency set by serial port.

OE (Pin 7): Asynchronous Output Enable. CLK and $\overline{CLK}$ are set LOW when this pin is LOW.

V^+ (Pin 8): Positive Power Supply. This supply must be kept free from noise and ripple. It should be bypassed directly to a ground plane with a quality 0.1µF capacitor. Additional bypass may be necessary for operation at high frequency or under larger loads.

BLOCK DIAGRAM



THEORY OF OPERATION

The LTC6903/LTC6904 contain an internal feedback loop which controls a high frequency square wave VCO operating between 34MHz and 68MHz. The internal feedback loop frequency is set over an octave by a 10-bit resistor DAC. The VCO tracks the internal feedback loop frequency and the output frequency of the VCO is divided by one of sixteen possible powers of two.

Higher VCO frequencies and lower output divider settings can result in higher output jitter. Random jitter at the lower frequency ranges is very low because of the high output divisor.

The higher frequency settings will display some deterministic jitter from coupling between the control loop and the output. This shows up in the frequency spectrum as spurs separated from the fundamental frequency by 1MHz to 2MHz.

APPLICATIONS INFORMATION

Frequency Setting Information

The frequency output of the LTC6903/LTC6904 is determined by the following equation:

$$f = 2^{OCT} \bullet \frac{2078(Hz)}{\left(2 - \frac{DAC}{1024}\right)}$$

where DAC is the integer value from 0-1023 represented by the serial port register bits DAC[9:0] and OCT is the integer value from 0-15 represented by the serial port register bits OCT [3:0].

Use the following two steps to choose binary numbers "OCT" and "DAC" in order to set frequency "f":

1) Use Table 1 to Choose "OCT" or use the following formula, rounding down to the integer value less than or equal to the result.

$$OCT = 3.322\log\left(\frac{f}{1039}\right)$$

2) Choose "DAC" by the following formula, rounding DAC to the nearest integer:

$$DAC = 2048 - \frac{2078(Hz) \bullet 2^{(10+OCT)}}{f}$$

Table 1. Output Frequency Range vs OCT Setting (Frequency Resolution 0.001 • f)

f ≥	f <	OCT
34.05MHz	68.03MHz	15
17.02MHz	34.01MHz	14
8.511MHz	17.01MHz	13
4.256MHz	8.503MHz	12
2.128MHz	4.252MHz	11
1.064MHz	2.126MHz	10
532kHz	1063kHz	9
266kHz	531.4kHz	8
133kHz	265.7kHz	7
66.5kHz	132.9kHz	6
33.25kHz	66.43kHz	5
16.62kHz	33.22kHz	4
8.312kHz	16.61kHz	3
4.156kHz	8.304kHz	2
2.078kHz	4.152kHz	1
1.039kHz	2.076kHz	0

For example, to set a frequency of 6.5MHz, first look at Table 1 to find an OCT value. 6.5MHz falls between 4.25MHz and 8.5MHz yielding an OCT value of 12 or 1100. Substituting the OCT value of 12 and the desired frequency of 6.5MHz into the previous equation results in:

$$DAC = 2048 - \frac{2078(Hz) \bullet 2^{(10+12)}}{6.5e6(Hz)} = 707.113$$

APPLICATIONS INFORMATION

Rounding 707.113 to the nearest integer yields a DAC value of 707 (or a 10-bit digital word of 1011000011.)

Power Up State

When power is first applied to the LTC6903/LTC6904, all register values are automatically reset to 0. This results in an output frequency of 1.039kHz with both outputs active.

Output Spectrum

In most frequency ranges, the output of the LTC6903/LTC6904 is generated as a division of the higher internal clock frequency. This helps to minimize jitter and subharmonics at the output of the device. In the highest frequency ranges, the division ratio is reduced, which will result in greater cycle-to-cycle jitter as well as spurs at the internal sampling frequency. Because the internal control loop runs at 1MHz to 2MHz without regard to the output frequency, output spurs separated from the set frequency by 1MHz to 2MHz may be observed. These spurs are characteristically more than 30dB below the level of the set frequency.

Frequency Settling

When frequency settings change, the settling time and shape differ depending on which bits are changed. Changing only the OCT bits will result in an instantaneous change in frequency for OCT values below 10. Values of 10 and above may take up to 100µs to settle due to the action of internal power conservation circuitry.

Changing the DAC bits will result in a smooth transition between the frequencies, occupying at most 100µs, with little overshoot.

Changing both the OCT and DAC bits simultaneously may result in considerable excursion beyond the frequencies requested before settling.

It should be noted that changing the DAC bits at the lower frequency ranges will result in a seemingly instantaneous frequency change because the settling time depends on the internal loop frequency rather than the set frequency.

Power Supply Bypass

In order to obtain the accuracies represented in this datasheet, it is necessary to provide excellent bypass on the power supply. Adequate bypass is a 1µF capacitor in parallel with a 0.01µF capacitor connected within a few millimeters of the power supply leads.

Monotonicity and Linearity

The DAC in the LTC6903/LTC6904 is guaranteed to be 10-bit monotonic. Nonlinearity of the DAC is less than 1%.

Additionally, the LTC6903/LTC6904 is guaranteed to be monotonic when switching between octaves with the OCT setting bits. For example, the frequency output with a DAC setting of “1111111111” and an OCT setting of “1100” will always be lower than the frequency output with a DAC setting of “0000000000” and an OCT setting of “1101”. Linearity at these transition points is typically around 3 LSBs.

Output Loading and Accuracy

Improper loading of the outputs of the LTC6903/LTC6904, especially with poor power supply bypassing, will result in accuracy problems. At low frequencies, capacitive loading of the output is not a concern. At frequencies above 1MHz, attention should be paid to minimize the capacitive load on the CLK and $\overline{CLK}$ pins.

The LTC6903/LTC6904 is designed to drive up to 5pF on each output with no degradation in accuracy. 5pF is equivalent to one to two HC series logic inputs. A standard 10x oscilloscope probe usually presents between 10pF and 15pF of capacitive load.

It is strongly suggested that a high speed buffer is used when driving more than one or two logic inputs, when driving a line more than 5 centimeters in length, or a capacitive load greater than 5pF.

APPLICATIONS INFORMATION

Output Control

The CLK and $\overline{CLK}$ outputs of the LTC6903/LTC6904 are individually controllable through the serial port as described in Table 2 below. The low power mode may also be accessed through these control bits. It is preferred that unused outputs be disabled in order to reduce power dissipation and improve accuracy.

Disabling an unused output will improve accuracy of operation at frequencies above 1MHz. An unused output running with no load typically degrades frequency accuracy up to 0.2% at 68MHz. An unused output running into a 5pF load typically degrades frequency accuracy up to 0.5% at 68MHz.

Table 2. Output Configuration

CNF1	CNF0	CLK	$\overline{CLK}$
0	0	ON	CLK + 180°
0	1	OFF	ON
1	0	ON	OFF
1	1	Powered-Down*	

* Powered-Down: When in this mode, the chip is in a low power state and will require approximately 100µs to recover. This is not the same effect as the OE pin, which is fast, but uses more power supply current.

Serial Port Bitmap (LTC6903/LTC6904)

(All serial port register bits default LOW at power up)

Table 3

D15	D14	D13	D12	D11	D10	D9	D8
OCT3	OCT2	OCT1	OCT0	DAC9	DAC8	DAC7	DAC6
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DAC5	DAC4	DAC3	DAC2	DAC1	DAC0	CNF1	CNF0

Serial Port Register Description

OCT[3:0] - Frequency Divider Setting. (See Frequency Setting Section)

DAC[9:0] - Master Oscillator Frequency Setting. (See Frequency Setting Section)

CNF[1:0] - Output Configuration - This controls outputs CLK and $\overline{CLK}$ according to Table 2.

LTC6903 SPI Compatible Interface

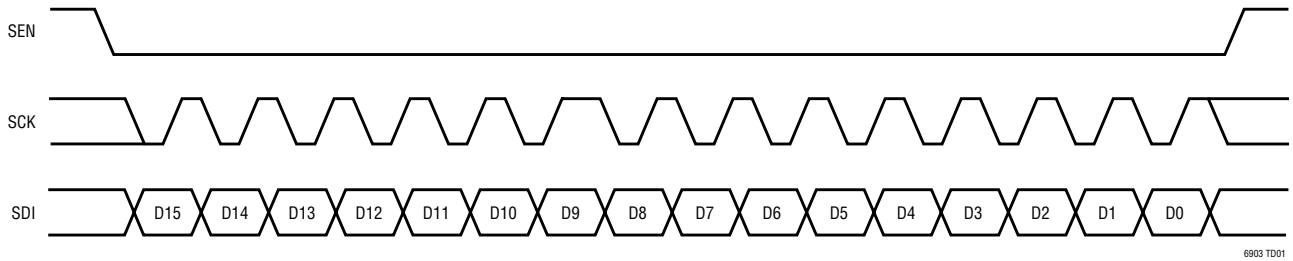
A serial data transfer is composed of sixteen (16) bits of data labeled D15 through D0. D15 is the first bit of data presented in each transaction. All serial port register bits are set LOW on power-up.

Writing Data (LTC6903 Only)

When the $\overline{SEN}$ line is brought LOW, serial data presented on the SDI input is clocked in on the rising edges of SCK until $\overline{SEN}$ is brought HIGH. On every eighth rising edge of SCK, the preceding 8-bits of data are clocked into the internal register. It is therefore possible to clock in only the 8 {D15 - D8} most significant bits of data rather than completing an entire transfer.

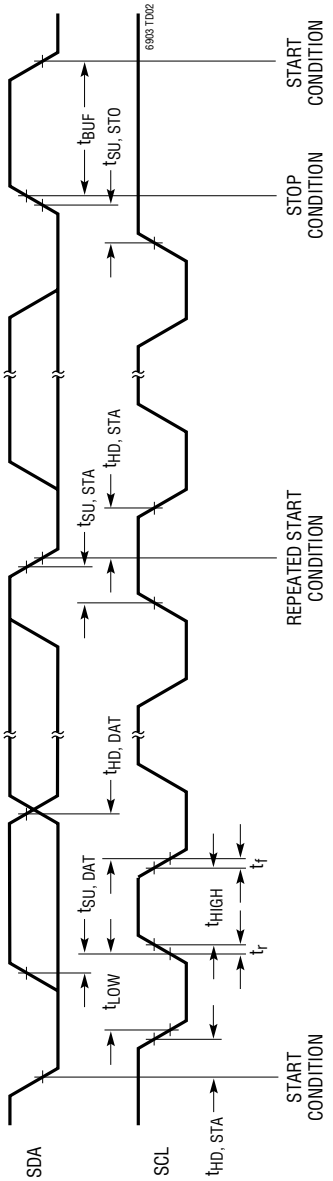
The serial data transfer starts with the most significant bit and ends with the least significant bit of the data, as shown in the timing diagram.

Timing Diagram (LTC6903)

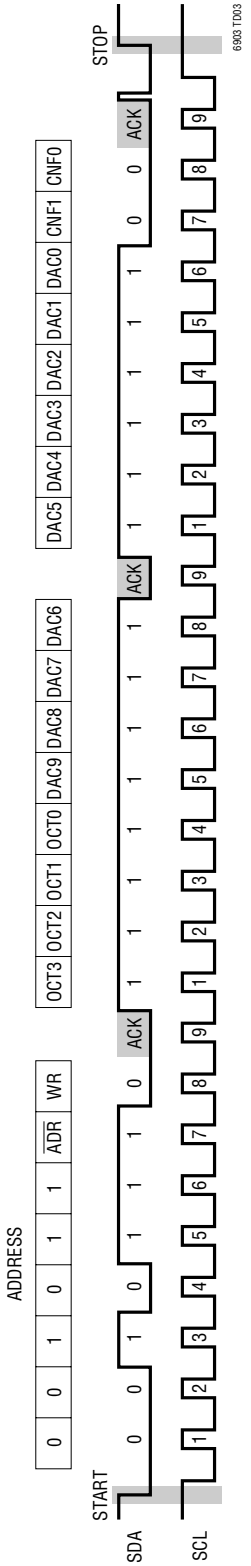


TIMING DIAGRAMS

Timing Diagram (LTC6904)



Typical LTC6904 Input Waveform—Programming Frequency to 68MHz ($\overline{ADR}$ Pin Set LOW)



TYPICAL APPLICATIONS

LTC6904 I²C Interface

The LTC6904 communicates with a host (master) using the standard I²C 2-wire interface. The Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus Accelerator, are required on these lines.

The LTC6904 is a receive-only (slave) device. The master can communicate with the LTC6904 using the Write Word protocols as explained later.

The START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a communication to a slave device by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high.

When the master has finished communicating with the slave, it issues a STOP condition. A STOP condition is generated by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another SMBus device.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave lets the master know that the latest byte of information was received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock pulse. The slave-receiver must pull down the SDA line during the Acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse.

Write Word Protocol

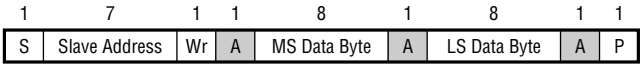
The master initiates communication with the LTC6904 with a START condition and a 7-bit address followed by the Write Bit (Wr) = 0. The LTC6904 acknowledges and the master delivers the most significant data byte. Again the LTC6904 acknowledges and the data is latched into the most significant data byte input register. The master then delivers the least significant data byte. The LTC6904 acknowledges once more and latches the data into the least significant data byte input register. Lastly, the master terminates the communication with a STOP condition.

Slave Address

The LTC6904 can respond to one of two 7-bit addresses. The first 6 bits (MSBs) have been factory programmed to 001011. The address pin, ADR (Pin 4) is programmed by the user and determines the LSB of the slave address, as shown in the table below:

ADR (Pin 4)	LTC6904 Address
0	0010111
1	0010110

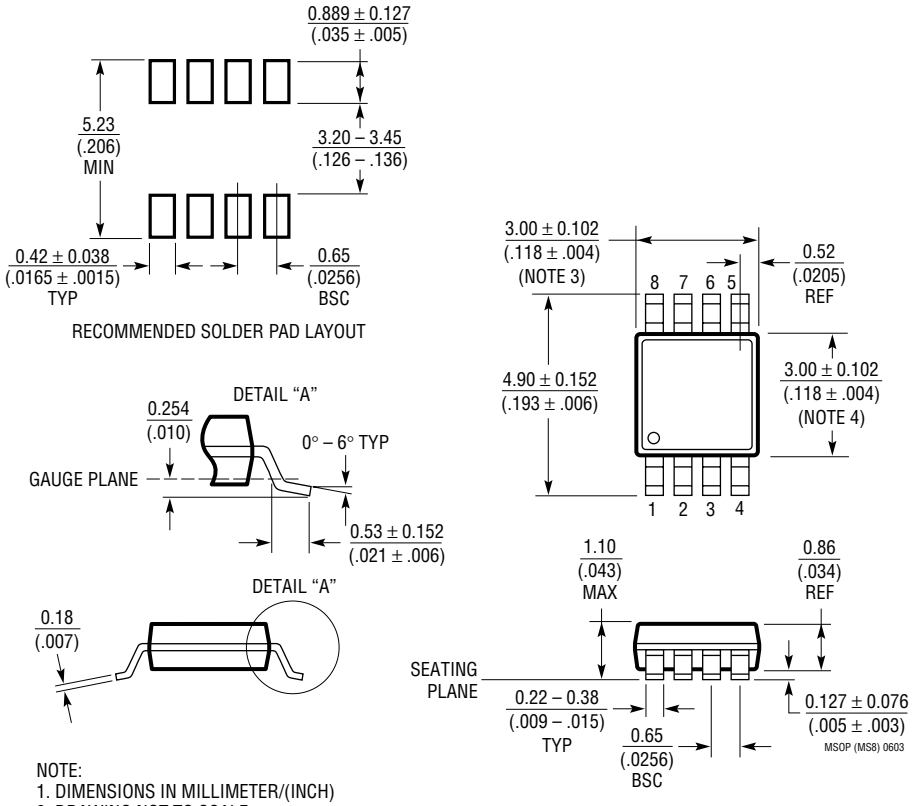
Write Word Protocol Used by the LTC6904



S = Start Condition, Wr = Write Bit = 0, A = Acknowledge, P = Stop Condition 6903 AI01

PACKAGE DESCRIPTION

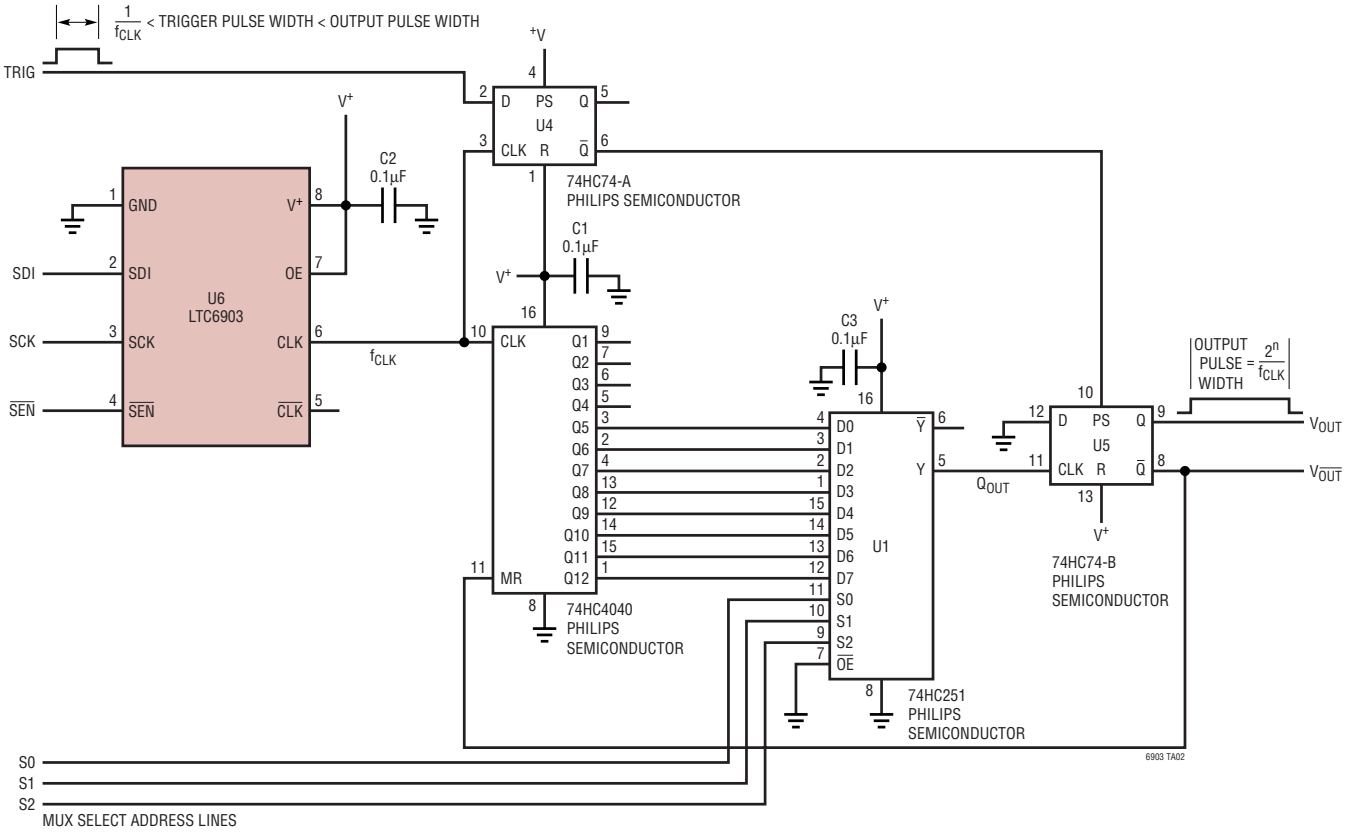
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Wide Range Time Interval Generator (1.97 Seconds to 4 Microseconds)



MUX Inputs				
S2	S1	S0	n	Output Pulsewidth
0	0	0	4	$16/f_{CLK}$
1	0	0	5	$32/f_{CLK}$
0	1	0	6	$64/f_{CLK}$
1	1	0	7	$128/f_{CLK}$
0	0	1	8	$256/f_{CLK}$
1	0	1	9	$512/f_{CLK}$
0	1	1	10	$1024/f_{CLK}$
1	1	1	11	$2048/f_{CLK}$

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1799	1kHz to 30MHz ThinSOT™ Oscillator	Single Output, Higher Frequency Operation
LTC6900	1kHz to 20MHz ThinSOT Oscillator	Single Output, Lower Power
LTC6902	Multiphase Oscillator with Spread Spectrum Modulation	2, 3 or 4-Phase Outputs

ThinSOT is a trademark of Linear Technology Corporation

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