



# Octal, 14-Bit Voltage-Output DAC with Parallel Interface for ATE

MAX5264

## General Description

The MAX5264 contains eight 14-bit, voltage-output digital-to-analog converters (DACs). On-chip precision output amplifiers provide the voltage outputs. The device operates from +14V/-9V supplies. Its bipolar output voltage swing ranges from +9V to -4V and is achieved with no external components. The MAX5264 has three pairs of differential reference inputs; two of these pairs are connected to two DACs each, and a third pair is connected to four DACs. The references are independently controlled, providing different full-scale output voltages to the respective DACs. The MAX5264 operates within the following voltage ranges:  $V_{DD} = +7V$  to +14V,  $V_{SS} = -5V$  to -9V, and  $V_{CC} = +4.75V$  to +5.25V.

The MAX5264 features double-buffered interface logic with a 14-bit parallel data bus. Each DAC has an input latch and a DAC latch. Data in the DAC latch sets the output voltage. The eight input latches are addressed with three address lines. Data is loaded to the input latch with a single write instruction. An asynchronous load input ( $\overline{LD}$ ) transfers data from the input latch to the DAC latch. The  $\overline{LD}$  input controls all DACs; therefore, all DACs can be updated simultaneously by asserting the  $\overline{LD}$  pin.

An asynchronous  $\overline{CLR}$  input sets the output of all eight DACs to the respective DUTGND input of the op amp. Note that  $\overline{CLR}$  is a CMOS input, which is powered by  $V_{DD}$ . All other logic inputs are TTL/CMOS compatible.

The "A" grade of the MAX5264 has a maximum INL of  $\pm 4$ LSBs, while the "B" grade has a maximum INL of  $\pm 8$ LSBs. Both grades are available in 44-pin MQFP packages.

## Applications

- Automatic Test Equipment (ATE)
- Industrial Process Controls
- Arbitrary Function Generators
- Avionics Equipment
- Minimum Component Count Analog Systems
- Digital Offset/Gain Adjustment
- SONET Applications

Functional Diagram appears at end of data sheet.

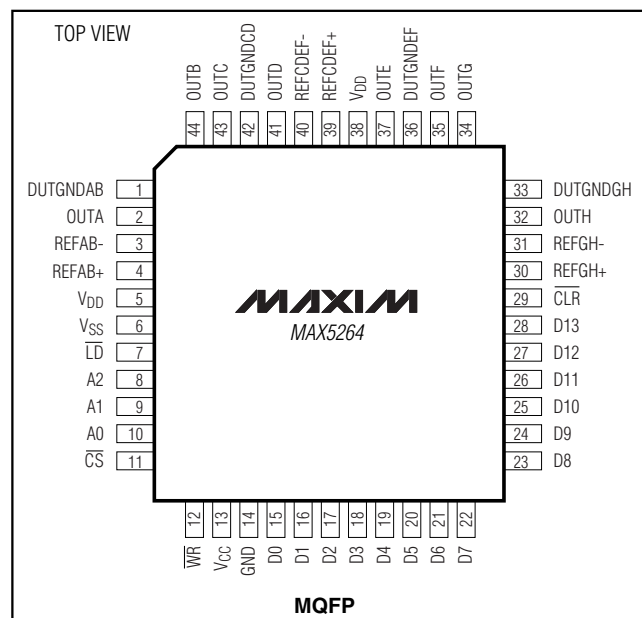
## Features

- ◆ Full 14-Bit Performance Without Adjustments
- ◆ 8 DACs in a Single Package
- ◆ Buffered Voltage Outputs
- ◆ Unipolar or Bipolar Voltage Swing to +9V and -4V
- ◆ 22 $\mu$ s Output Settling Time
- ◆ Drives Up to 10,000pF Capacitive Load
- ◆ Low Output Glitch: 30mV
- ◆ Low Power Consumption: 10mA (typ)
- ◆ Small 44-Pin MQFP Package
- ◆ Double-Buffered Digital Inputs
- ◆ Asynchronous Load Updates All DACs Simultaneously
- ◆ Asynchronous  $\overline{CLR}$  Forces All DACs to DUTGND Potential

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5264ACMH	0°C to +70°C	44 MQFP	$\pm 4$
MAX5264BCMh	0°C to +70°C	44 MQFP	$\pm 8$

## Pin Configuration



Maxim Integrated Products 1

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# Octal, 14-Bit Voltage-Output DAC with Parallel Interface for ATE

## ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to GND	-0.3V to +16.8V	Maximum Current into Any Signal Pin	±50mA
V <sub>SS</sub> to GND	-10.8V to +0.3V	OUT_ Short-Circuit Duration to V <sub>DD</sub> , V <sub>SS</sub> , and GND	1s
V <sub>CC</sub> to GND	-0.3V to +6V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
A_, D_, WR, CS, LD, CLR to GND	+0.3V to (V <sub>CC</sub> + 0.3V)	44-Pin MQFP (derate 11.1mW/°C above +70°C)	870mW
REF_+_, REF_-_,		Operating Temperature Range	0°C to +70°C
DUTGND_	(V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V)	Junction Temperature	+150°C
OUT_	V <sub>DD</sub> to V <sub>SS</sub>	Storage Temperature Range	-65°C to +150°C
Maximum Current into REF_+, DUTGND_	±10mA	Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +14V, V<sub>SS</sub> = -9V, V<sub>CC</sub> = +5V, V<sub>GND</sub> = V<sub>DUTGND\_</sub> = 0, V<sub>REF\_+</sub> = +4.500V, V<sub>REF\_-</sub> = -2.000V, R<sub>L</sub> = 10kΩ, C<sub>L</sub> = 50pF, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>STATIC PERFORMANCE (ANALOG SECTION)</b>						
Resolution	N		14			Bits
Relative Accuracy	INL	MAX5264A			±4	LSB
		MAX5264B			±8	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Zero-Scale Error				±4	±8	LSB
Full-Scale Error				±8	±16	LSB
Gain Error				±4	±10	LSB
Gain Temperature Coefficient		(Note 1)		0.15	20	ppm FSR/°C
DC Crosstalk		(Note 1)		14	75	μV
<b>REFERENCE INPUTS</b>						
Input Resistance			1			MΩ
Input Current				±1	±10	μA
REF_+ Input Range			1.5		4.5	V
REF_- Input Range			-2.0		-1.5	V
(REF_+) - (REF_-) Range			3		6.5	V
V <sub>DD</sub> - (2 · V <sub>REF_+</sub> ) Range			3.5		8.5	V
(2 · V <sub>REF_-</sub> ) - V <sub>SS</sub> Range			3.5		5	V
V <sub>DD</sub> - (V <sub>REF_+</sub> ) Range			7.5		10	V
(V <sub>REF_-</sub> ) - V <sub>SS</sub> Range			5		7	V
<b>ANALOG OUTPUTS</b>						
Maximum Output Voltage			9	V <sub>DD</sub> - 2		V
Minimum Output Voltage				V <sub>SS</sub> + 2	-4	V
Resistive Load to GND			5			kΩ
Capacitive Load to GND		(Note 2)			10,000	pF
DC Output Impedance		(Note 1)			0.5	Ω

# Octal, 14-Bit Voltage-Output DAC with Parallel Interface for ATE

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +14V$ ,  $V_{SS} = -9V$ ,  $V_{CC} = +5V$ ,  $V_{GND} = V_{DUTGND\_} = 0$ ,  $V_{REF\_+} = +4.500V$ ,  $V_{REF\_} = -2.000V$ ,  $R_L = 10k\Omega$ ,  $C_L = 50pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DUTGND_ CHARACTERISTICS</b>						
Input Impedance per DAC			55	115		k $\Omega$
Input Current per DAC		(Note 1)	-120		73	$\mu A$
Input Range			-2		2	V
<b>DIGITAL INPUTS</b>						
Input Voltage High	$V_{IH}$		2.4			V
Input Voltage Low	$V_{IL}$				0.8	V
Input Capacitance	$C_{IN}$	(Note 1)			10	pF
Input Current	$I_{IN}$	$V_{IN} = 0$ or $V_{CC}$	-1		1	$\mu A$
<b>POWER SUPPLIES</b>						
$V_{DD}$ Analog Power-Supply Range	$V_{DD}$		11.5		14	V
$V_{SS}$ Analog Power-Supply Range	$V_{SS}$		-9		-6.5	V
$V_{DD} - V_{SS}$			18		23	V
Digital Power Supply	$V_{CC}$		4.75	5	5.25	V
Positive Supply Current	$I_{DD}$	$R_L = 10k\Omega$ , $V_{OUT\_} = 9V$ (Note 3)			20	mA
Negative Supply Current	$I_{SS}$	$R_L = 10k\Omega$ , $V_{OUT\_} = -4$ (Note 4)			20	mA
Digital Supply Current	$I_{CC}$	(Note 5)			0.5	mA
		(Note 6)			5	
PSRR, $\Delta V_{OUT} / \Delta V_{DD}$		$V_{DD} = 14V \pm 5\%$		94		dB
PSRR, $\Delta V_{OUT} / \Delta V_{SS}$		$V_{SS} = -9V \pm 5\%$		98		dB

## INTERFACE TIMING CHARACTERISTICS

( $V_{DD} = +14V$ ,  $V_{SS} = -9V$ ,  $V_{CC} = +5V$ ,  $V_{GND} = V_{DUTGND\_} = 0$ ,  $V_{REF\_+} = +4.500V$ ,  $V_{REF\_} = -2.000V$ , Figure 2,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width Low	$t_1$		50			ns
$\overline{WR}$ Pulse Width Low	$t_2$		50			ns
$\overline{LD}$ Pulse Width Low	$t_3$		50			ns
$\overline{CS}$ Low to $\overline{WR}$ Low	$t_4$		0			ns
$\overline{CS}$ High to $\overline{WR}$ High	$t_5$		0			ns
Data Valid to $\overline{WR}$ Setup	$t_6$		50			ns
Data Valid to $\overline{WR}$ Hold	$t_7$		0			ns
Address Valid to $\overline{WR}$ Setup	$t_8$		15			ns
Address Valid to $\overline{WR}$ Hold	$t_9$		0			ns

# Octal, 14-Bit Voltage-Output DAC with Parallel Interface for ATE

## DYNAMIC CHARACTERISTICS

( $V_{DD} = +14V$ ,  $V_{SS} = -9V$ ,  $V_{CC} = +5V$ ,  $V_{GND} = V_{DUTGND} = 0$ ,  $V_{REF\_+} = +4.500V$ ,  $V_{REF\_ -} = -2.000V$ ,  $R_L = 10k\Omega$ ,  $C_L = 50pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Settling Time		To $\pm 1$ LSB of full scale		22		$\mu s$
Output Slew Rate				1		$V/\mu s$
Digital Feedthrough		(Note 7)		3		nVs
Digital Crosstalk		(Note 8)		3		nVs
Digital-to-Analog Glitch Impulse				120		nVs
DAC-to-DAC Crosstalk				3		nVs
Channel-to-Channel Isolation				100		dB
Output Noise Spectral Density		At $f = 1kHz$		130		$nV/\sqrt{Hz}$

**Note 1:** Guaranteed by design. Not production tested.

**Note 2:** Guaranteed by design when  $220\Omega$  resistor is in series with  $C_L = 10,000pF$ .

**Note 3:** All DAC latches at full scale (0x3FFF).

**Note 4:** All DAC latches at zero scale (0x0000).

**Note 5:** All digital inputs ( $\overline{D}$ ,  $A$ ,  $\overline{WR}$ ,  $\overline{CS}$ ,  $\overline{LD}$ , and  $\overline{CLR}$ ) at GND or  $V_{CC}$  potential.

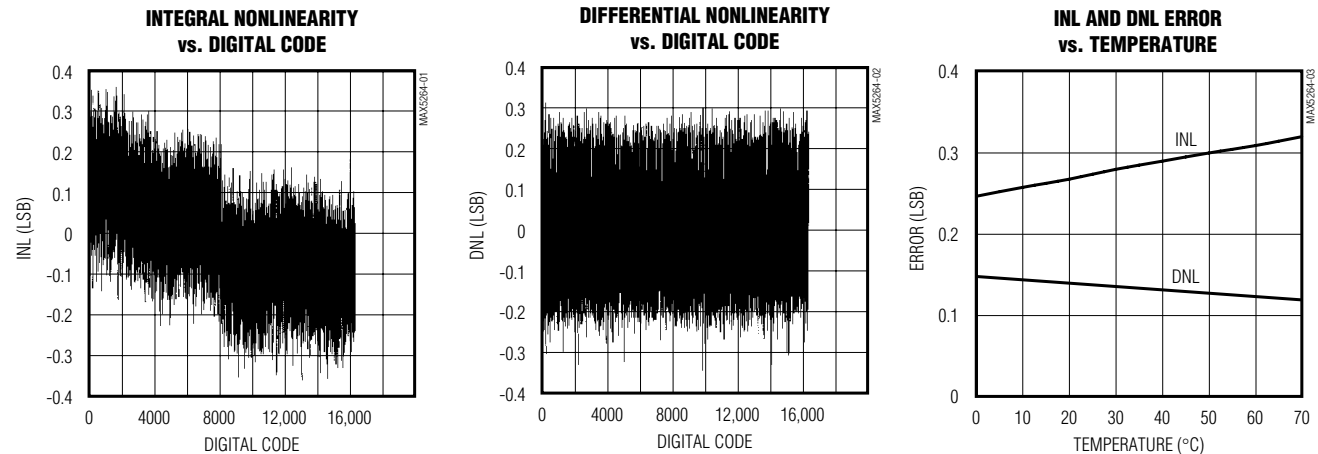
**Note 6:** All digital inputs ( $\overline{D}$ ,  $A$ ,  $\overline{WR}$ ,  $\overline{CS}$ ,  $\overline{LD}$ , and  $\overline{CLR}$ ) at +0.8V or +2.4V.

**Note 7:** All data inputs (D0 to D13) transition from GND to  $V_{CC}$ , with  $\overline{WR} = V_{CC}$ .

**Note 8:** All digital inputs ( $\overline{D}$ ,  $A$ ,  $\overline{WR}$ ,  $\overline{CS}$ ,  $\overline{LD}$ , and  $\overline{CLR}$ ) at +0.8V or +2.4V.

## Typical Operating Characteristics

( $V_{DD} = +14V$ ,  $V_{SS} = -9V$ ,  $V_{CC} = +5V$ ,  $V_{GND} = V_{DUTGND} = 0$ ,  $V_{REF\_+} = +4.500V$ ,  $V_{REF\_ -} = -2.000V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



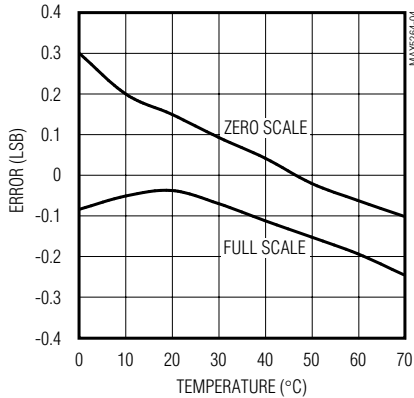
# Octal, 14-Bit Voltage-Output DAC with Parallel Interface for ATE

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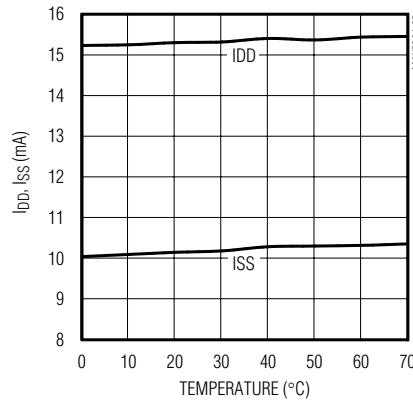
## Typical Operating Characteristics (continued)

( $V_{DD} = +14V$ ,  $V_{SS} = -9V$ ,  $V_{CC} = +5V$ ,  $V_{GND} = V_{DUTGND} = 0$ ,  $V_{REF\_+} = +4.500V$ ,  $V_{REF\_ -} = -2.000V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

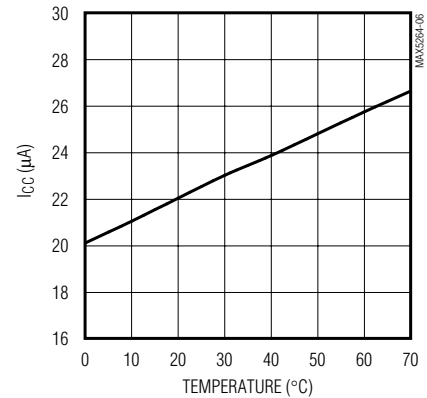
**ZERO-SCALE AND FULL-SCALE ERROR vs. TEMPERATURE**



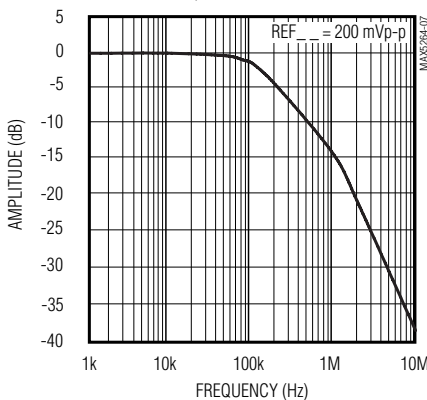
**$I_{DD}$  AND  $I_{SS}$  vs. TEMPERATURE (WITH 10k $\Omega$  LOADS)**



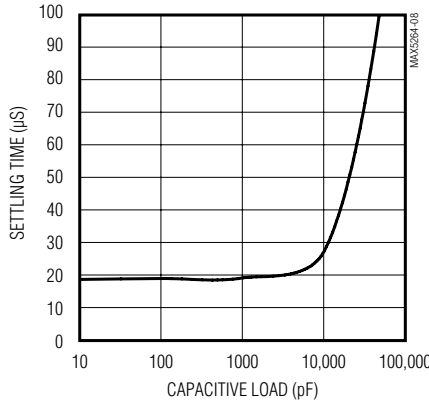
**DIGITAL SUPPLY CURRENT vs. TEMPERATURE**



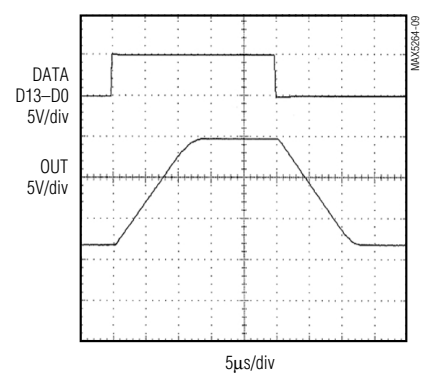
**REFERENCE INPUT FREQUENCY RESPONSE**



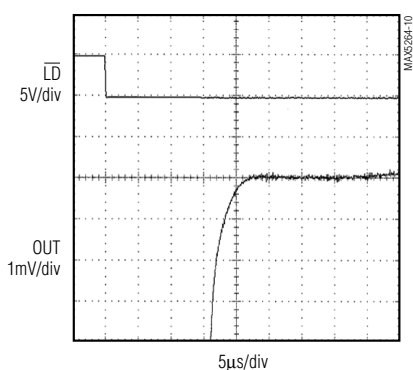
**SETTLING TIME vs. CAPACITIVE LOAD**



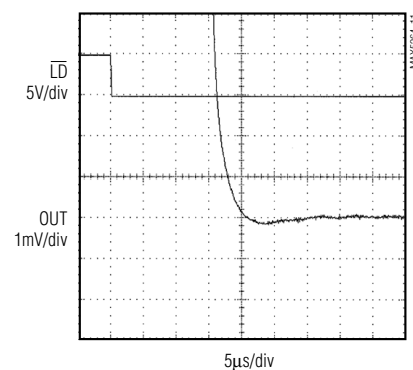
**LARGE-SIGNAL STEP RESPONSE**



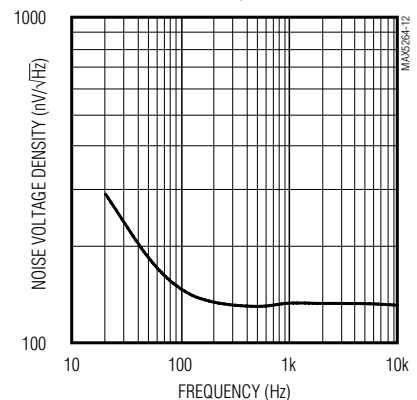
**POSITIVE SETTLING TIME**



**NEGATIVE SETTLING TIME**



**NOISE VOLTAGE DENSITY vs. FREQUENCY**

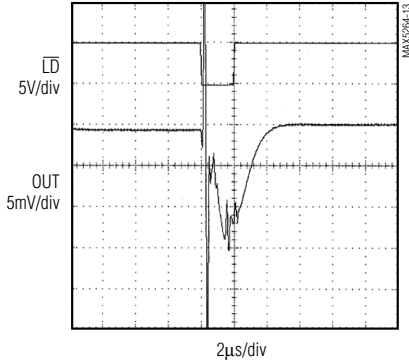


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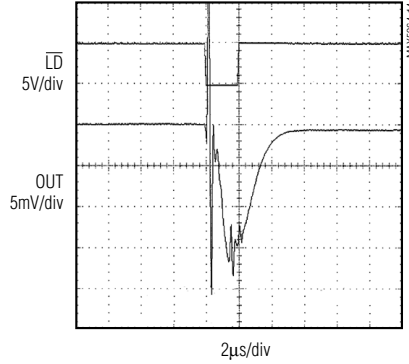
## Typical Operating Characteristics (continued)

( $V_{DD} = +14V$ ,  $V_{SS} = -9V$ ,  $V_{CC} = +5V$ ,  $V_{GND} = V_{DUTGND\_} = 0$ ,  $V_{REF\_} = +4.500V$ ,  $V_{REF\_} = -2.000V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

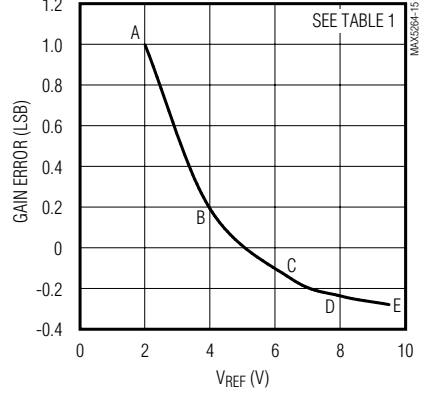
**MAJOR CARRY GLITCH IMPULSE  
(0 x 1FFF - 0 x 2000)**



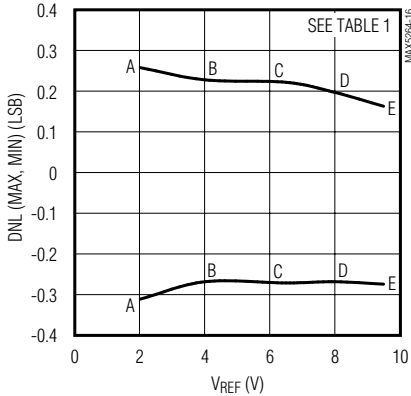
**MAJOR CARRY GLITCH IMPULSE  
(0 x 2000 - 0 x 1FFF)**



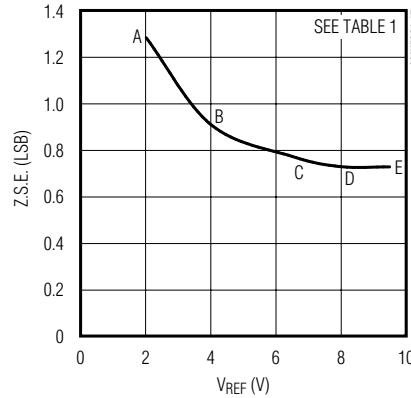
**GAIN ERROR  
vs.  $V_{REF}$  ( $V_{REF+} - V_{REF-}$ )**



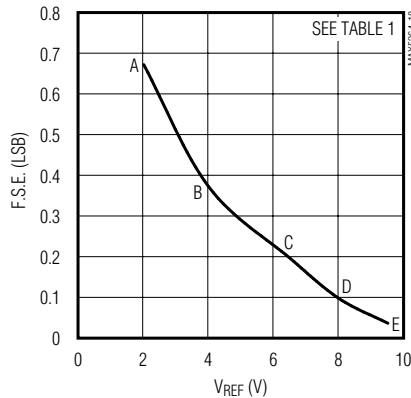
**DNL (MAX, MIN)  
vs.  $V_{REF}$  ( $V_{REF+} - V_{REF-}$ )**



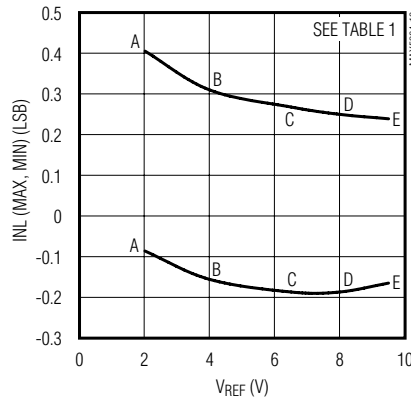
**Z.S.E.  
vs.  $V_{REF}$  ( $V_{REF+} - V_{REF-}$ )**



**F.S.E.  
vs.  $V_{REF}$  ( $V_{REF+} - V_{REF-}$ )**



**INL (MAX, MIN)  
vs.  $V_{REF}$  ( $V_{REF+} - V_{REF-}$ )**



# Octal, 14-Bit Voltage-Output DAC with Parallel Interface for ATE

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**Table 1. Test Conditions for Static Performance Typical Operating Characteristics**

VOLTAGE	A	B	C	D	E
V <sub>REF</sub>	2	4	6.5	8	9.5
V <sub>REF+</sub>	1	2.25	4.5	5	6
V <sub>REF-</sub>	-1	-1.75	-2	-3	-3.5
V <sub>DD</sub>	7	7	11	12	14
V <sub>SS</sub>	-5	-5.5	-6	-8	-9

**Note:**  $V_{REF} = V_{REF+} - V_{REF-}$

## Pin Description

PIN	NAME	FUNCTION
1	DUTGNDAB	Device Sense Ground Input for OUTA and OUTB. In normal operation, OUTA and OUTB are referenced to DUTGNDAB. When $\overline{CLR}$ is low, OUTA and OUTB are forced to the potential on DUTGNDAB.
2	OUTA	DAC A Buffered Output Voltage
3	REFAB-	Negative Reference Input for DACs A and B
4	REFAB+	Positive Reference Input for DACs A and B
5, 38	V <sub>DD</sub>	Positive Analog Power Supply. Normally set to +14V. Connect both pins to the supply voltage. See <i>Grounding and Bypassing</i> section for bypass requirements.
6	V <sub>SS</sub>	Negative Analog Power Supply. Normally set to -9V. See <i>Power Supplies, Grounding, and Bypassing</i> section for bypass requirements.
7	$\overline{LD}$	Load Input. Drive this asynchronous input low to transfer the contents of the input latches to their respective DAC latches. DAC latches are transparent when LD is low and latched when $\overline{LD}$ is high.
8	A2	Address Bit 2 (MSB)
9	A1	Address Bit 1
10	A0	Address Bit 0 (LSB)
11	$\overline{CS}$	Chip Select. Active-low input.
12	$\overline{WR}$	Write Input. Active-low strobe for conventional memory write sequence. Input data latches are transparent when $\overline{WR}$ and $\overline{CS}$ are both low. $\overline{WR}$ latches data into the DAC input latch selected by A2–A0 on the rising edge of $\overline{CS}$ .
13	V <sub>CC</sub>	Digital Power Supply. Normally set to +5V. See <i>Power Supplies, Grounding, and Bypassing</i> section for bypass requirements.
14	GND	Ground
15–28	D0–D13	Data Bits 0–13. Offset binary coding.
29	$\overline{CLR}$	Clear Input. Drive $\overline{CLR}$ low to force all DAC outputs to the voltage on their respective DUTGND_ _ . Does not affect the status of internal registers. All DACs return to their previous levels when $\overline{CLR}$ goes high.
30	REFGH+	Positive Reference Input for DACs G and H
31	REFGH-	Negative Reference Input for DACs G and H

# Octal, 14-Bit Voltage-Output DAC with Parallel Interface for ATE

## Pin Description (continued)

PIN	NAME	FUNCTION
32	OUTH	DAC H Buffered Output Voltage
33	DUTGNDGH	Device Sense Ground Input for OUTG and OUTH. In normal operation, OUTG and OUTH are referenced to DUTGNDGH. When CLR is low, OUTG and OUTH are forced to the potential on DUTGNDGH.
34	OUTG	DAC G Buffered Output Voltage
35	OUTF	DAC F Buffered Output Voltage
36	DUTGNDEF	Device Sense Ground Input for OUTE and OUTF. In normal operation, OUTE and OUTF are referenced to DUTGNDEF. When $\overline{\text{CLR}}$ is low, OUTE and OUTF are forced to the potential on DUTGNDEF.
37	OUTE	DAC E Buffered Output Voltage
39	REFCDEF+	Positive Reference Input for DACs C, D, E, and F
40	REFCDEF-	Negative Reference Input for DACs C, D, E, and F
41	OUTD	DAC D Buffered Output Voltage
42	DUTGNDCD	Device Sense Ground Input for OUTC and OUTD. In normal operation, OUTC and OUTD are referenced to DUTGNDCD. When $\overline{\text{CLR}}$ is low, OUTC and OUTD are forced to the potential on DUTGNDCD.
43	OUTC	DAC C Buffered Output Voltage
44	OUTB	DAC B Buffered Output Voltage



# Octal, 14-Bit Voltage-Output DAC with Parallel Interface for ATE

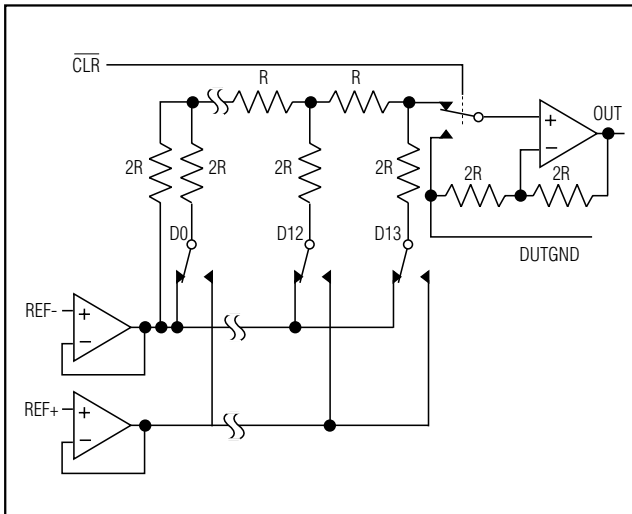


Figure 1. DAC Simplified Circuit

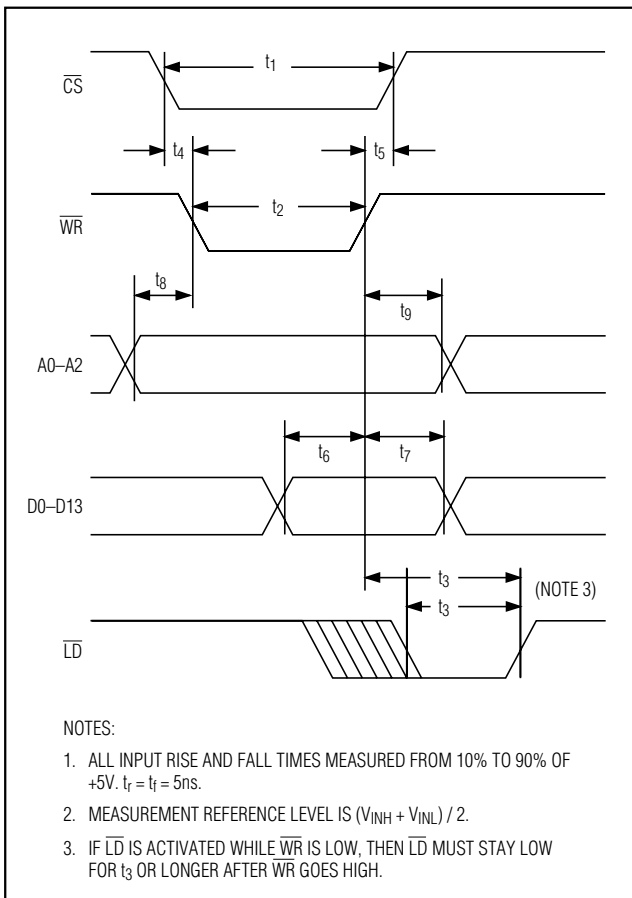


Figure 2. Digital Timing Diagram

## Detailed Description

### Analog Section

The MAX5264 contains eight 14-bit voltage-output DACs. These DACs are “inverted” R-2R ladder networks that convert 14-bit digital inputs into equivalent analog output voltages, in proportion to the applied reference voltages (Figure 1). The MAX5264 has three positive reference inputs (REF\_ \_\_\_+) and three negative reference inputs (REF\_ \_\_\_-). The difference from REF\_ \_\_\_+ to REF\_ \_\_\_-, multiplied by two, sets the DAC output span.

In addition to the differential reference inputs, the MAX5264 has four analog-ground input pins (DUTGND\_ \_). When CLR is high (unasserted), the voltage on DUTGND\_ \_ offsets the DAC output voltage range. If CLR is asserted, the output amplifier is forced to the voltage present on DUTGND\_ \_.

### Reference and DUTGND Inputs

All of the MAX5264’s reference inputs are buffered with precision amplifiers. This allows the flexibility of using resistive dividers to set the reference voltages. Because of the relatively high multiplying bandwidth of the reference input (188kHz), any signal present on the reference pin within this bandwidth is replicated on the DAC output.

The DUTGND pins of the MAX5264 are connected to the negative source resistor (nominally 115kΩ) of the output amplifier. The DUTGND pins are typically connected directly to analog ground. Each of these pins has an input current that varies with the DAC digital code. If the DUTGND pins are driven by external circuitry, budget  $\pm 200\mu\text{A}$  per DAC for load current.

### Output Buffer Amplifiers

The MAX5264’s voltage outputs are internally buffered by precision gain-of-two amplifiers with a typical slew rate of  $1\text{V}/\mu\text{s}$ . With a full-scale transition at its output, the typical settling time to  $\pm 1\text{LSB}$  is  $22\mu\text{s}$ . This settling time does not significantly vary with capacitive loads less than  $10,000\text{pF}$ .

### Output Deglitching Circuit

The MAX5264’s internal connection from the DAC ladder to the output amplifier contains special deglitch circuitry. This glitch/deglitch circuitry is enabled on the falling edge of  $\overline{\text{LD}}$  to remove the glitch from the R-2R DAC. This enables the MAX5264 to exhibit a fraction of the glitch impulse energy of parts without the deglitching circuit.

# Octal, 14-Bit Voltage-Output DAC with Parallel Interface for ATE

## Digital Inputs and Interface Logic

All digital inputs are compatible with both TTL and CMOS logic. The MAX5264 interfaces with microprocessors using a data bus at least 13 bits wide. The interface is double buffered, allowing simultaneous updating of all DACs. There are two latches for each DAC (see *Functional Diagram*): an input latch that receives data from the data bus, and a DAC latch that receives data from the input latch. Address lines A0, A1, and A2 select which DAC's input latch receives data from the data bus as shown in Table 2. Both the input latches and the DAC latches are transparent when  $\overline{CS}$ ,  $\overline{WR}$ , and  $\overline{LD}$  are all low. Any change of D0–D13 during this condition appears at the output instantly. Transfer data from the input latches to the DAC latches by asserting the asynchronous  $\overline{LD}$  signal. Each DAC's analog output reflects the data held in its DAC latch. All control inputs are level triggered. Table 3 is an interface truth table.

**Table 2. MAX5264 DAC Addressing**

A2	A1	A0	FUNCTION
0	0	0	DAC A input latch
0	0	1	DAC B input latch
0	1	0	DAC C input latch
0	1	1	DAC D input latch
1	0	0	DAC E input latch
1	0	1	DAC F input latch
1	1	0	DAC G input latch
1	1	1	DAC H input latch

**Table 3. Interface Truth Table**

$\overline{CLR}$	$\overline{LD}$	$\overline{WR}$	$\overline{CS}$	FUNCTION
X	X	0	0	Input register transparent
X	X	X	1	Input register latched
X	X	1	X	Input register latched
X	0	X	X	DAC register transparent
X	1	X	X	DAC register latched
0	X	X	X	Outputs of DACs at DUTGND_ _
1	1	X	X	Outputs of DACs set to voltage defined by the DAC register, the references, and the corresponding DUTGND_ _

X = Don't care

## Input Write Cycle

Data can be latched or transferred directly to the DAC.  $\overline{CS}$  and  $\overline{WR}$  control the input latch, and  $\overline{LD}$  transfers information from the input latch to the DAC latch. The input latch is transparent when  $\overline{CS}$  and  $\overline{WR}$  are low, and the DAC latch is transparent when  $\overline{LD}$  is low. The address lines (A0, A1, A2) must be valid for the duration that  $\overline{CS}$  and  $\overline{WR}$  are low (Figure 2) to prevent data from being inadvertently written to the wrong DAC. Data is latched within the input latch when either  $\overline{CS}$  or  $\overline{WR}$  is high.

## Loading the DACs

Taking  $\overline{LD}$  high latches data into the DAC latches. If  $\overline{LD}$  is brought low when  $\overline{WR}$  and  $\overline{CS}$  are low, the DAC addressed by A0, A1, and A2 is directly controlled by the data on D0–D13. This allows the maximum digital update rate; however, it is sensitive to any glitches or skew in the input data stream.

## Asynchronous Clear

The MAX5264 has an asynchronous clear pin ( $\overline{CLR}$ ) that, when asserted, sets all DAC outputs to the voltage present on their respective DUTGND pins. Deassert  $\overline{CLR}$  to return the DAC output to its previous voltage. Note that  $\overline{CLR}$  does not clear any of the internal digital registers.

## Applications Information

### Multiplying Operation

The MAX5264 can be used for multiplying applications. Its reference accepts both DC and AC signals. Since the reference inputs are unipolar, multiplying operation is limited to two quadrants. See the graphs in the *Typical Operating Characteristics* for dynamic performance of the DACs and output buffers.

### Digital Code and Analog Output Voltage

The MAX5264 uses offset binary coding. A 14-bit two's complement code is converted to a 14-bit offset binary code by adding  $2^{13} = 8192$ .

### Output Voltage Range

For typical operation, connect DUTGND to signal ground,  $V_{REF+}$  to +4.5V, and  $V_{REF-}$  to -2.0V. Table 4 shows the relationship between digital code and output voltage.

The DAC digital code controls each leg of the 14-bit R-2R ladder. A code of 0x0 connects all legs of the ladder to REF-, corresponding to a DAC output voltage ( $V_{DAC}$ ) equal to REF-. A code of 0x3FFF connects all legs of the ladder to REF+, corresponding to a  $V_{DAC}$  approximately equal to REF+.

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**Table 4. Analog Voltage vs. Digital Code**

INPUT CODE	OUTPUT VOLTAGE (V)
11 1111 1111 1111	+8.999207
10 0000 0000 0000	+2.500
01 0011 1011 0010	+610 $\mu$
00 0000 0000 0001	-3.999207
00 0000 0000 0000	-4.000

**Note:** Output voltage is based on REF+ = +4.5V, REF- = -2.0V, and DUTGND = 0.

The output amplifier multiplies  $V_{DAC}$  by 2, yielding an output voltage range of  $2 \times REF-$  to  $2 \times REF+$  (Figure 1). Further manipulation of the output voltage span is accomplished by offsetting DUTGND. The output voltage of the MAX5264 is described by the following equation:

$$V_{OUT} = 2 \left[ (V_{REF+} - V_{REF-}) \frac{DATA}{2^{14}} + V_{REF-} \right] - V_{OUTGND}$$

where DATA is the numeric value of the DAC's binary input code, and DATA ranges from 0 to 16383 ( $2^{14} - 1$ ). The resolution of the MAX5264, defined as 1LSB, is described by the following equation:

$$LSB = \frac{2(REF+ - REF-)}{2^{14}}$$

### Reference Selection

Because the MAX5264 has precision buffers on its reference inputs, the requirements for interfacing to these inputs are minimal. Select a low-drift, low-noise reference within the recommended REF+ and REF- voltage ranges. The MAX5264 does not require bypass capacitors on its reference inputs. Add capacitors only if the reference voltage source requires them to meet system specifications.

### Minimizing Output Glitch

The MAX5264's internal deglitch circuitry is enabled on the falling edge of  $\overline{LD}$ . Therefore, to achieve optimum performance, drive  $\overline{LD}$  low after the inputs are either latched or steady state. This is best accomplished by having the falling edge of  $\overline{LD}$  occur at least 50ns after the rising edge of  $\overline{CS}$ .

### Power Supplies, Grounding, and Bypassing

For optimum performance, use a multilayer PC board with an unbroken analog ground. For normal operation, connect the four DUTGND pins directly to the ground plane. Avoid sharing the connections of these sensitive pins with other ground traces.

As with any sensitive data-acquisition system, connect the digital and analog ground planes together at a single point, preferably directly underneath the MAX5264. Avoid routing digital signals underneath the MAX5264 to minimize their coupling into the IC.

For normal operation, bypass  $V_{DD}$  and  $V_{SS}$  with 0.1 $\mu$ F ceramic chip capacitors to the analog ground plane. To enhance transient response and capacitive drive capability, add 10 $\mu$ F tantalum capacitors in parallel with the ceramic capacitors. Note, however, that the MAX5264 does not require the additional capacitance for stability. Bypass  $V_{CC}$  with a 0.1 $\mu$ F ceramic chip capacitor to the digital ground plane.

### Power-Supply Sequencing

To guarantee proper operation of the MAX5264, ensure that power is applied to  $V_{DD}$  before  $V_{SS}$  and  $V_{CC}$ . Also ensure that  $V_{SS}$  is never more than 300mV above ground. To prevent this situation, connect a Schottky diode between  $V_{SS}$  and the analog ground plane, as shown in Figure 3. Do not power up the logic input pins before establishing the supply voltages. If this is not possible and the digital lines can drive more than 10mA, place current-limiting resistors (e.g., 470 $\Omega$ ) in series with the logic pins.

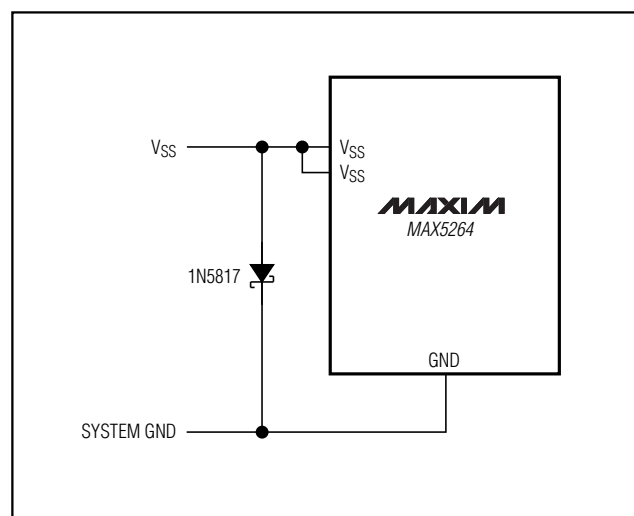


Figure 3. Schottky Diode Between  $V_{SS}$  and GND

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## ***Driving Capacitive Loads***

The MAX5264 typically drives capacitive loads up to 0.01 $\mu$ F without a series output resistor. However, whenever driving high capacitive loads, it is prudent to use a 220 $\Omega$  series resistor between the MAX5264 output and the capacitive load.

## ***Chip Information***

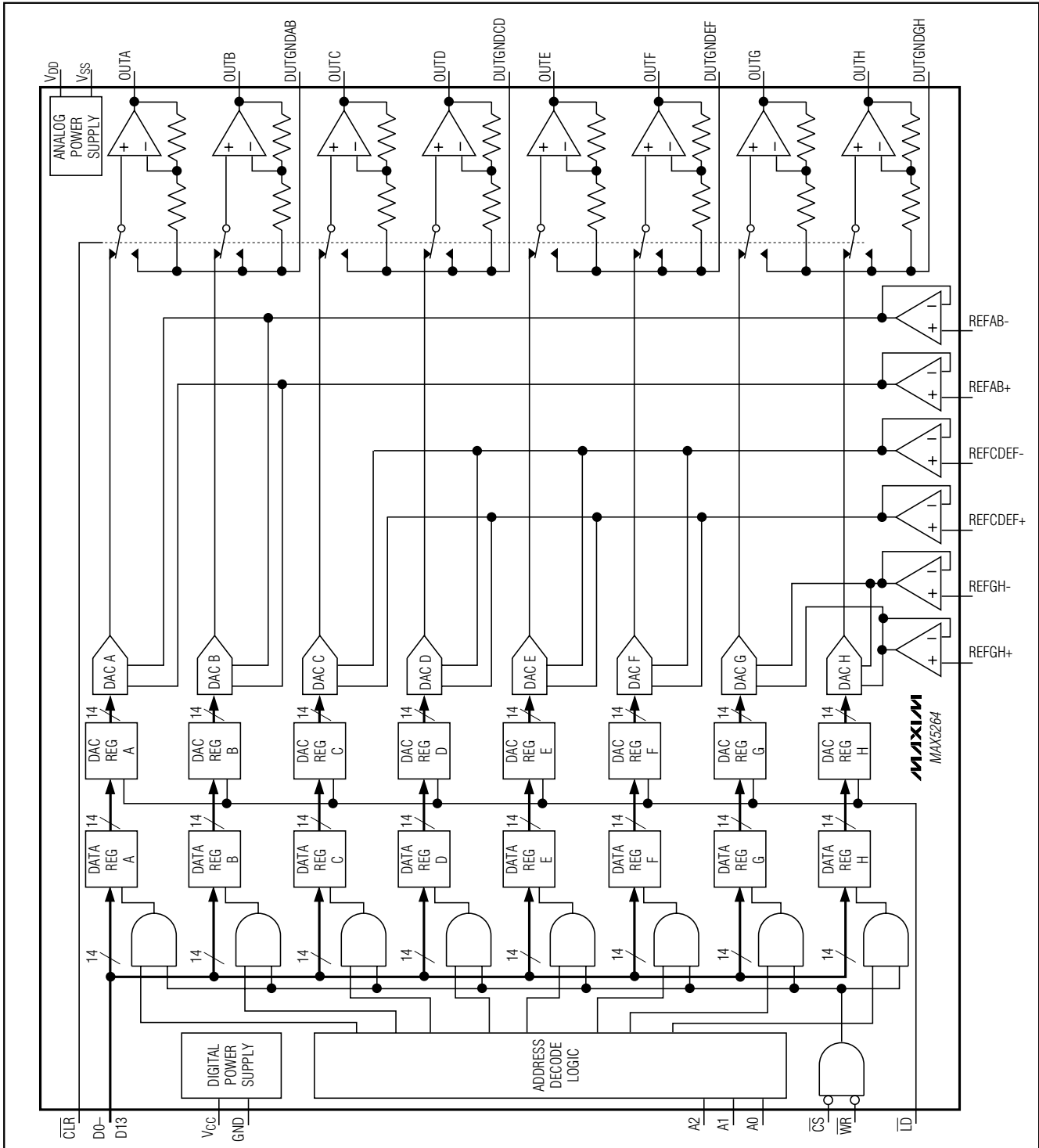
TRANSISTOR COUNT: 13,225

PROCESS: BiCMOS

# Octal, 14-Bit Voltage-Output DAC with Parallel Interface for ATE

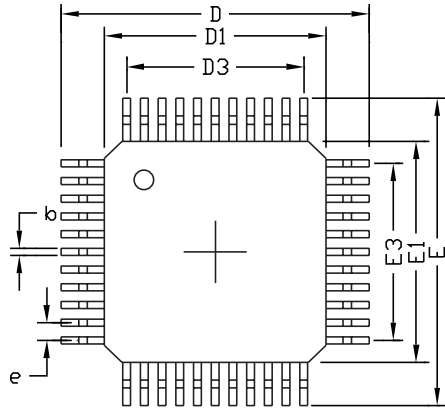
## Functional Diagram

**MAX5264**

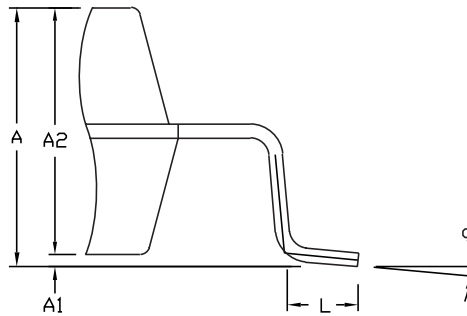
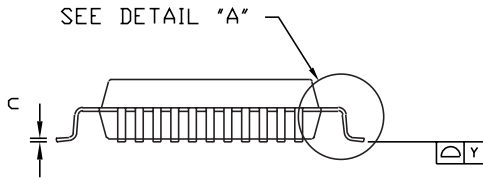


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## Package Information



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.032	2.388	0.080	0.094
A1	0.102	0.254	0.004	0.010
A2	1.930	2.134	0.076	0.084
b	0.305	0.457	0.012	0.018
c	0.102	0.254	0.004	0.010
D	12.954	13.462	0.510	0.530
D1	9.906	10.109	0.390	0.398
D3	8.000	REF	0.315	REF
E	12.954	13.462	0.510	0.530
E1	9.906	10.109	0.390	0.398
E3	8.000	REF	0.315	REF
e	0.800	REF	0.0315	REF
L	0.635	0.940	0.025	0.037
α	*0	*10	*0	*10



NOTES:

1. D1&E1 DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-108-AA-2.

DETAIL "A"

<b>MAXIM</b>		
<small>PROPRIETARY INFORMATION</small>		
<small>TITLE:</small>		
PACKAGE OUTLINE, MQFP, 44L		
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small>	<small>REV</small>
	21-0826	C 1/1

MQFP44.EPS

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with Parallel Interface for ATE**

NOTES

**MAX5264**

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## **NOTES**

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