MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

# MC1445
# MC1545

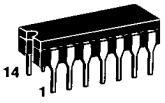
# Gate Controlled Two Channel Input Wideband Amplifier

The MC1445/1545 was designed for use as a general purpose gated wideband amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier.

- Large Bandwidth; 50 MHz Typical
- Channel Select Time of 20 ns Typical
- Differential Inputs and Differential Output

**GATE CONTROLLED TWO CHANNEL INPUT WIDEBAND AMPLIFIER**

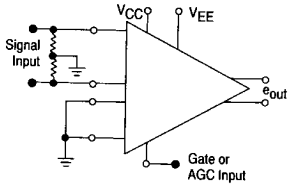
**SILICON MONOLITHIC INTEGRATED CIRCUIT**



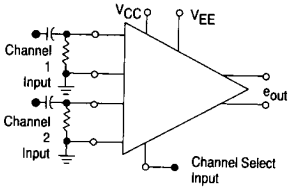

**L SUFFIX**
CERAMIC PACKAGE
CASE 632

## Typical Applications

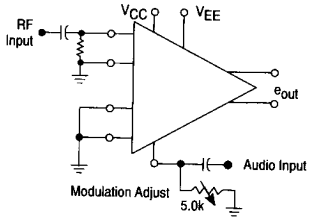
**Video Switch or Differential Amplifier with AGC**



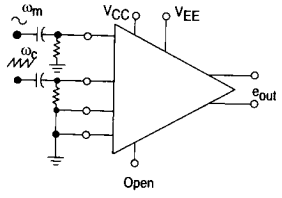

**Multiplex or FSK**



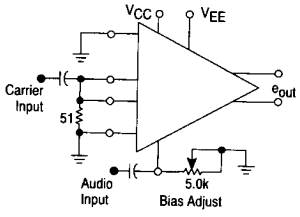

**Amplitude Modulator**



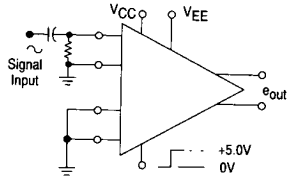

**Pulse Width Modulator**



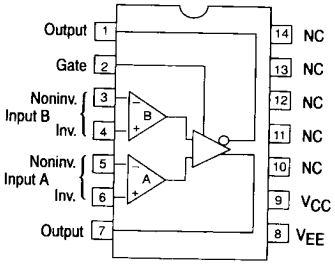

**Balanced Modulator**




**Analog Switch**




## PIN CONNECTIONS




(Top View)

## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| LM1445L | 0° to +75°C | Ceramic DIP |
| LM1545L | −55° to +125°C | Ceramic DIP |

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**MAXIMUM RATINGS** ($T_A$ = +25°C, unless otherwise noted.)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Supply Voltage | | $V_{CC}$<br>$V_{EE}$ | +12<br>−12 | Vdc |
| Input Differential Voltage Range | | $V_{IDR}$ | ±5.0 | V |
| Load Current | | $I_L$ | 25 | mA |
| Power Dissipation (Package Limitation)<br>Ceramic Dual In-Line Package<br>Derate above $T_A$ = +25°C | | $P_D$ | <br>625<br>5.0 | <br>mW<br>mW/°C |
| Operating Ambient Temperature Range | MC1445<br>MC1545 | $T_A$ | 0 to +75<br>−55 to +125 | °C |
| Storage Temperature Range | | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = −5.0 Vdc, @ $T_A$ = +25°C, specifications apply to both input channels, unless otherwise noted.)

| Characteristics | Fig. No. | Symbol | MC1545 Min | MC1545 Typ | MC1545 Max | MC1445 Min | MC1445 Typ | MC1445 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Single-Ended Voltage Gain | 1, 12 | $A_{VS}$ | 16 | 19 | 21 | 16 | 19.5 | 23 | dB |
| Bandwidth | 1, 12 | BW | 40 | 50 | — | — | 50 | — | MHz |
| Input Impedance (f = 50 kHz) | 5, 14 | $z_i$ | 4.0 | 10 | — | 3.0 | 10 | — | kΩ |
| Output Impedance (f = 50 kHz) | 6, 15 | $z_o$ | — | 25 | — | — | 25 | — | Ω |
| Output Differential Voltage Range ($R_L$ = 1.0 kΩ, f = 50 kHz) | 4, 13 | $V_{ODR}$ | 1.5 | 2.5 | — | 1.5 | 2.5 | — | $V_{p-p}$ |
| Input Bias Current | 16 | $I_{IB}$ | — | 15 | 25 | — | 15 | 30 | μAdc |
| Input Offset Current | 16 | $I_{IO}$ | — | 2.0 | — | — | 2.0 | — | μAdc |
| Input Offset Voltage | 17 | $V_{IO}$ | — | 1.0 | 5.0 | — | — | 7.5 | mVdc |
| Quiescent Output dc Level | 17 | $V_O$ | — | 0.1 | — | — | 0.1 | — | Vdc |
| Output dc Level Change (Gate Input Voltage Change: +5.0 V to 0 V) | 17 | $\Delta V_O$ | — | ±15 | — | — | ±15 | — | mV |
| Common Mode Rejection (f = 50 kHz) | 9, 18 | CMR | — | 85 | — | — | 85 | — | dB |
| Input Common Mode Voltage Range | 18 | $V_{ICR}$ | — | ±2.5 | — | — | ±2.5 | — | $V_{pk}$ |
| Gate Characteristics<br>Gate Input Voltage – Low Logic State (Note 1)<br>Gate Input Voltage – High Logic State (Note 2) | 8 | <br>$V_{IL(G)}$<br>$V_{IH(G)}$ | <br>0.40<br>— | <br>0.70<br>1.5 | <br>—<br>2.2 | <br>0.2<br>— | <br>0.4<br>1.3 | <br>—<br>3.0 | Vdc |
| Gate Input Current – Low Logic State ($V_{IL(G)}$ = 0 V) | 18 | $I_{IL(G)}$ | — | — | 2.5 | — | — | 4.0 | mA |
| Gate Input Current – High Logic State ($V_{IH(G)}$ = +5.0 V) | 18 | $I_{IH(G)}$ | — | — | 2.0 | — | — | 4.0 | μA |
| Step Response ($e_{in}$ = 20 mV) | 19 | $t_{PLH}$<br>$t_{PHL}$<br>$t_{TLH}$<br>$t_{THL}$ | —<br>—<br>—<br>— | 6.5<br>6.3<br>6.5<br>7.0 | 10<br>10<br>15<br>15 | —<br>—<br>—<br>— | 6.5<br>6.3<br>6.5<br>7.0 | —<br>—<br>—<br>— | ns |
| Wideband Input Noise (5.0 Hz – 10 MHz, $R_S$ = 50 Ω) | 10, 20 | $e_n$ | — | 25 | — | — | 25 | — | μV(rms) |
| DC Power Consumption | 11, 20 | $P_C$ | — | 70 | 110 | — | 70 | 150 | mW |

**NOTES:** 1. $V_{IL(G)}$ is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
2. $V_{IH(G)}$ is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

**Figure 1. Single-Ended Voltage Gain versus Frequency**

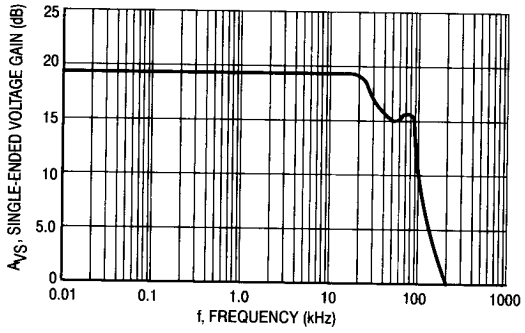


**Figure 2. Single-Ended Voltage Gain versus Temperature**

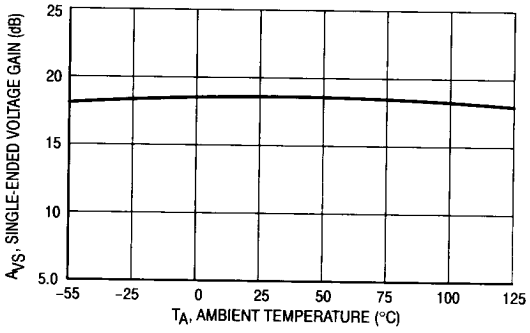


**Figure 3. Voltage Gain versus Power Supply Voltages**

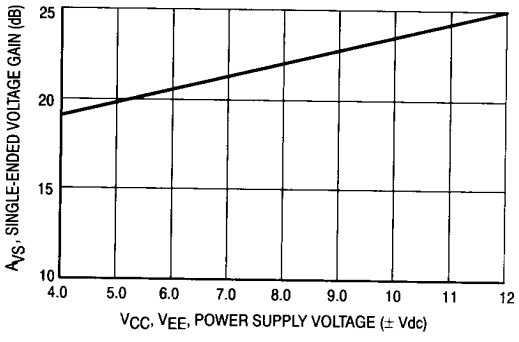


**Figure 4. Output Voltage Swing versus Load Resistance**

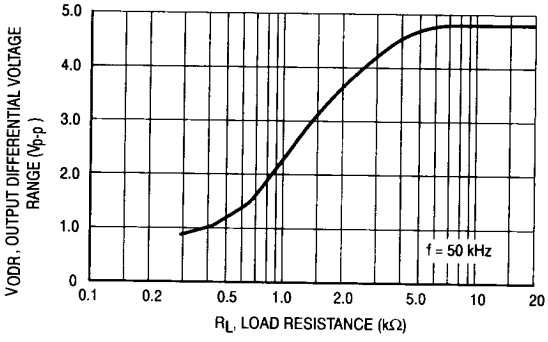


**Figure 5. Input Cp and Rp versus Frequency (Both Channels)**

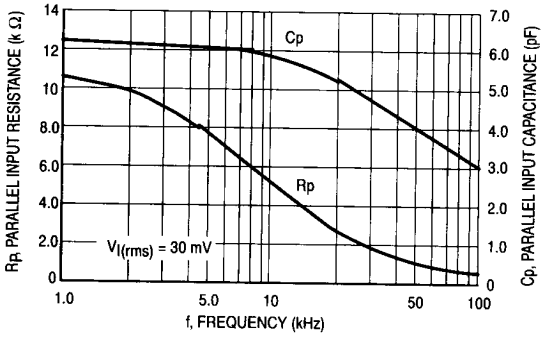


**Figure 6. Output Impedance versus Frequency**

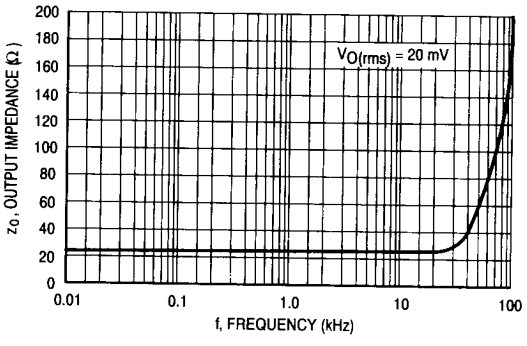

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**Figure 7. Channel Separation versus Frequency**

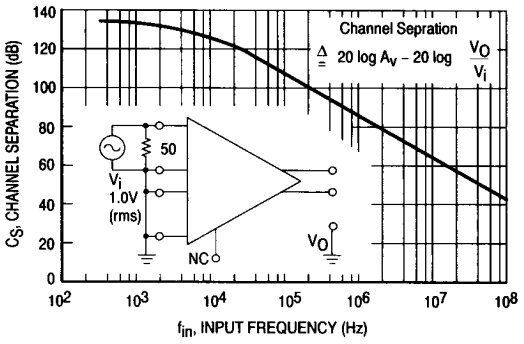


**Figure 8. Gate Characteristics**

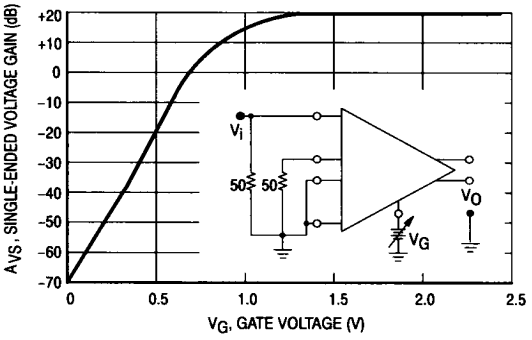


**Figure 9. Common Mode Rejection Ratio versus Frequency**

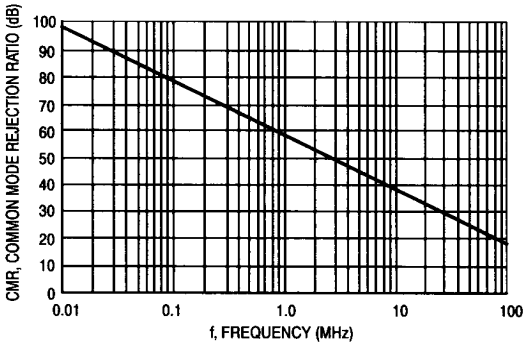


**Figure 10. Input Wideband Noise versus Source Resistance**

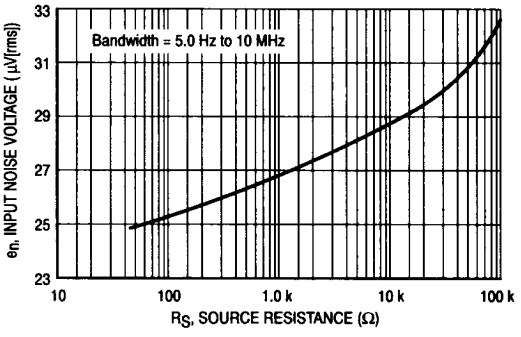


**Figure 11. Circuit Schematic**

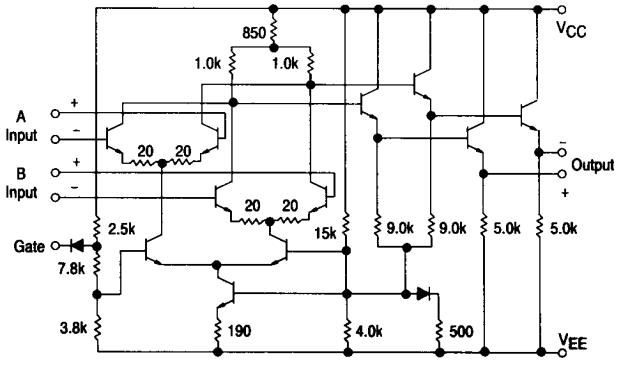


**Figure 12. Single-Ended Voltage Gain and Bandwidth Test Circuit**

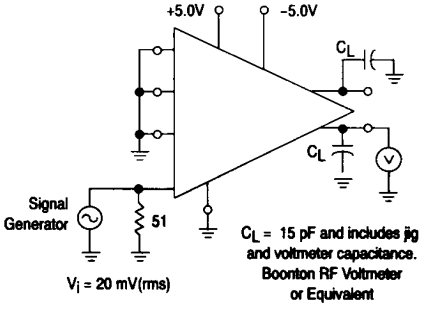

**Figure 13. Output Voltage Swing Test Circuit**

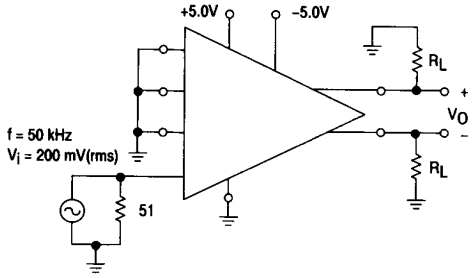


**Figure 14. Input Impedance Test Circuit**

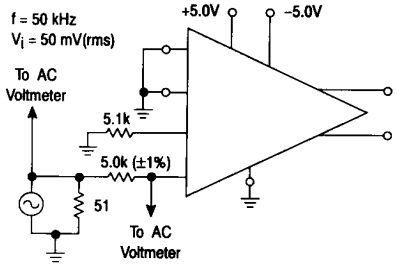


**Figure 15. Output Impedance Test Circuit**

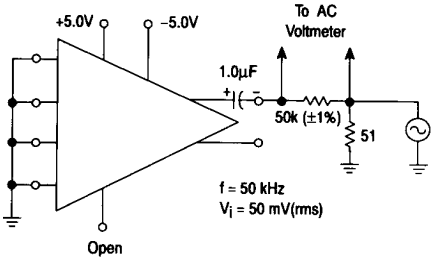


**Figure 16. Input Bias Current and Input Offset Current Test Circuit**

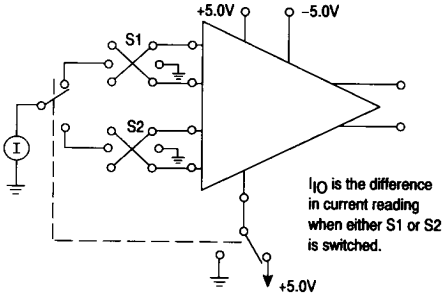


**Figure 17. Input Offset Voltage and Quiescent Output Level Test Circuit**

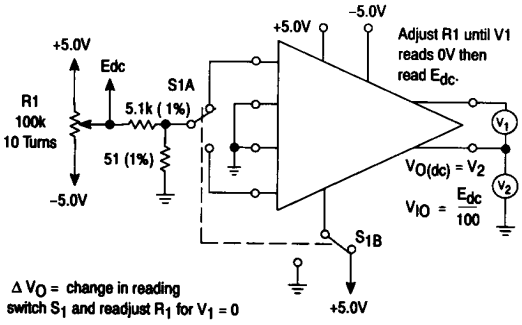


**Figure 18. Gate Current (High and Low), Common Mode Rejection and Common Mode Input Range Test Circuit**

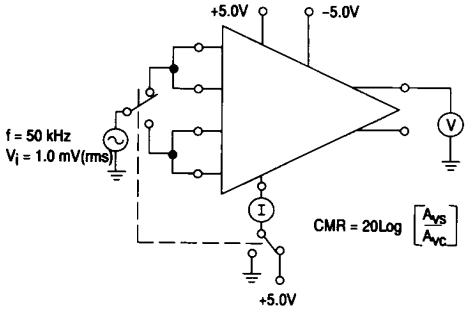

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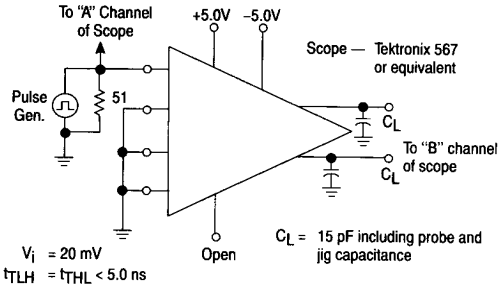
**Figure 19. Propagation Delay, Rise and Fall Times Test Circuit**



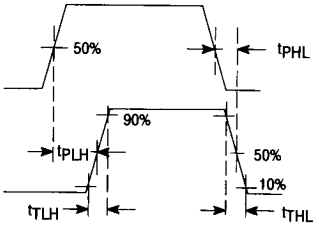




**Figure 20. Power Dissipation and Wideband Input Noise Test Circuit**

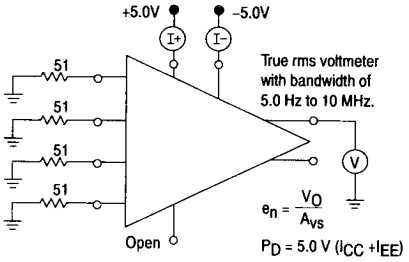



**Figure 21. Limiting Characteristic**