

Nexperia PNX1500

Connected media processor

Exceptional performance, high integration, and support for a broad range of media formats make the Philips Nexperia PNX1500 the media processor of choice for powering the next generation of connected, multimedia consumer devices.



Key features

- Connected media processor for streaming multimedia applications: audio, video, graphics, and communications
- Innovative 32-bit TriMedia™ CPU with powerful multimedia and floating point instructions
- On-chip, independent, DMA-driven I/O and coprocessing units
- Video output up to W-XGA TFT LCD (1280 x 768 60 Hz) and up to HD video (1920 x 1080 60i)
- Image scaling and advanced de-interlacing unit
- 2D engine accelerates complex graphics for real-time overlay
- Full DVD playback
- Supports up to 256-MB DDR SDRAM memory system using 16- or 32-bit wide data at rates up to 400 MHz (1.6 GB/s)
- Comprehensive software development tools and application software enable application development entirely in C/C++
- Support for Philips V2F dynamic power management enables frequency and power consumption to be tailored per application

Semiconductors

Building on a tradition of high-performance, low-cost, real-time media processors, the Nexperia PNX1500 handles more formats of video, audio, graphics, and communications datastreams than previous Nexperia media processors. It includes a completely redesigned TriMedia CPU core and offers compatibility with all leading video standards, including MPEG-2, MPEG-4, DV, RealNetworks®, and DivX-5. The PNX1500 also integrates a TFT LCD controller and an Ethernet 10/100 MAC, reducing external components and supporting advanced product configurations.

Real-time multimedia processing, extensive connectivity options, and support for dynamic power management make PNX1500 an ideal single-chip solution for an increasing variety of standalone and networked multimedia products—from personal video recorders, to connected DVD players, wireless LAN devices, IP set-top boxes, advanced home gateways, smart display pads, videoconferencing devices, and more. It handles popular multimedia algorithms and standard communication protocols in real time, including encode/decode of MPEG-2 or MPEG-4 (SP, MVP), MPEG-4 ASP decode, DV decode, H.263 encode/decode, DivX-5 decode, MP3 encode/decode, AAC encode/decode, TCP/IP, Ethernet, and Universal PnP.

The PNX1500 is supported by a comprehensive software development environment enabling application development entirely in the C and C++ programming languages. Extensive applications libraries, developed by Philips and third parties, improve time-to-market, reduce design cycles, and lower product development costs.

PHILIPS

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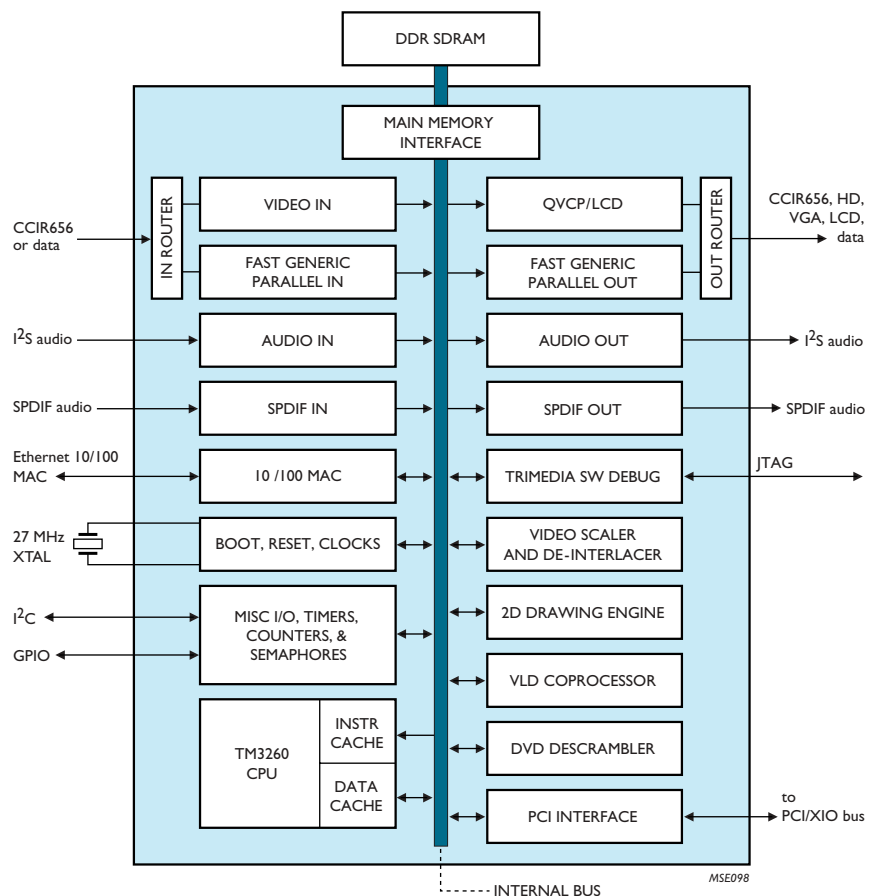
Architectural overview

The PNXI500 leverages a powerful, completely redesigned C/C++ programmable TriMedia TM3260 CPU for improved media processing. It runs a small real-time operating system enabling efficient and predictable response to real-time events. Independent, on-chip, bus-mastering DMA units capture and format datastream I/O and accelerate processing of multimedia algorithms. A sophisticated memory hierarchy manages internal I/O and streamlines access to external memory. The result—a low-cost, programmable media processor proven in standalone and hosted multimedia products.

C/C++-programmable VLIW CPU

The PNXI500 CPU core delivers top performance through an elegant implementation of a fine-grain parallel very-long instruction word (VLIW) architecture. Five issue slots enable up to five simultaneous RISC-like operations to be scheduled into only one VLIW instruction. These operations can simultaneously target any five of the CPU's 31 pipelined functional units within one clock cycle.

On a single chip, the Nexperia PNXI500 accelerates processing of audio, video, graphics, control, and communications datastreams.



In addition to a full complement of traditional 32-bit integer and IEEE-754 compliant floating-point microprocessor operations, the TriMedia TM3260 instruction set includes an extensive set of multimedia operations and single instruction multiple data (SIMD)-style 'special' operations (ops) for dual 16-bit or quad 8-bit packed data. By combining multiple simple operations, a single special op can implement up to 12 traditional microprocessor operations. In this way, up to 40 traditional operations can be executed in a single VLIW instruction. When incorporated into application source code, special ops dramatically improve performance and increase the efficiency of the PNX1500 CPU's parallel architecture.

On-chip I/O and coprocessing units

Video input processor (VIP)

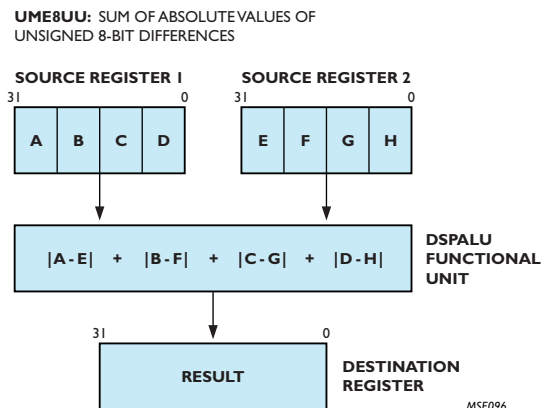
The VIP unit captures and processes digital video for use by on-chip units. It accepts up to 10-bit parallel YUV 4:2:2 digital video from any device or component outputting a CCIR656-compliant stream or a YUV stream with separate H and V syncs. During capture of a continuous video stream, the VIP unit can crop, horizontally downscale, or convert the YUV video to one of many standard pixel formats as needed before writing data to memory. When streaming video from TV broadcasts, it can also capture raw VBI data into a separate window in memory. This unit shares its pin interface with a fast generic parallel input unit through an input router.

Fast generic parallel input (FGPI)

The FGPI unit captures unstructured, infinite parallel datastreams, messages, or control signals—any datastream with no YUV processing requirements. When raw mode is enabled, an 8-, 16-, or 32-bit parallel datastream is captured continuously and double buffered into memory. For example, the FGPI unit can receive an ATSC transport stream from an external channel decoder.

Video scaler and de-interlacing

A versatile, programmable memory-based scaler unit applies a wide variety of image size, color, and format manipulations to improve video quality and prepare it for display. This unit handles de-interlacing (with optional edge detection/correction), horizontal and vertical scaling, linear and non-linear aspect ratio conversion, anti-flicker filtering, pixel format conversions, and more.



The PNX1500 CPU's special 'ops' dramatically improve performance and increase the efficiency of its parallel architecture. The ume8uu operation, commonly used for motion estimation in video compression, implements 11 simple operations in one TriMedia special op.

Quality video composition processor (QVCP)

The QVCP unit composites two planes of display data from different sources before output. It supports either two video planes or one video plane and one graphics plane, such as video from DVD playback and graphics from a web browser. Working together with the on-chip 2D engine and the memory-based scaler, QVCP enables the PNX1500 to support many types of multimedia applications at high speeds with few external components.

In addition to two-layer video compositing, the QVCP integrates scaling, an TFT LCD controller and a long list of video quality enhancements including de-indexing or gamma equalization, contrast and brightness control, luminance sharpening, horizontal dynamic peaking, skin tone correction, dithering, and generation of screen timing required by the target display.

QVCP outputs the resulting video datastream to any of a wide variety of off-chip video subsystems supporting CCIR656, YUV, or RGB formats, progressive or interlaced scan modes, and resolutions up to W-XGA TFT LCD (1280 x 768 60 Hz) or SD/HD video (up to 1920 x 1080 60I). The QVCP unit shares its pin interface with a fast generic parallel output unit through an output data router.

Fast generic parallel output (FPGO)

The FPGO unit can output any raw datastream with no video post processing requirements, for example, an ATSC bitstream. It can also broadcast unidirectional messages to other PNX1500 processors.

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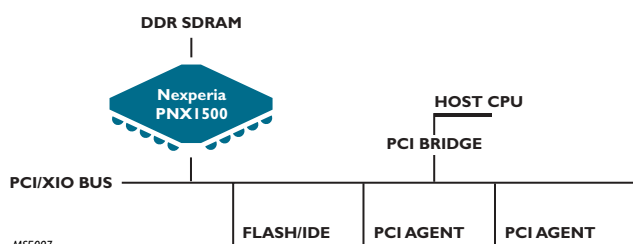
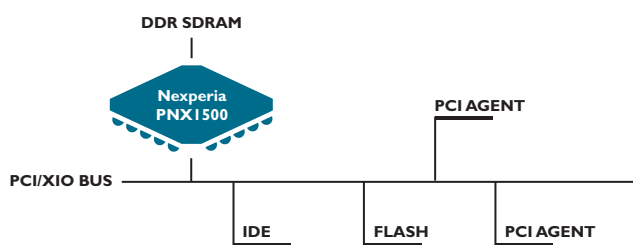


Audio input (AI) and audio output (AO)

Highly programmable AI and AO units provide all signals needed to read and write digital audio datastreams from/to most high-quality, low-cost serial audio oversampling A/D and D/A converters and codecs. Both units connect to off-chip stereo converters through flexible bit-serial I²S interfaces. Their high level of programmability provides tremendous flexibility in handling custom datastreams, adapting to custom protocols, and upgrading to future audio standards.

The AI unit supports capture of up to eight channels of stereo audio. In raw mode, it captures any quantity of bits from the programmable frame. The AO unit outputs up to eight channels and directly drives up to four external stereo I²S or similar D/A converters or highly integrated PC codecs. Software support for decode and output of Dolby Pro Logic[®] and DTS is provided through optional application library modules.

The PNX1500 is designed for use as the main processor in standalone systems and as a coprocessor in a hosted or multiprocessor environment.



MSE097

SPDIF input and output

An SPDIF (Sony/Philips Digital Interface) input unit connects to external sources of digital audio, such as a DVD player, to receive audio datastreams a variety of formats, including stereo PCM data, 5.1-channel Dolby Digital[®] data (per IEC-1937), and more. An SPDIF output unit outputs a high-speed serial datastream. Primarily used to transmit digital SPDIF-formatted audio data to external audio equipment, it can also be used to output two-channel linear PCM audio from an internal audio mix or captured, compressed multi-channel audio streams such as Dolby Digital, DTS, or AAC (per Project 1937). Software-decoded audio can be mixed with other audio before output.

Both SPDIF input and output units have independent, programmable sample rates ensuring perfect synchronization to any time reference in the system. Datastream content is software generated and software controlled.

2D drawing engine (2D DE)

An on-chip 2D rendering and DMA engine accelerates high-speed 2D graphics operations including solid fills, lines, three-operand bitblts, and color expansion of monochrome data to any supported pixel format. A full 256-level alpha bitblt blends source and destination images together.

Variable length decoder (VLD)

A VLD coprocessor offloads the CPU during decoding or transcoding of Huffman-encoded MPEG-2 and MPEG-1 datastreams. It outputs a decoded stream to memory that is optimized for MPEG decompression software.

DVD descrambler

An on-chip DVD descrambler unit handles DVD authentication and descrambling tasks, enabling PNX1500 to integrate complete DVD datastream playback. An IDE DVD drive can be attached directly to the PNX1500 PCI/XIO interface.

Memory system

The PNX1500 couples main memory to substantial on-chip caches through a glueless main memory interface and internal bus system.

Glueless main memory interface (MMI)

The MMI acts as the main memory controller and programmable central arbiter, allocating memory bandwidth for on-chip unit activities. MMI provides a 16- or 32-bit DDR SDRAM interface. The 32-bit interface is equivalent to a 64-bit SDR SDRAM interface running at 200 MHz, resulting in theoretical maximum bandwidth of up to 1.6 GB/s. Programmable memory timing parameters enable the MMI memory controller to support most DDR SDRAM devices. Memory clock speed is programmable and independent of the PNX1500 CPU clock, eliminating the top-speed limitations of fixed memory/CPU clock ratios. Flexible memory configurations support memory footprints from 8 to 256 MB, enabling a wide variety of PNX1500-based systems to be built.

Dedicated instruction and data cache

The PNX1500 CPU is supported by separate, dedicated on-chip data and instruction caches employing a variety of techniques to improve cache hit ratios and CPU performance. The 16-KB eight-way, set-associative data cache supports dual accesses per cycle. It is non-blocking thus cache misses and CPU cache accesses can be handled simultaneously. Early restart techniques reduce read-miss latency. Background copyback reduces CPU stalls.

A 64 KB 8-way set-associative instruction cache provides 224 bits of instructions every clock cycle. To reduce internal bus bandwidth requirements, instructions in main memory and cache use a compressed format.

High-speed internal bus

The PNX1500 CPU and processing units access external memory through an internal bus system comprising separate 64-bit data and 32-bit address buses. Arbitrated by the MMI unit, the internal buses maintain real-time responsiveness in a variety of applications.

Control and connectivity

The PNX1500's versatile interfaces and control options support many advanced product configurations.

I²C interface

The PNX1500's I²C master/slave external interface operates in both standard (100 kHz) and fast (400 kHz) modes. It can connect to an optional EEPROM for boot and can be used to control a variety of different I²C board-level devices.

I/O Ethernet MAC

The PNX1500 incorporates an Ethernet MAC sublayer of the IEEE 802.3 standard, enabling an external PHY chip to be attached through a standard media independent interface (MII) or reduced MII interface (RMII). It implements dual-transmit descriptor buffers, supporting both real-time and non-real-time traffic. Quality of Service (QoS) is ensured through low- and high-priority transmit queues.

Timers

The PNX1500 provides four 32-bit general purpose timers for performance analysis, real-time interrupt generation and/or system event counting.

PCI/XIO bus interface

A PCI/XIO interface connects the CPU and on-chip units to a variety of board-level memory components and off-chip devices. It allows simultaneous connection of 32-bit PCI master/slave devices as well as separate address/data-style 8- and 16-bit microprocessor slave peripherals, standard (NOR) or disk-type (NAND) Flash memories, or an IDE disk interface.

TriMedia software debug (TMDBG) unit/JTAG port

Remote debugging of software running on the CPU core can be performed using the TriMedia interactive source debugger. The PNX1500 JTAG port connects a PC (running the debugger) to the TMDBG unit, enabling full support for interactive debugging features. The JTAG port is also used for boundary scan.

General purpose I/O (GPIO) and flexible serial interface

The PNX1500 supports 16 dedicated GPIO I/O pins for software I/O, external interrupt input, universal Remote Control Blaster transmission, and signal sampling and pattern generation for emulating high-speed serial protocols.

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IR remote control receive and transmit

The PNX1500 uses the GPIO pin event sequence timestamping mechanism and software event interpretation to execute remote control (RC) commands. This approach supports a wide variety of RC protocols including Philips RC-5, RC-6, and RC-MM.

Dynamic power management

Philips V²F power management enables devices to conserve power by tailoring frequency and core voltage to application requirements. When PNX1500 is configured with an external, programmable core voltage regulator, its software-programmable clocks enable the CPU to run at lower speeds, reducing power consumption during less cycle-consuming tasks. For example, decoding an MP3 audio stream requires less than 30 MHz of CPU cycles. Power is conserved by adjusting the clock speed and the external voltage to service this lower cycle requirement.

Robust software development environment

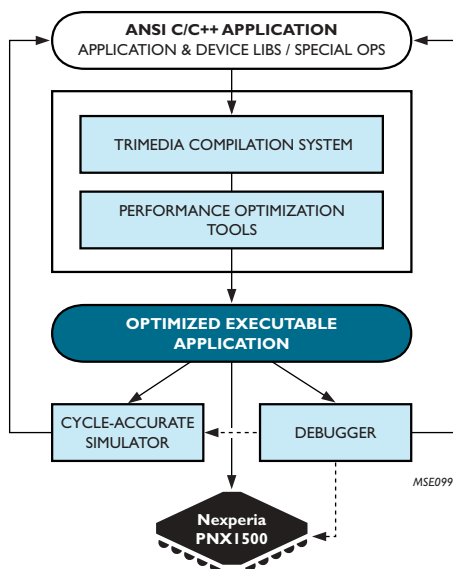
The PNX1500 is supported by a full suite of system software tools to compile and debug code, analyze and optimize performance, and simulate execution of its TriMedia CPU core. This comprehensive software development environment dramatically lowers development costs and reduces time-to-market by enabling development of multi-media applications entirely in the C and C++ programming languages.

Nexperia PNX1500 processors preserve investments in software development through compatibility between PNX1500 family members at the source code level. Powerful, optimizing compilers ensure that programmers never need to resort to non-portable assembler programming. As evolutionary hardware and software enhancements are incorporated into newer PNX processors, increased performance is often achieved by simply recompiling application software.

TriMedia application libraries

Many application libraries are available from Philips and third-party suppliers. These C-callable routines are optimized for top performance on the TriMedia CPU and include modules for functions such as:

- MPEG-1 encode/decode
- MPEG-2 encode/decode
- MPEG-4 (SP, MVP) encode/decode, MPEG-4 ASP decode
- DV decode
- DivX-5 decode
- H.32x encode/decode
- H.263 encode/decode
- Dolby Pro Logic or Dolby Digital (AC-3) decode
- MP3 encode/decode
- AAC encode/decode
- TCP/IP, Ethernet, Universal PnP protocols
- and more.



Unique to the TriMedia core's VLIW implementation, parallelism is optimized at compile time by an innovative compilation system.

Technical specifications

PHYSICAL

Process	0.13- μ m CMOS
Package	456 BGA
Power	<i>supply</i> core 1.2 V, DDR 2.5 V, I/O 3.3 V (5 V tolerant) <i>consumption</i> 1.5 W typical at 266 MHz
Case temperature	0 to 85°C

CENTRAL PROCESSING UNIT

Type	TriMedia TM3260
Clock speed	266 MHz, 300 MHz
Issue slots	5
Address space	32-bit, linear
Instruction set	Arithmetic and logical, load/store, special multimedia and DSP, IEEE-754 compliant floating point
Data types	Boolean, 8-, 16- and 32-bit signed and unsigned integer, 32-bit IEEE floats
Functional units	31 pipelined: integer and floating-point arithmetic units, data-parallel DSP-like units
Registers	128 fully general purpose, 32 bits wide, non-banked
Interrupts	64 auto-vectoring, with 8 programmable priority levels
Byte order	Big or little endian

CACHES

Access	<i>data</i> 8-, 16-, or 32-bit words <i>instruction</i> 64 bytes
Associativity	8-way set-associative with hierarchical LRU replacement
Block size	64 bytes
Size	<i>data</i> 16 KB <i>instruction</i> 64 KB

VIDEO INPUT PROCESSOR UNIT (VIP)

External interface	38 pins: 32 data, 2 clock, and 2 validity signals
Formats	CCIR 601/656: 10-bit video (up to 40.5 Mpix/sec); HD video (using 20-bit YUV input mode)
Clock rate	Up to 81 MHz pixel clock
Functions	Programmable on-the-fly horizontal scaling
VBI formats	Closed Captioning, Teletext, NABST, CGMS, and WSS

FAST GENERIC PARALLEL INPUT UNIT (FGPI)

Data rate	Up to 100 MHz for 8-, 16- or 32-bit parallel data and messages, aggregate input bandwidth up to 400 MB/s
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VIDEO SCALER & DE-INTERLACER UNIT (MBS)

Scaling	Simultaneous vertical and horizontal scaling with linear and non-linear aspect-ratio conversion
De-interlacing	Simple median, majority-selection (i.e. selects best case out of 3 different algorithms), simple field insertion and line doubling, or high-end, Philips edge-dependent de-interlacing (EDDI) algorithm
Filtering	Programmable up to 6-tap polyphase filters
Color/Formats	Variable color space conversion; conversions between 4:2:0, 4:2:2 and 4:4:4; color-key and alpha processing
Performance	Up to 120 Mpix/s

VIDEO OUTPUT UNIT (QVCP)

Data formats	24- or 30-bit full parallel RGB or YUV, 16- or 20-bit Y and U/V multiplexed data, 8- or 10-bit 656 (full D1, 4:2:2 YUV), 8- or 10-bit 4:4:4 format in 656-style with RGB or YUV
Resolutions	TFT LCD W-XGA (1280 x 768) at 60 Hz, SD/HD video up to 1920 x 1080 60I
Clock rates	Up to 81 MHz
Functions	2-layer compositing, picture quality improvements, gamma correction, horizontal 10-tap scaling, genlock mode

FAST GENERIC PARALLEL OUTPUT (FGPO)

Data rate	Up to 100 MHz for 8-, 16- or 32-bit parallel data and messages, aggregate output bandwidth up to 400 MB/s
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AUDIO INPUT & OUTPUT UNITS (AI & AO)

Sample size	8 channels, 16- or 32-bit samples per channel
Sample rates	Programmable with 0.001 Hz resolution; maximum sample rate is application dependent
Data formats	16-bit (mono and stereo), 32-bit (mono and stereo), PC standard memory data format
Clock source	Internal or external
Native protocol	I ² S over serial 6-wire protocols

SPDIF INPUT & OUTPUT UNITS (SPDI & SPDO)

Sample size	6 channels, 16 or 24 bits per channel
Bit rate	Up to 40 Mbits/s in raw mode
Native protocol	IEC-958, 1 wire

2D DRAWING ENGINE

Functions	Solid fills, 3-operand bitblt, lines, monochrome data expansion, 256-level alpha bitblt (to blend 2 images), anti-aliased lines and fonts
Formats	8-, 16-, and 32-bit/pixel

VARIABLE LENGTH DECODER UNIT (VLD)

Functions	Parses MPEG-1 and MPEG-2 elementary bitstreams generating run-level pairs and filling macroblock headers
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Technical specifications (continued)

DVD DESCRAMBLER UNIT (DVDD)

Functions Authentication, descrambling

I²C INTERFACE

Modes Master and slave

Addressing Up to 10-bit

Operating modes *standard* 100 kHz
fast 400 kHz

ETHERNET MAC

Interface 10/100 IEEE 802.3, MII, and RMII

Functions Real-time traffic, QoS

PCI/XIO BUS INTERFACE

Width 32-bit data, 32-bit address space

Speed 33-MHz PCI 2.2 interface with integrated PCI bus arbiter up to 4 masters

Voltage 3.3 V (5 V tolerant)

Functions PCI master and slave
8-, and 16-bit NAND or NOR Flash memories
IDE controller

MEMORY SYSTEM

Speed Up to 200 MHz (1.6 GB/s)

Memory size 8 to 256 MB

Supported types 64 to 512 Mbit DDR SDRAM devices

Width 16- or 32-bit bus

Signal levels 2.5 V SSTL-II

TIMERS

Number 4

Sources (prescaled) CPU clock, data or instruction breakpoints, cache events, video I/O clocks, audio in/out word strobe

GPIO

Dedicated pins 16

Functions Software I/O, external interrupt, universal RC blaster, clock source/gate for system event timers/counters, emulating high-speed serial protocols

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