



PRELIMINARY SPECIFICATION

BIPOLAR ANALOG INTEGRATED CIRCUIT  
 $\mu$ PC1401C

NTSC CHROMINANCE, LUMINANCE, SYNCHRONIZATION,  
 AND DEFLECTION CIRCUIT  
 (CRYSTAL OSCILLATOR TYPE)

$\mu$ PC1401C is a bipolar analog integrated circuit designed for NTSC color TV.

It contains video signal processing circuit, chroma signal demodulation circuit, synchronous signal separator, deflection signal – horizontal and vertical – generator and the peripheral circuits in a plastic molded 42 pins dual in-line package.

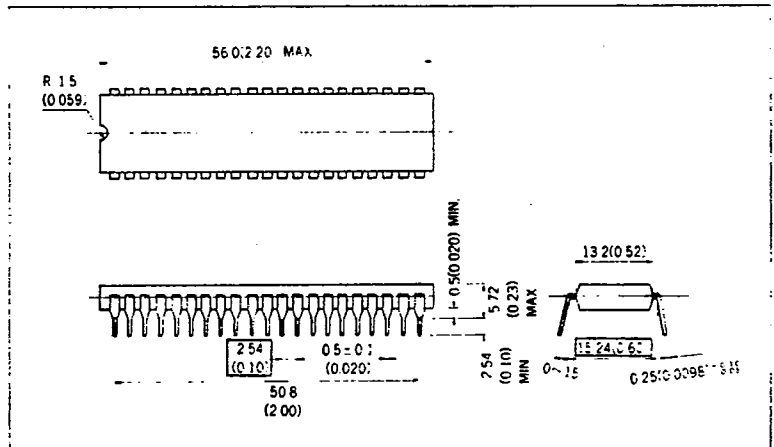
It makes such adjustments as chroma phase controller, "HORIZONTAL HOLD" and "VERTICAL HOLD" unnecessary.

So, number of components and adjustment man-hour are reduced remarkably.

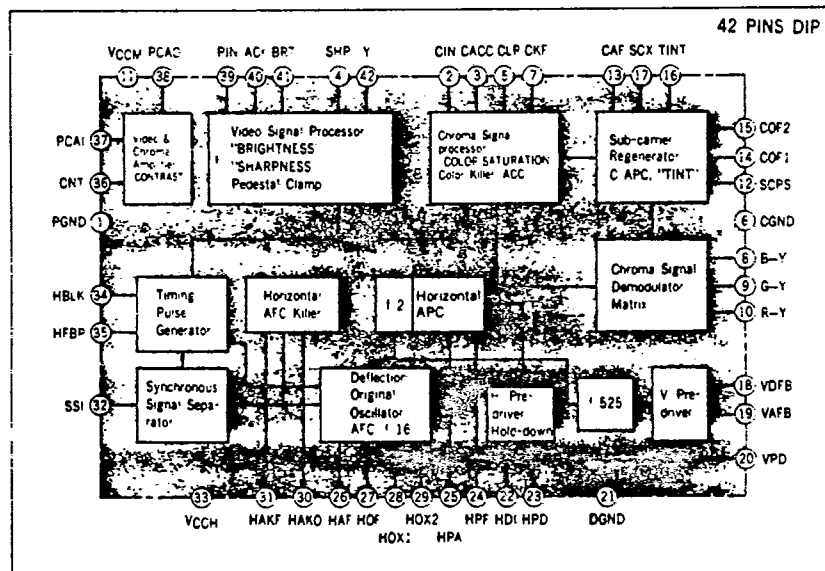
FEATURES

- Chroma sub-carrier regenerator works using a crystal resonator.
- Deflection original clock signal is generated using a ceramic resonator.
- All of user controls are controlled with DC voltage externally.
- Chroma difference signal output, and built-in Y (intensity of brightness) signal power stage.
- Clear view by the built-in aperture correction circuit.
- Freely programable video DC restration externally.

PACKAGE DIMENSIONS Unit : in millimeters (inches)



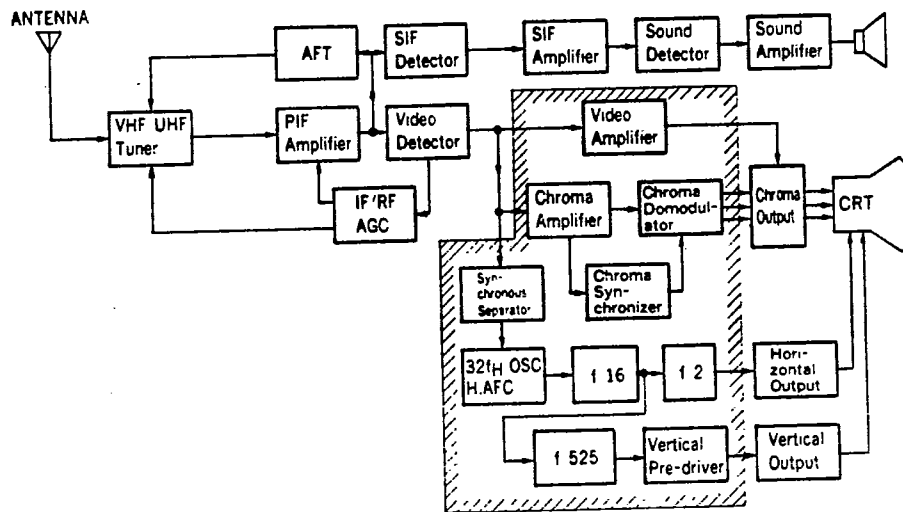
BLOCK DIAGRAM



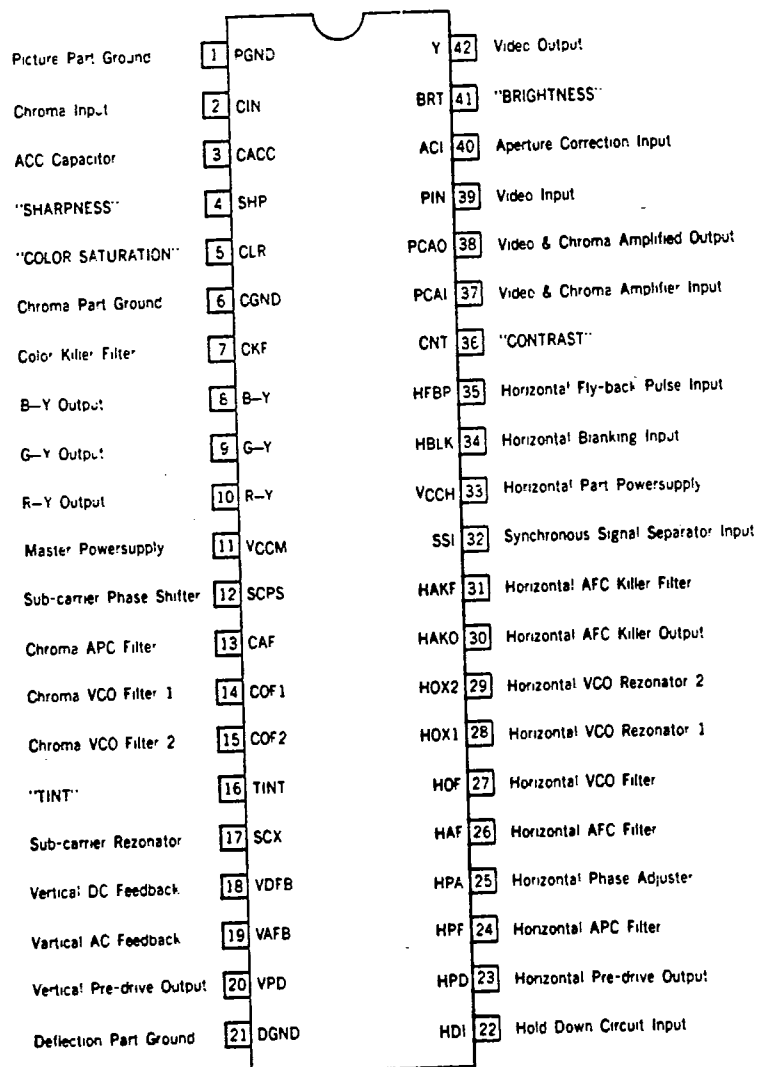
**μPC1401C**

**NEC** ELECTRON DEVICE

**TV BLOCK DIAGRAM**



**CONNECTION DIAGRAM (Top View)**



ABSOLUTE MAXIMUM RATINGS ( $T_s=25^\circ\text{C}$ )

Master Powersupply Voltage	$V_{CCM}$	13.5	V
Horizontal Powersupply Voltage	$V_{CCH}$	13.5	V
V & C Amplifier Input Voltage	$V_{PCAI}$	5.0	V
Chroma Input Voltage	$V_{CIN}$	5.0	V
Synch. Separator Input Voltage	$V_{SSI}$	5.0	V
H. Flyback Pulse Input Voltage	$V_{HFBP}$	$V_{CCH}$	V
H. Blanking Pulse Input Voltage	$V_{HBLK}$	$V_{CCH}$	V
Video Output Current	$I_Y$	50 ( $V_Y < 5.0\text{ V}$ )	mA
B-Y, G-Y, R-Y Output Current	$I_{B-Y}, I_{G-Y}, I_{R-Y}$	-10	mA
H. Pre-driver Output Current	$I_{HPD}$	$\pm 10$	mA
V. Pre-driver Output Current	$I_{VPD}$	-10	mA
Total Power Dissipation	$P_D$	1.4 ( $T_s=60^\circ\text{C}$ )	W
Operating Temperature	$T_{opt}$	-10 to +60	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-40 to +150	$^\circ\text{C}$

Mark "-" of current means flow out from the terminal.

RECOMMENDED OPERATING CONDITIONS ( $T_s=25^\circ\text{C}$ )

Master Power-supply Voltage	$V_{CCM}$	$12 \pm 1$	V
Horizontal Power-supply Voltage	$V_{CCH}$	$12 \pm 1$	V
V & C Input Signal Level	$e_{PCAI}$	1	$V_{p-p}$
Chroma Input Signal Level	$e_{CIN}$	200 (Burst Signal)	$mV_{p-p}$
H. Blanking Pulse Input Voltage	$e_{HBLK}$	More than 7	$V_{p-p}$
H. Flyback Pulse Input Voltage	$e_{HFBP}$	More than 7	$V_{p-p}$
Video Output Voltage	$E_Y$	6 (Pedestal Level)	V
"CONTRAST" Control Voltage	$V_{CNT}$	0 to (4 to 5) to $V_{CCM}$	V
"BRIGHTNESS" Control Voltage	$V_{BRT}$	0 to (8 to 9) to $V_{CCM}$	V
"SHARPNESS" Control Voltage	$V_{SHP}$	0 to (4 to 5) to $V_{CCM}$	V
"COLOR SATURATION" Control Voltage	$V_{CLR}$	$V_{CCM}$ to (5 to 4) to 0	V
"TINT" Control Voltage	$V_{TINT}$	0 to (4 to 5) to $V_{CCM}$	V
Hold-down Circuit Input Voltage	$V_{HDI}$	Trigger level is 0.7	V
H. Pre-driver Output Current	$I_{HPD}$	$\pm 2$	mA

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ELECTRICAL CHARACTERISTICS ( $T_s=25^\circ\text{C}$ )

## Video &amp; Chroma Part

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Master Powersupply Current	$I_{CCM}$	42	55	75	mA	$V_{CCM} (=V_{CCH})=12\text{ V}$
B-Y Output Stability Depend On ACC -1	ACC1	-3	0	+3	dB	Burst level at CIN changes from 0 dB (200 mV <sub>p-p</sub> ) to +6 dB (400 mV <sub>p-p</sub> ).
B-Y Output Stability Depend On ACC -2	ACC2	-7	-3	+2	dB	Burst level at CIN changes from 0 dB (200 mV <sub>p-p</sub> ) to -20 dB (20 mV <sub>p-p</sub> ).
Maximum Burst Signal Level Suppressed by Color Killer Function	$e_K$		-40		dB	0 dB = 200 mV <sub>p-p</sub> .
Remaining B-Y Signal Under Suppression of Color Killer Function	$e_{B-Y(K)}$			50	mV <sub>p-p</sub>	Remaining B-Y signal level when burst signal is applied to CIN at $e_K$ level.
Remaining B-Y Signal At Minimum Of "COLOR SATURATION"	$e_{B-Y(CLR)}$			20	mV <sub>p-p</sub>	Remaining B-Y signal level when CLR voltage is 9 V.
B-Y Signal Distribution In Standard Condition	$e_{B-Y(SC)}$	1.5	2.5	3.6	V <sub>p-p</sub>	Burst level at CIN is 200 mV <sub>p-p</sub> . CLR voltage is 7.1 V.
Maximum B-Y Signal Level	$e_{B-Y(MAX)}$	5.0	5.8		V <sub>p-p</sub>	Burst level at CIN is 200 mV <sub>p-p</sub> . CLR voltage is 0 V.
Variable Range of B-Y Signal Phase Depend On "TINT" Control Function	$\Delta\theta_{B-Y}$	80	90		deg.	TINT voltage changes from 0 V to $V_{CCM}$ .
B-Y Signal Distribution At Standard "CONTRAST" Control Voltage	$e_{B-Y(CNT)}$	1.4	2.0	2.4	V <sub>p-p</sub>	Burst level at CIN is 200 mV <sub>p-p</sub> . Adjust B-Y signal level to 2.5 V <sub>p-p</sub> with "COLOR SATURATION" control function when CNT voltage is 9V. After it, set CNT voltage to 4.7 V.
Variable Range of B-Y Signal Level Depend On "CONTRAST" Control Function	$\Delta e_{B-Y(CNT)}$	10.5	11.5	12.5	dB	Burst level at CIN is 200 mV <sub>p-p</sub> . Adjust B-Y signal level to 2.5 V <sub>p-p</sub> with "CONTRAST" control function when CNT voltage is 9 V. After it, set CNT voltage to 0 V.
Variable Frequency Range of Regenerated Sub-carrier -1	$f_{SC1}$	400	580	750	kHz	Frequency aberration of SCPS signal from 3 579.545 kHz. CAF voltage is 4.5 V.
Variable Frequency Range of Regenerated Sub-carrier -2	$f_{SC2}$	-800	-1050	-1300	kHz	Frequency aberration of SCPS signal from 3 579.545 kHz. CAF voltage is 7.5 V.
Peak Voltage of CAF Signal Under Control Of Internal Automatic Sweep Function	$V_{PCAF}$	7.0	7.2	7.5	V	PCAI input is deflection synchronous signal only. The input level is 300 mV <sub>p-p</sub> .
Bottom Voltage Of CAS Signal Under Control Of Internal Automatic Sweep Function	$V_{BCAF}$	4.3	4.6	4.8	V	PCAI input is deflection synchronous signal only. The input level is 300 mV <sub>p-p</sub> .
Chroma Demodulator Output Ratio -1	R-Y/B-Y	0.68	0.75	0.82	V/V	R-Y level divided by B-Y. CIN input is 200 mV <sub>p-p</sub> at the burst level, and 400 mV <sub>p-p</sub> at the coloring ingredient. Frequency of the coloring ingredient is 3.63 MHz.
Chroma Demodulator Output Ratio -2	G-Y/B-Y	0.20	0.25	0.31	V/V	G-Y level divided by B-Y. CIN input is 200 mV <sub>p-p</sub> at the burst level, and 400 mV <sub>p-p</sub> at the coloring ingredient. Frequency of the coloring ingredient is 3.63 MHz.

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
R-Y Demodulation Angle	$\angle R-Y$	90	98	106	deg.	R-Y vector angle against B-Y vector. Burst level of CIN input is 200 mV <sub>p-p</sub> .
G-Y Demodulation Angle	$\angle G-Y$	230	240	250	deg.	G-Y vector angle against B-Y vector. Burst level of CIN input is 200 mV <sub>p-p</sub> .
Demodulator Output DC Voltage Distribution	$E_o$	6.6	7.1	7.6	V	DC voltage of B-Y, G-Y, and R-Y, when no input to CIN.
Temperature Coefficient Of $E_o$	$\Delta E_o(T_a)$		0	$\pm 2$	mV/°C	Ambient Temperature changes from -10 °C to +60 °C
Non-uniformity of $E_o$	$dE_o$		0	$\pm 200$	mV	DC voltage difference among B-Y, G-Y, and R-Y, at tracing time.
Supply Voltage Dependence of $dE_o$	$\Delta dE_o(V_{CCM})$		0	50	mV	$V_{CCM}$ changes from 11 V to 13 V. $V_{CCH}=V_{CCM}$
Temperature Coefficient of $dE_o$	$\Delta dE_o(T_a)$		0	+1	mV/°C	Ambient Temperature changes from -10 °C to +60 °C
Remaining Carrier Wave Level Of Demodulator Output	$e_{carry}$		60	120	mV	Remaining sub-carrier wave level of B-Y, G-Y, and R-Y in tracing time (Contains harmonic over-tone ingredient), when no input to CIN.
Harmonic Over-tone Of Demodulator Output	$e_{hot}$		0.6	1.0	V <sub>p-p</sub>	Harmonic over-tone level of B-Y, G-Y, and R-Y (Contains remaining sub-carrier) Burst signal level of CIN input is 200 mV <sub>p-p</sub> .
Maximum Voltage Gain Of Video & Chroma Amplifier	APCA	6.0	7.0	9.0	dB	PCAO signal level comparing with PCAI input. The PCAI input is shown by Fig. 2 in page 8. CNT voltage is 9 V.
PCAO Signal Distribution At Standard "CONTRAST" Control Voltage	$e_{PCAO}(CNT)$	1.3	1.8	2.3	V <sub>p-p</sub>	PCAO output level, when CNT voltage is 4.7 V. PCAI input is shown by Fig. 2 in page 8.
Variable Range Of PCAO Output Depend On "CONTRAST" Control Function	$\Delta e_{PCAO}(CNT)$	11	12	13	dB	Variable Range of PCAO output level when CNT voltage is changed from 0 V to 9 V. PCAI input is shown by Fig. 2 in page 8.
Frequency Response Of Video & Chroma Amplifier	FRPCA	-3	0		dB	Gain inconstancy when PCAI input signal frequency changes from 200 kHz to 4.2 MHz. PCAI input signal is shown by Fig. 1 in page 8.
Voltage Gain Of Video Signal Processor	APSP	10	12	14	dB	Y output level comparing with PIN input signal. PCAI input signal is shown by Fig. 1 in page 8. The input signal frequency is 200 kHz.
"BRIGHTNESS" Control Voltage Distribution for Standard Y Output Level	V <sub>BRT</sub>	7.9	8.2	8.5	V	Applied BRT voltage when black level of Y output is controlled to 6 V. PCAI input is 300 mV <sub>p-p</sub> deflection synchronous signal only.
Y Black Level At a BRT Voltage -1	V <sub>Y(BRT)1</sub>	6.0	7.0		V	Black level of Y output when BRT voltage is 7.5 V. PCAI input is 300 mV <sub>p-p</sub> deflection synchronous signal only.
Y Black Level At a BRT Voltage -2	V <sub>Y(BRT)2</sub>		1.5	2.0	V	Black level of Y output when BRT voltage is 9.5 V. PCAI input is 300 mV <sub>p-p</sub> deflection synchronous signal only.

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CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Frequency Response Of Video Signal Processor Depend On "SHARPNESS" Control Function -1	FRY(SHP)1	-5.5	-3.5	-1.5	dB	Difference of gain for 2 MHz signal against one for 200 kHz signal, when SHP voltage is 9 V. PCAI input is shown by Fig. 1 in page 8.
Frequency Response Of Video Signal Processor Depend On "SHARPNESS" Control Function -2	FRY(SHP)2	+6.0	+9.0	+12	dB	Difference of gain for 2 MHz signal against one for 200 kHz signal, when SHP voltage is 0 V. PCAI input is shown by Fig. 1 in page 8.
Null Point Of "SHARPNESS" Control Voltage	VNSHP	4.6	4.9	5.2	V	SHP voltage is adjusted as frequency response of video signal processor is constant for signal from 200 kHz to 2.0 MHz. PCAI Input is shown by Fig. 1 in page 8.
Temperature Coefficient Of Y Black Level	$\Delta V_Y(T_a)$	0	+2.5	+5.0	mV/°C	Temperature Coefficient of black level of Y output when ambient temperature changes from -10 °C to +60 °C. Black level of Y output is set to 6 V at 25 °C.

Synchronization & Deflection Part

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Horizontal Part Powersupply Current	I <sub>CCH</sub>	8	12	16	mA	V <sub>CCH</sub> (=V <sub>CCM</sub> )=12 V	
Synchronous Signal Separator Input DC Voltage	ESSI	7.3	7.6	7.9	V	SSI terminal DC voltage with no input.	
Vertical Free-running Frequency -1	f <sub>vo1</sub>		f <sub>H</sub> :296		Hz	Frequency ratio of VDFB terminal signal against HPD output, when SSI voltage is set to V <sub>CCM</sub> .	
Vertical Free-running Frequency -2	f <sub>vo2</sub>		f <sub>H</sub> :232		Hz	Frequency ratio of VDFB terminal signal against HPD output, when SSI voltage is set to 0 V.	
Lowest VDFB Input Voltage Interrupting VPD Pulse	V <sub>LVDFB</sub>	3.7	4.0	4.3	V	Lowest VDFB voltage with which VPD output is disappeared.	
Vertical Blanking Pulse Width	PW <sub>VBLK</sub>	See Fig. 3 in page 8					Watch blanking time length of Y output. PCAI input is 300 mV <sub>p-p</sub> deflection synchronous signal only.
VPD Output Pulse Width	PW <sub>VPD</sub>	See Fig. 3 in page 8					Watch VPD output pulse width. PCAI input is 300 mV <sub>p-p</sub> deflection synchronous signal only.
Voltage Gain Distribution Of Vertical Pre-driver	A <sub>VPD</sub>	4.5	6.0	7.5	V/V	Change of VPD output comparing with change of VAFB input when VAFB DC voltage is changed from 3.5 V to 3.7 V.	
Lowest V <sub>CCM</sub> Available To Vertical Frequency Divider	V <sub>LCCM</sub> (VO)		3.3	4.0	V	Lowest V <sub>CCM</sub> with which VDFB pulse appears. PCAI input is 300 mV <sub>p-p</sub> deflection synchronous signal only.	
Lowest V <sub>CCM</sub> Available To Vertical Synchronizer	V <sub>LCCM</sub> (VS)		4.1	5.0	V	Lowest V <sub>CCM</sub> with which VDFB terminal signal synchronizes with synchronous signal of PCAI input. The input is 300 mV <sub>p-p</sub> deflection synchronous signal only.	
Horizontal Free-running Frequency	f <sub>HO</sub>	-50	0	+50	Hz	Frequency aberration of HPD output from 15.734 kHz.	

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage Dependence Of $f_{HO}$ -1	$\Delta f_{HO}(V_{CCH}1)$		$\pm 5$	$\pm 20$	Hz	Frequency change of HPD output when $V_{CCH}$ is changed from 11 V to 13 V. $V_{CCM}=V_{CCH}$ . Compare with HPD output frequency at $V_{CCH}$ is 12 V.
Supply Voltage Dependence Of $f_{HO}$ -2	$\Delta f_{HO}(V_{CCH}2)$	0	-40	-100	Hz	Frequency change of HPD output at $V_{CCH}$ is 7.0 V comparing with frequency at $V_{CCH}$ is 12 V. $V_{CCM}=V_{CCH}$
Drift Of $f_{HO}$ Depend On Ambient Temperature	$\Delta f_{HO}(T_a)$			$\pm 20$	Hz	Frequency drift of HPD output when ambient temperature changes from $-10^\circ\text{C}$ to $+60^\circ\text{C}$ . Compare with the frequency at ambient temperature is $25^\circ\text{C}$ .
Horizontal Synchronous Capture Range	$f_{HC}$	$\pm 500$	$\pm 600$		Hz	Farthest frequency of synchronous signal of PCA1 input which can be captured by horizontal AFC function. PCA1 input is 300 mV <sub>p-p</sub> variable frequency horizontal synchronous signal only. PCA1 input pulse width is 4.8 $\mu\text{s}$ .
Horizontal Pre-driver Output Pulse Width	$PW_{HPD}$	19	21	23	$\mu\text{s}$	High level time of HPD output. PCA1 input is 300 mV <sub>p-p</sub> deflection synchronous signal only.
Phase Change Of HPD Output Depend On Frequency Of Synchronous Signal	$\Delta\phi_H$		2	3	$\mu\text{s}/600\text{ Hz}$	Watch phase change of HPD output comparing with PCA1 input when synchronous signal frequency of PCA1 changes from 15.434 kHz to 16.034 kHz.
Lowest $V_{CCH}$ Available To Horizontal Part	$V_{LCCH}$		4.0	5.0	V	Lowest $V_{CCH}$ with which HPD output appears. PCA1 input is 300 mV <sub>p-p</sub> deflection synchronous signal only.
Maximum Deflection Synchronous Signal Level Triggering Horizontal AFC Killer	$e_{PCA1}(HAK)$	-14	-10	-6	dB	Maximum synchronous signal level of PCA1 input with which HAKO terminal voltage keeps above 1.0 V. PCA1 input is deflection synchronous signal only. 0 dB = 250 mV <sub>p-p</sub> .
Lowest Triggering Voltage Of HDI Input	$E_{HDI}$	580	640	700	mV	Lowest HDI input voltage with which HPD output is disappeared.
Lowest $V_{CCH}$ Keeping Hold Down Work	$V_{CCH}(HD)$			3.0	V	After trigger hold down circuit, lowest $V_{CCH}$ with which hold down circuit can keep the work.

Fig. 1 TEST SIGNAL OF FR<sub>PCA</sub>, A<sub>PSP</sub>, F<sub>RY(SHP)1</sub>, F<sub>RY(SHP)2</sub>, AND V<sub>NSHP</sub>

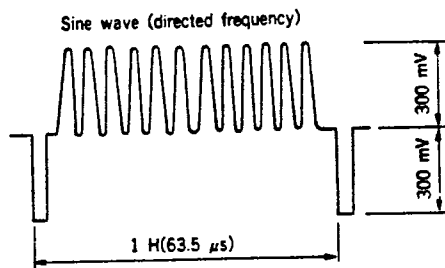


Fig. 2 TEST SIGNAL OF A<sub>PCA</sub>, e<sub>PCAO(CNT)</sub>, AND 4e<sub>PCAO(CNT)</sub>

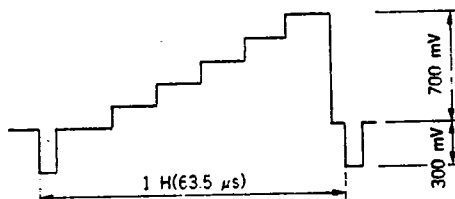
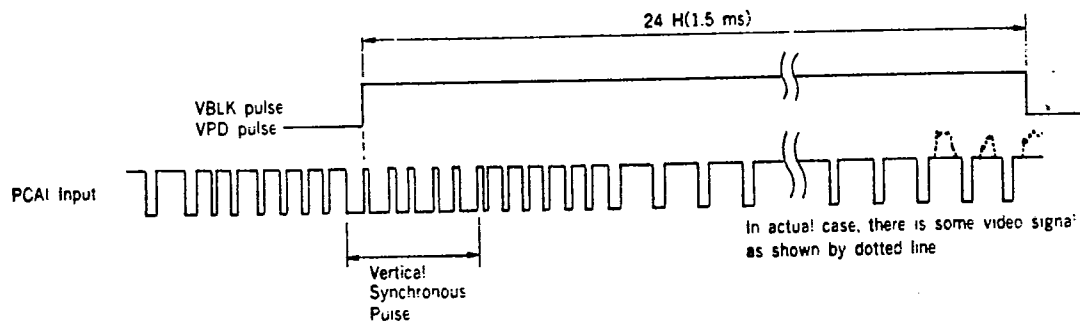
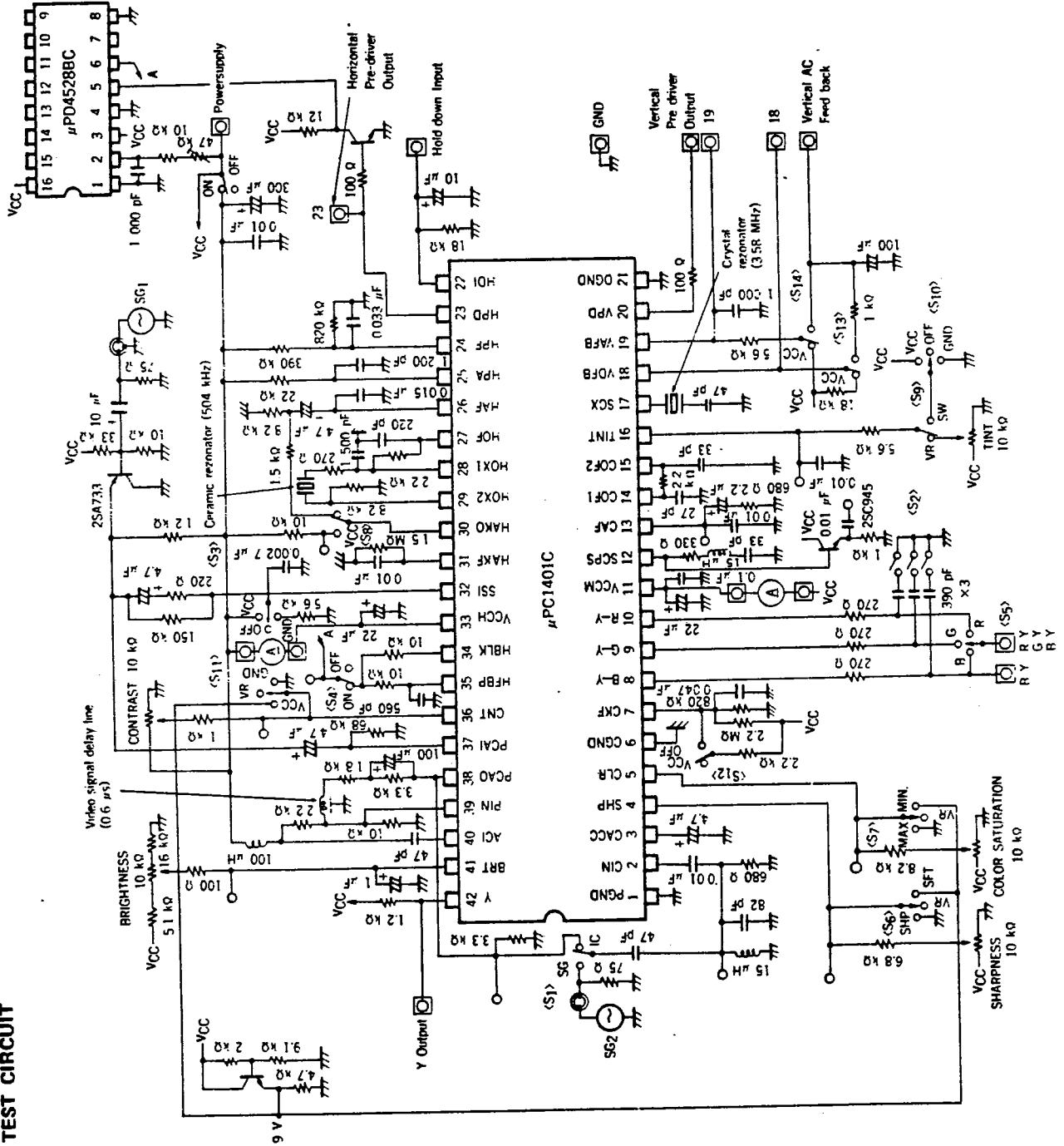


Fig. 3 SIGNAL TIMING OF PW<sub>VBLK</sub>, AND PW<sub>VPD</sub>



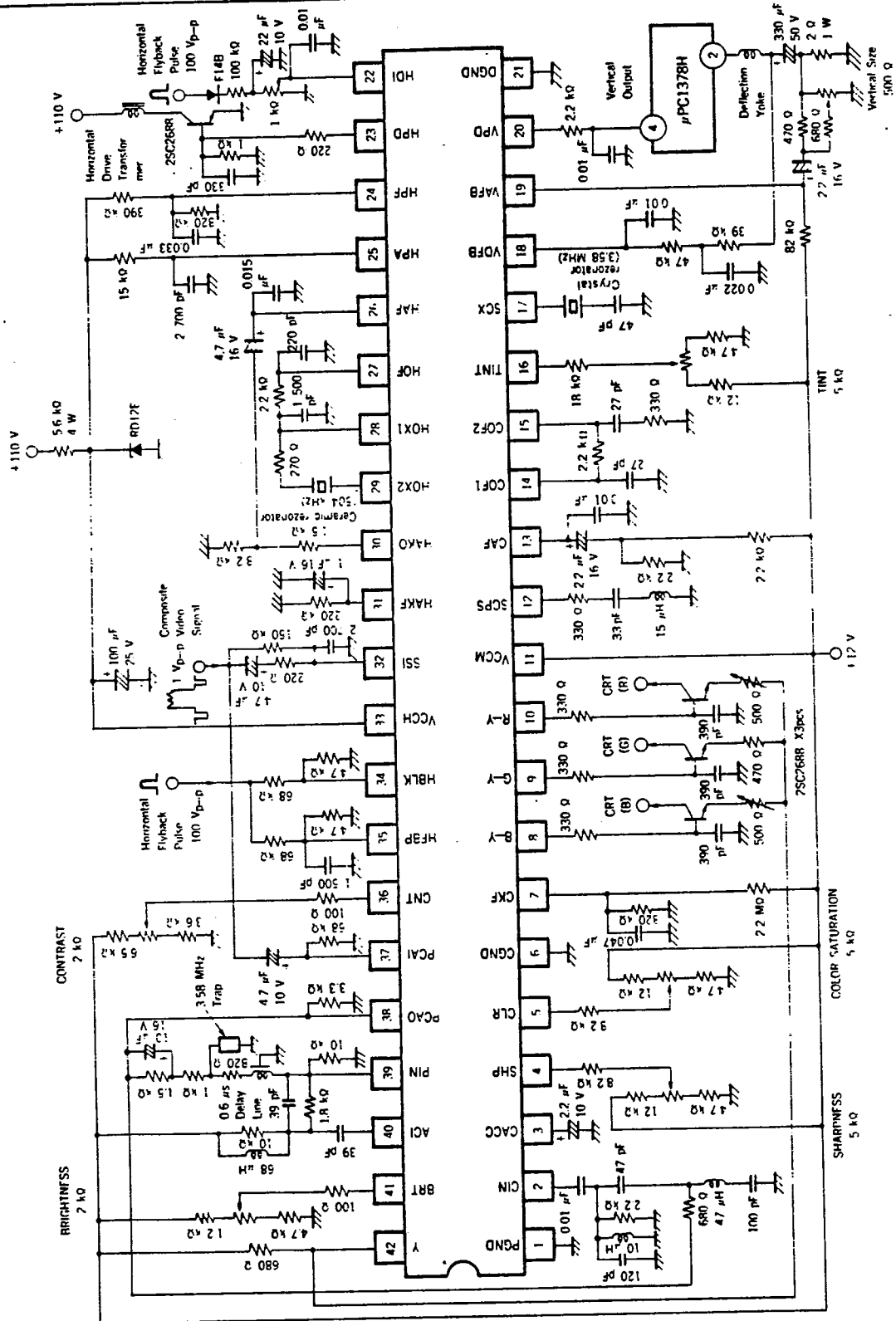


TEST CIRCUIT



$\mu$ PC1401C

EXAMPLE OF APPLICATION CIRCUIT



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