SIEMENS

V23814-K1306-M230
Parallel Optical Link: PAROLI™ Tx DC/MUX-ENC

V23815-K1306-M230
Parallel Optical Link: PAROLI™ Rx DC/DEMUX-DEC

Preliminary

Dimensions in (mm) inches

FEATURES
- **Power supply (3.3 V)**
- **Low voltage differential signal electrical interface (LVDS)**
- **22 electrical data + 1 clock channels**
- **Synchronous, DC-coupled optical link**
- **12 optical data channels**
- **Electrical transmission data rate of 200-500 Mbit/s per channel, total link data rate up to 11 Gbit/s**
- **Two clocking modes can be selected**
- **Transmission distance depends on data rate and fiber skew, up to 75 m at maximum data rate**
- **Transmitter: 840 nm VCSEL (Vertical Cavity Surface Emitting Laser) technology**
- **Receiver: 840 nm PIN diode array**
- **Fiber ribbon: 62.5 μm graded index multimode fiber**
- **MT based optical port**
- **SMD technology**
- **Transmitter: Class 1 FDA and Class 3A IEC laser safety compliant**

APPLICATIONS

Telecommunication
- **Switching equipment**
- **Access network**

Data Communication
- **Interframe (rack-to-rack)**
- **Intraframe (board-to-board)**
- **On board (optical backplane)**
- **Interface to SCI and HIPPI 6400 standards**

Absolute Maximum Ratings

Stress beyond the values stated below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Supply Voltage (V_{CC}–V_{EE}) .... –0.3 V to 4.5 V
Data/Control Input Levels (V_{IN})[1] .... –0.5 V to V_{CC}+0.5 V
LVDS Input Differential Voltage ($|V_{ID}|$)[2] .... 2.0 V
Operating Case Temperature (T_{CASE})[3] .... 0°C to 80°C
Storage Ambient Temperature (T_{STG}) .... –20°C to 100°C
Operating Moisture .... 20% to 85%
Storage Moisture .... 20% to 85%
Soldering Conditions Temp/Time (T_{SOLD}, t_{SOLD})[4] ....260°C/10s
ESD Resistance (all pins to V_{EE} human body model)[5] .... 1 kV

Notes
1. At LVDS and LVCMOS inputs.
2. $|V_{ID}|=|$(input voltage of non-inverted input minus input voltage of inverted input)$|$.
3. Measured at case temperature reference point (see dimensional drawing).
4. Hot bar soldering.
5. To avoid electrostatic damage the handling precautions as for MOS devices must be taken into account.

DESCRIPTION

PAROLI is a parallel optical link for high-speed data transmission. A complete PAROLI system consists of a transmitter module, a 12-channel fiber optic cable, and a receiver module.

Transmitter V23814-K1306-M230

The PAROLI transmitter module converts parallel electrical input signals (data and clock) into parallel optical output signals.

Figure 1. Transmitter block diagram
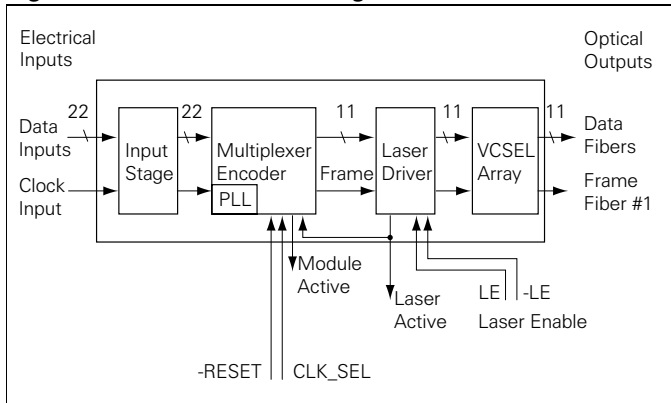
All electrical data and clock inputs are LVDS compatible. The module also features several LVCMOS compatible control inputs and outputs, which are described in the Transmitter Pin Description.

The module features multiplexing and encoding of 22 electrical data input channels to 11 optical data output channels. The input data are serialized by 2 to 1 multiplexers which results in a reduced data rate at the electrical interface. The multiplexed data are encoded (4B5B encoding) to achieve DC-balanced signals at the input of the laser driver.

The electrical input clock signal is used to control an integrated PLL circuit, which generates internal clock signals for encoding and multiplexing. The PLL circuit also generates a frame signal for the optical interface, which is transmitted over a separate fiber.

Transmission delay of the PAROLI system is at a maximum of 4 strobe cycles + 3 ns for the transmitter, 3 strobe cycles + 3 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

Clocking Modes

The transmitter can be operated in one of two input clocking modes: Strobe mode or SCI mode. The mode is selected via CLK_SEL input. In Strobe mode, the rising edges of the non-inverted clock signal are centered over the data bits. In SCI mode, High/Low transitions of clock and data signals coincide. In SCI mode, the transmitter's electrical interface complies with SCI and HIPPI standards. See Timing diagram Fig. 2.

Multiplexing and Encoding

The electrical input data is strobed into the input register with the internal clock signal generated by the PLL and then multiplexed 2:1. Input channels 1 to 11 are grouped with input channels 12 to 22, i.e. data inputs 1 and 12 feed optical data output 1; data inputs 2 and 13 feed optical data output 2, etc.

Four data bits read from two input channels during two strobe cycles form 4B words. Inside the 4B word, data from the lower inputs (1 to 11) is transmitted first, i.e. after input data is

strobed. Inputs 1 to 11 are routed before inputs 12 to 22. 4B words are then fed through eleven separate 4B/5B encoders to form the signals to be transmitted over the optical interface. Coding is based on the running disparity of previously transmitted output data. With a running disparity ≥0, either more High than Low levels or an equal number of Highs and Lows have been transmitted. The next output nibble will be inverted if High levels again dominate; otherwise it will be sent without inversion. With a running disparity <0, more Low than High levels have been transmitted. The next output nibble will be inverted if Low levels again dominate; otherwise it will be sent uninverted.

To indicate whether a nibble has been inverted, an inversion bit is added, thus forming a 5B word (High, if transmitted nibble is uninverted; Low, if transmitted nibble is inverted). It is placed in front of the nibble (at the beginning of the 5B word) and immediately follows the FRAME transition. FRAME signal transitions delimit 5B words. Each 5B word contains the inversion bit and the nibble (inverted or non-inverted) mounted from two input data strobe cycles. The 5B words and FRAME signal are the signals transmitted over the optical interface. The pulse lengths of the 5B word and the frame signal is twice the pulse length of the electrical input signal.

Example

To transmit electrical data at the maximum data rate of 500 Mbit/s per channel the corresponding clock signal (square 0101 pattern) has a frequency of 250 MHz in SCI mode or 500 MHz in STROBE mode. The FRAME signal with a corresponding frequency of 125 MHz is transmitted via fiber #1. The data rate of the optical signal at the Transmitter output is 1.25 Gbit/s in each of the fibers #2 to #12.

LASER SAFETY

The transmitter of the DC coupled Parallel Optical Link (PAROLI) is an FDA Class 1 laser product. It complies with FDA regulations 21 CFR 1040.10 and 1040.11. The transmitter is an IEC Class 3A laser product as defined by IEC 825-1. To avoid possible exposure to hazardous levels of invisible radiation, do not exceed maximum ratings.

The PAROLI module must be operated under the specified operating conditions (supply voltage between 3.0 V and 3.6 V, case temperature between 0°C and 80°C) under all circumstances to ensure laser safety.
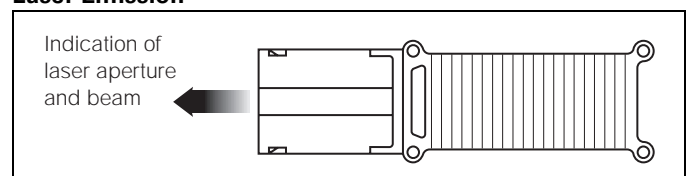
Caution

Do not stare into beam or view directly with optical instruments. The use of optical instruments with this product will increase eye hazard.

Note

Any modification of the module will be considered an act of "manufacturing," and will require, under law, recertification of the product under FDA (21 CFR 1040.10 (i)).

Laser Emission

START-UP PROCEDURE

Detailed information can be found in the data sheet of the Paroli Testboard AC/DC, part number V23814-S1306-M931 and V23815-S1306-M931.

- Switch system power supply on
- Release -RESET when VCC has reached 3.0 V level and clock input is stable
- Activate LE/-LE (laser enable) control input.
- Delay tSTARTUP until laser controller and PLL have settled
- After tSTARTUP, MU and MA will be high
- Apply data input

Module starts transmitting

TECHNICAL DATA

The electro-optical characteristics described in the following tables are valid only for operation under the recommended operating conditions.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	3.0	3.6	V
Noise on Power Supply[1]	N_{PS1}		10	mV
Noise on Power Supply[2]	N_{PS2}		100	
LVDS Input Voltage Range[3]	V_{LVDSI}	500	1900	
LVDS Input Differential Voltage[3, 4]	$|V_{ID}|$	100	1000	
LVDS Clock Input Rise/Fall Time[5]	t_R, t_F	100	400	ps
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0	V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}	0.8	
LVCMOS Input Rise/Fall Time[6]	t_R, t_F		20	ns
Clock Input Frequency, SCI Mode[7]	f_{CLOCK}	100	250	MHz
Clock Input Frequency, Strobe Mode[7]	f_{CLOCK}	200	500	MHz
Clock Input Duty Cycle Distortion	dcd	45	55	%
Input Skew between Clock Inputs[8]	t_{SPN}		0.75 x t_R, t_F	ps
Clock Input Total Jitter(pk-pk)	CJ		0.025	UI

Notes

Voltages refer to V_{EE}=0 V.

1. Noise frequency is 1 kHz to 1 MHz. Voltage is peak-to-peak value.
2. Noise frequency is 1 MHz to 1 GHz. Voltage is peak-to-peak value.

3. Level diagram:
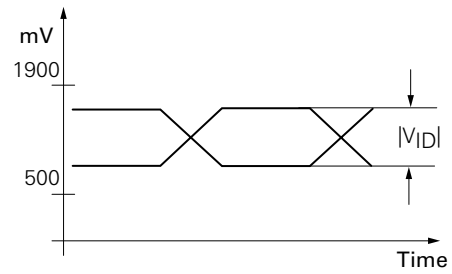
4. $|V_{ID}|=|$(input voltage of non-inverted input minus input voltage of inverted input)$|$.
5. See Measurement Conventions (Figure 3).
6. Measured between 0.8 V and 2.0 V.
7. Lower limit of clock frequency due to PLL frequency limitations.
8. See Measurement Conventions (Figure 3).

Transmitter Electro-Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Current	I_{CC}		940	1140	mA
Power Consumption	P		3.9	4.1	W
Data Rate in SCI Mode[1]	D_{RSCI}	200		500	Mbit/s
Data Rate in Strobe Mode[1]	D_{RSTR}				
LVDS Differential Input Impedance[2]	R_{IN}	80		120	Ω
LVCMOS Output Voltage Low	$V_{LVCMOSOL}$			0.4	V
LVCMOS Output Voltage High	$V_{LVCMOSOH}$	2.5			
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	−500		500	µA
LVCMOS Output Current High[3]	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output Current Low[4]	$I_{LVCMOSOL}$			4.0	
LVDS Differential Input Current	$|I_I|$			5.0	

Notes

1. Data rate on electrical channel. Number of consecutive high or low bits is unlimited.
2. LVDS Input stage.
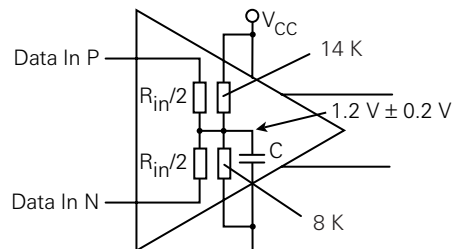
3. Source current
4. Sink current

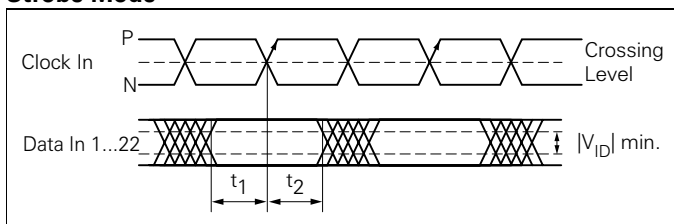| Parameter	Symbol	Min.	Max.	Units
Optical Rise Time[1]	t_R		400	ps
Optical Fall Time[1]	t_F			
Random Jitter (14σ)[2]	J_R		0.23	UI
Deterministic jitter	J_D		0.20	
Launched Average Power	P_{AVG}	−11	−6.0	dBm
Launched Power Shutdown	P_{SD}		−30	
Center Wavelength	λ_C	820	860	nm
Spectral Width (FWHM)	$\Delta\lambda$		2.0	
Relative Intensity Noise	RIN		−116	dB/Hz
Extinction Ratio (dynamic)	ER	5.0		dB

Notes

Optical parameters valid for each channel.

1. 20%–80% level.

2. Measured with 01010... (square) optical output pattern.
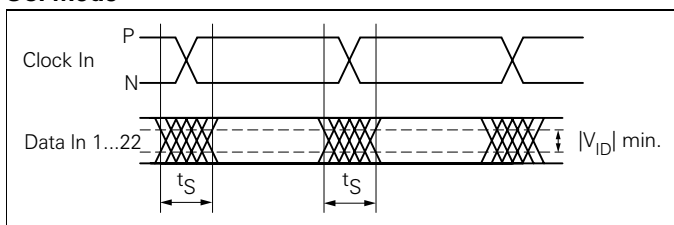
Figure 2. Timing diagram

Strobe Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
Input Setup Time[1]	t_1	250			ps
Input Hold Time[1]	t_2				

Note

1. Refers to positive clock input signal. See Measurement Conventions (Figure 3).

SCI Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
Input Skew[1]	t_S			§	ps

§. Maximum Input Skew=(2*Data Rate)$^{-1}$ – 250 ps – $DCD_{IN\text{-}CLOCK}$ where $DCD_{IN\text{-}CLOCK}=|(\text{Data Rate})^{-1}-dcd*(1/2 \text{ Data Rate})^{-1}|$ (dcd: see Recommended Operating Conditions).

Note

1. See Measurement Conventions (Figure 3).

Reset Timing Diagram
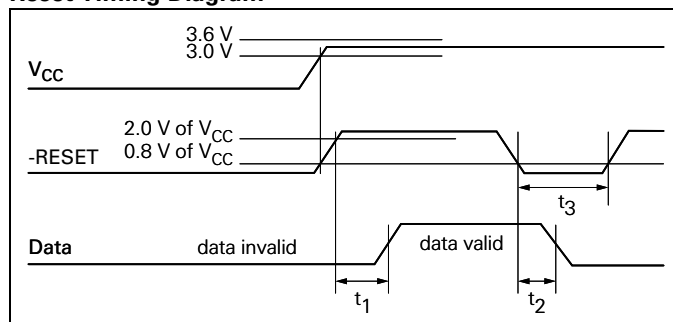
Parameter	Symbol	Min.	Typ.	Max.	Units
-RESET On Delay Time[1]	t_1			100	ms
-RESET Off Delay Time	t_2			50	µs
-RESET Low Duration[2]	t_3	tbd			ms

Notes

1. Valid after the release of -RESET. (Clock input must first be stable. Keep -RESET low until clock input is at stable frequency.)

2. Only when not used as power-on reset. At any failure recovery, -RESET should be brought to low level for at least t_3.
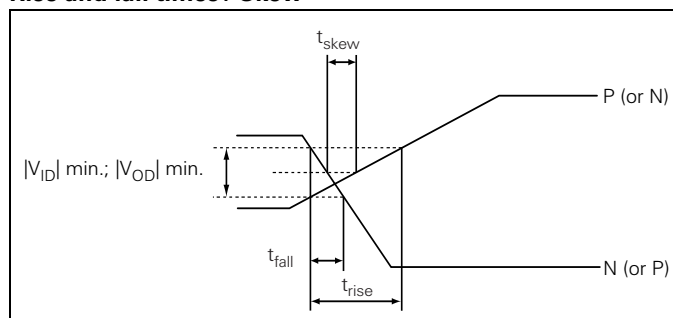
Figure 3. Measurement conventions for LVDS signals
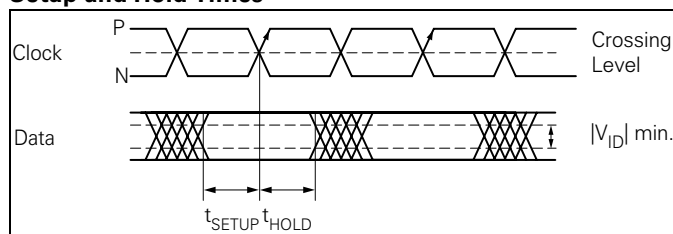
Setup and Hold Times

Setup and hold times are measured between the crosspoint of positive and negative clock and the points where rising and falling data edge cross the borders of the V-range.

Rise and fall times / Skew

Transmitter Pin Description

Pin#	Pin Name	Level/Logic	Description
1	V_{CC1}		Power supply voltage of laser driver
2	t.b.l.o.		to be left open
3			
4			
5			

Pin#	Pin Name	Level/Logic	Description
6	LA	LVCMOS Out	Laser Active High=laser controller is operational
7	V_{EE}		Ground
8	V_{EE}		Ground
9	V_{CC3}		Power supply voltage of digital circuitry and PLL
10	MA	LVCMOS Out	Module Active High=normal operation Low=laser fault or PLL not locked or -RESET low
11	CIN	LVDS In	Clock Input, inverted
12	CIP	LVDS In	Clock Input, non-inverted
13	DI01N	LVDS In	Data Input #1, inverted
14	DI01P	LVDS In	Data Input #1, non-inverted
15	DI12N	LVDS In	Data Input #12, inverted
16	DI12P	LVDS In	Data Input #12, non-inverted
17	DI02N	LVDS In	Data Input #2, inverted
18	DI02P	LVDS In	Data Input #2, non-inverted
19	DI13N	LVDS In	Data Input #13, inverted
20	DI13P	LVDS In	Data Input #13, non-inverted
21	DI03N	LVDS In	Data Input #3, inverted
22	DI03P	LVDS In	Data Input #3, non-inverted
23	DI14N	LVDS In	Data Input #14, inverted
24	DI14P	LVDS In	Data Input #14, non-inverted
25	V_{CC3}		Power supply voltage of digital circuitry and PLL
26	DI04N	LVDS In	Data Input #4, inverted
27	DI04P	LVDS In	Data Input #4, non-inverted
28	V_{EE}		Ground
29	DI15N	LVDS In	Data Input #15, inverted
30	DI15P	LVDS In	Data Input #15, non-inverted
31	DI05N	LVDS In	Data Input #5, inverted
32	DI05P	LVDS In	Data Input #5, non-inverted
33	DI16N	LVDS In	Data Input #16, inverted
34	DI16P	LVDS In	Data Input #16, non-inverted
35	DI06N	LVDS In	Data Input #6, inverted
36	DI06P	LVDS In	Data Input #6, non-inverted
37	DI17N	LVDS In	Data Input #17, inverted
38	DI17P	LVDS In	Data Input #17, non-inverted
39	DI07N	LVDS In	Data Input #7, inverted
40	DI07P	LVDS In	Data Input #7, non-inverted
41	DI18N	LVDS In	Data Input #18, inverted
42	DI18P	LVDS In	Data Input #18, non-inverted
43	DI08N	LVDS In	Data Input #8, inverted
44	DI08P	LVDS In	Data Input #8, non-inverted
45	V_{EE}		Ground
46	DI19N	LVDS In	Data Input #19, inverted
47	DI19P	LVDS In	Data Input #19, non-inverted

Pin#	Pin Name	Level/Logic	Description
48	V_{CC3}		Power supply voltage of digital circuitry and PLL
49	DI09N	LVDS In	Data Input #9, inverted
50	DI09P	LVDS In	Data Input #9, non-inverted
51	DI20N	LVDS In	Data Input #20, inverted
52	DI20P	LVDS In	Data Input #20, non-inverted
53	DI10N	LVDS In	Data Input #10, inverted
54	DI10P	LVDS In	Data Input #10, non-inverted
55	DI21N	LVDS In	Data Input #21, inverted
56	DI21P	LVDS In	Data Input #21, non-inverted
57	DI11N	LVDS In	Data Input #11, inverted
58	DI11P	LVDS In	Data Input #11, non-inverted
59	DI22N	LVDS In	Data Input #22, inverted
60	DI22P	LVDS In	Data Input #22, non-inverted
61	CLK-SEL	LVCMOS In	Input Clocking Mode Select High=strobe mode Low=SCI mode This input has an internal pull-up resistor. When left open, strobe mode is active.
62	t.b.l.o.		to be left open
63	V_{CC3}		Power supply voltage of digital circuitry and PLL
64	-RESET	LVCMOS In low active	High=normal operation Low=resets module, shuts laser diode array down This input has an internal pull-down resistor to ensure laser safety switch-off in case of unconnected -RESET input.
65	V_{EE}		Ground
66	V_{EE}		Ground
67	LE	LVCMOS In	Laser ENABLE. High=laser array is on if -LE is also active. Low=laser array is off. This input can be used for connection with an Open Fiber Control (OFC) circuit to enable IEC class 1 links. Has an internal pull-up, therefore can be left open.
68	-LE	LVCMOS In low active	Laser ENABLE. Low=laser array is on if LE is also active. This input can be used for connection with an Open Fiber Control (OFC) circuit to enable IEC class 1 links. Has an internal pull-down, therefore can be left open.
69	t.b.l.o.		to be left open
70	t.b.l.o.		to be left open
71	t.b.l.o.		to be left open
72	V_{CC1}		Power supply voltage of laser driver

DESCRIPTION

Receiver V23815-K1306-M230

The PAROLI receiver module converts parallel optical input signals (data and frame) into parallel electrical output signals.

Figure 4. Receiver block diagram
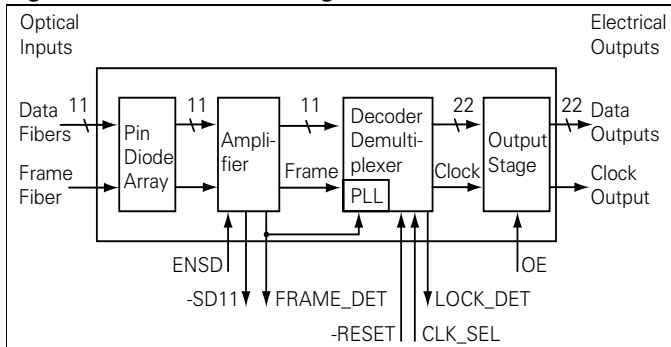
All electrical data and clock inputs are LVDS compatible. The module also features several LVCMOS compatible control inputs and outputs, which are described in the Receiver Pin Description.

The module features demultiplexing and decoding of 11 optical data input channels to 22 electrical data output channels. The frame signal is used to control an integrated PLL circuit, which generates internal clock signals for decoding and demultiplexing. The PLL circuit also generates a clock signal at the Receiver output.

Transmission delay of the PAROLI system is at a maximum of 4 strobe cycles + 3 ns for the transmitter, 3 strobe cycles + 3 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

Clocking Modes

The receiver can be operated in one of two output clocking modes: Strobe mode or SCI mode. The mode is selected via CLK_SEL input. In Strobe mode, the rising edges of the non-inverted clock signal are centered over the data bits. In SCI mode, High/Low transitions of clock and data signals coincide In SCI mode the electrical interface complies with SCI and HIPPI standards. See Timing diagram Fig. 5.

Decoding and Demultiplexing

The input data received from the optical interface is strobed into the input register with the PLL generated internal clock signal. The data is read in relation to FRAME input. The input frequency expected at FRAME is one fifth of square input data frequency, as FRAME transitions indicate 5B word boundaries. FRAME input is expected to change levels simultaneously with data transitions.

All eleven input data channels are fed through individual 5B/4B decoders. Decoding is based on an inversion bit which is received at the first position of a 5B word. This bit determines whether the nibble received at bit positions 2, 3, 4 and 5 has to be inverted. An inversion bit High level indicates a nibble which was transmitted uninverted, i.e. this 4B nibble will be directly forwarded to the demultiplexer. If the inversion bit received is Low, the corresponding nibble will be inverted by the decoder before it is demultiplexed.

The 4B words from the decoders are then demultiplexed 1:2 to electrical output data channels. Output channels 1 to 11 are grouped with output channels 12 to 22, i.e. optical data input 1 feeds electrical data outputs 1 and 12; optical data input 2 feeds electrical data outputs 2 and 13, etc.

Demultiplexing of a 4B word (with bits #1...#4) takes two data output cycles.

During the first cycle, bit #1 is presented at the lower data output (1...11) and bit #2 at the higher data output (12...22). During the second cycle, bits #3 and #4 are presented at the lower and higher outputs, respectively.

(Example: Of the 4B word from optical data channel 1, bit #1 is presented at corresponding lower data output 1 and bit #2 is presented at corresponding higher data output 12.)

The demultiplexed data bits are presented as 22 parallel outputs together with the output clock signal, the characteristics of which depend on the clocking mode. (See Clocking Modes above.)

Start-up Procedure

Detailed information can be found in the data sheet of the Paroli Testboard AC/DC, part number V23815-S1306-M931.
- Switch system power supply on
- Release -RESET when VCC has reached 3.0 V level
- Wait for LOCK_DET to become High
- Module starts presenting data at the data outputs if OE is High.

If OE is at a high level or left open during start-up, clock output will start running immediately after release of -RESET. Clock frequency will drift upwards to the operating frequency established by FRAME input when FRAME_DET indicates sufficient input signal level. After PLL has locked (indicated by LOCK_DET high level) data outputs are also enabled. OE can be used for complete LVDS switch-off whenever clock drift during start-up is critical.

TECHNICAL DATA
Recommended Operating Conditions

| Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	3.0	3.6	V
Noise on Power Supply[1]	N_{PS1}		10	mV
Noise on Power Supply[2]	N_{PS2}		100	
Differential LVDS Termination Impedance	R_t	80	120	Ω
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0	V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}	0.8	
LVCMOS Input Rise/Fall Time[3]	t_R, t_F		20	ns
Optical FRAME Input Frequency	f_{FRAME}	50	125	MHz
Optical Data, FRAME Input Skew[4]	t_{SI}		tbd	
Optical FRAME Input Duty Cycle Distortion	dcd	tbd		%
Optical Data, FRAME Input Rise/Fall Time[5]	t_R, t_F		400	ps
Optical Data, FRAME Input Extinction Ratio	ER	5.0		dB
Input Center Wavelength	λ_C	820	860	nm

Notes

Voltages refer to $V_{EE}=0$ V.

1. Noise frequency is 1 kHz to 1 MHz. Voltage is peak-to-peak value.
2. Noise frequency is 1 MHz to 1 GHz. Voltage is peak-to-peak value.
3. Measured between 0.8 V and 2.0 V.
4. Between all data and frame optical inputs.
5. 20%–80% level.

Receiver Electro-Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Current	I_{CC}		910	1030	mA
Power Consumption	P			3.0	3.7	W
LVDS Output Low Voltage[1, 4]	V_{LVDSOL}	925			mV
LVDS Output High Voltage[1, 4]	V_{LVDSOH}			1475	
LVDS Output Differential Voltage[1, 2, 4]	$|V_{OD}|$	250		400	
LVDS Output Offset Voltage[1, 3, 4]	V_{OS}	1125		1275	mV
Clock Output Rise and Fall Time[5]	t_R, t_F			400	ps
LVCMOS Output Voltage Low	$V_{LVCMOSOL}$			400	mV
LVCMOS Output Voltage High	$V_{LVCMOSOH}$	2500			
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	−500		500	µA
LVCMOS Output Current High[6]	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output Current Low[7]	$I_{LVCMOSOL}$			4.0	
Data Rate per channel (output)	D_R	200		500	Mbit/s
Clock Frequency SCI Mode	f_{CLOCK}	100		250	MHz
Clock Frequency Strobe Mode	f_{CLOCK}	200		500	MHz

Notes
1. Level Diagram:
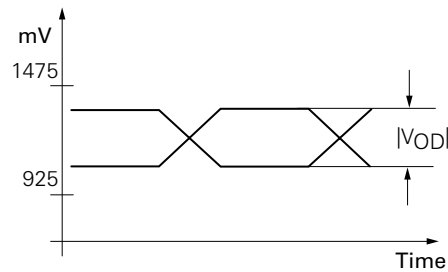
2. $|V_{OD}|=|$(output voltage of non-inverted output minus output voltage of inverted output)$|$.
3. $V_{OS}=1/2$ (output voltage of inverted output + output voltage of non-inverted output).
4. LVDS output must be differentially terminated with R_t.
5. With a maximum capacity load of 5 pF. See Measurement Conventions (Figure 6).
6. Source current.
7. Sink current

.

Parameter	Symbol	Min.	Max.	Units
Sensitivity (Average Power)[1]	P_{IN}		−18.0	dBm
Saturation (Average Power)	P_{SAT}	−8.0		
FRAME Detect Assert Level[2]	P_{FDA}		−19.0	
FRAME Detect Deassert Level[2]	P_{FDD}	−26.0		
FRAME Detect Hysteresis[2]	$P_{FDA}-P_{FDD}$	1.0	4.0	dB
Return Loss of Receiver	A_{RL}	12		

Notes

Optical parameters valid for each channel.

1. BER=10^{-12} at infinite ER.

2. P_{FDA}: Average optical power when FRAME_DET switches from Low to High.

   P_{FDD}: Average optical power when FRAME_DET switches from High to Low.

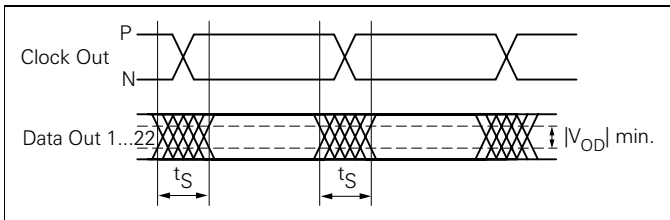   Values are also applicable for SD11 function, except SD11 is low active.

Figure 5. Timing diagram

Strobe Mode
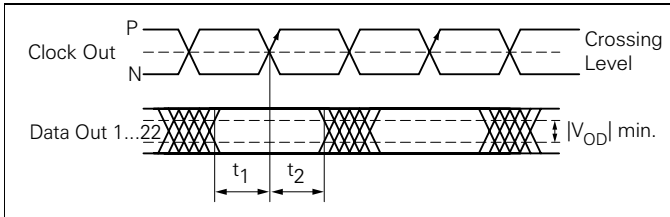
Parameter	Symbol	Min.	Typ.	Max.	Units
Output Setup Time	t_1	625			ps
Output Hold Time	t_2				

SCI Mode

In this operation mode the clock output is supplied in phase to data outputs.

Parameter	Symbol	Min.	Typ.	Max.	Units
Output Skew[1]	t_S			810	ps

Note

1. All data outputs and clock output.

FRAME_DET and -RESET Timing Diagrams
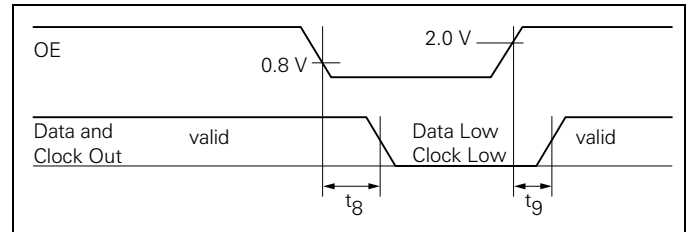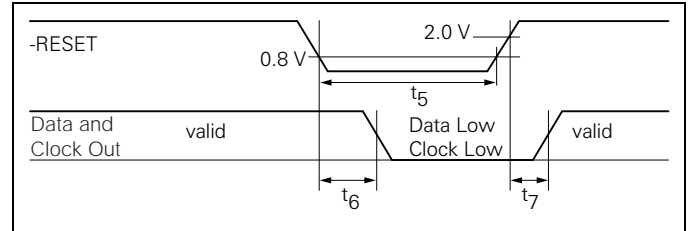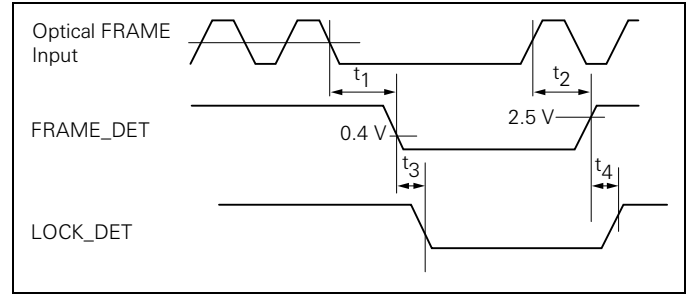
Parameter	Symbol	Min.	Max.	Units
FRAME_DET Deassert time[1]	t_1		10	µs
FRAME_DET Assert Time[1]	t_2			
FRAME_DET Low to LOCK_DET Low Delay	t_3		20	ns
FRAME_DET High to LOCK_DET High Duration[2]	t_4		tbd	
-RESET Low Duration[3]	t_5	tbd		ms
-RESET Off Delay Time	t_6		20	ns
-RESET On Delay Time[4]	t_7		tbd	ms
LVDS Output Disable Time	t_8		20	ns
LVDS Output Enable Time	t_9		20	

Notes

1. Timing also applicable for SD11 function on fiber #12.

2. Stable frame input required. -RESET not activated.

3. Except when used as power-on reset. At any failure recovery, -RESET should be brought to low level for at least t_3.

4. Valid if -RESET is set high when V_{CC} exceeds 3.0 V level and optical FRAME (FRAME_DET=high) and data input is valid. t_5 starts when all these conditions are fulfilled. -RESET must be set to Low during power-up.
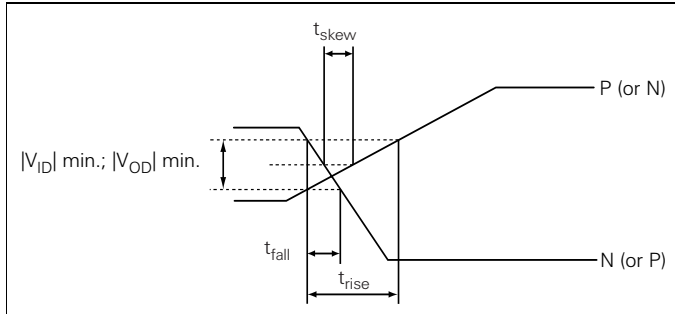
Figure 6. Measurement conventions for LVDS signals
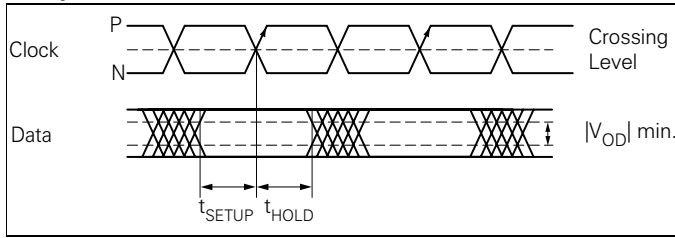
Setup and Hold Times

Setup and hold times are measured between the crosspoint of positive and negative clock and the points where rising and falling data edge cross the borders of the V-range.

Rise and Fall Times / Skew

Receiver Pin Description

Pin#	Pin Name	Level/Logic	Description
1	V_{EE}		Ground
2	V_{CC1}		Power supply voltage of preamplifier
3	V_{CC2}		Power supply voltage of analog circuitry
4	t.b.l.o.		to be left open
5	-RESET	LVCMOS in low active	High=receiver is active. Low=internal logic is reset and LVDS outputs are set to low. Internal pull- up pulls to high level when this input is left open.
6	FRAME_DET	LVCMOS Out	High=FRAME input signal present (on fiber #1) Low=insufficient FRAME signal
7	V_{CC3}		Power supply voltage of digital circuitry
8	V_{EE}		Ground
9	V_{CC4}		Power supply voltage of decoder
10	LOCK_DET	LVCMOS Out	High=PLL has successfully locked onto incoming FRAME signal. LOCK_DET being low sets all LVDS data outputs to low; clock output is unaffected by LOCK_DET.
11	COP	LVDS Out	Clock Output, non-inverted
12	CON	LVDS Out	Clock Output, inverted
13	DO01P	LVDS Out	Data Output #1, non-inverted
14	DO01N	LVDS Out	Data Output #1, inverted
15	DO12P	LVDS Out	Data Output #12, non-inverted

Pin#	Pin Name	Level/Logic	Description
16	DO12N	LVDS Out	Data Output #12, inverted
17	DO02P	LVDS Out	Data Output #2, non-inverted
18	DO02N	LVDS Out	Data Output #2,inverted
19	DO13P	LVDS Out	Data Output #13, non-inverted
20	DO13N	LVDS Out	Data Output #13, inverted
21	DO03P	LVDS Out	Data Output #3, non-inverted
22	DO03N	LVDS Out	Data Output #3, inverted
23	DO14P	LVDS Out	Data Output #14, non-inverted
24	DO14N	LVDS Out	Data Output #14, inverted
25	V_{CC4}		Power supply voltage of decoder
26	DO04P	LVDS Out	Data Output #4, non-inverted
27	DO04N	LVDS Out	Data Output #4, inverted
28	V_{EE}		Ground
29	DO15P	LVDS Out	Data Output #15, non-inverted
30	DO15N	LVDS Out	Data Output #15, inverted
31	DO05P	LVDS Out	Data Output #5, non-inverted
32	DO05N	LVDS Out	Data Output #5, inverted
33	DO16P	LVDS Out	Data Output #16, non-inverted
34	DO16N	LVDS Out	Data Output #16, inverted
35	DO06P	LVDS Out	Data Output #6, non-inverted
36	DO06N	LVDS Out	Data Output #6, inverted
37	DO17P	LVDS Out	Data Output #17, non-inverted
38	DO17N	LVDS Out	Data Output #17, inverted
39	DO07P	LVDS Out	Data Output #7, non-inverted
40	DO07N	LVDS Out	Data Output #7, inverted
41	DO18P	LVDS Out	Data Output #18, non-inverted
42	DO18N	LVDS Out	Data Output #18, inverted
43	DO08P	LVDS Out	Data Output #8, non-inverted
44	DO08N	LVDS Out	Data Output #8, inverted
45	V_{EE}		Ground
46	DO19P	LVDS Out	Data Output #19, non-inverted
47	DO19N	LVDS Out	Data Output #19, inverted
48	V_{CC4}		Power supply voltage of decoder
49	DO09P	LVDS Out	Data Output #9, non-inverted
50	DO09N	LVDS Out	Data Output #9, inverted
51	DO20P	LVDS Out	Data Output #20, non-inverted
52	DO20N	LVDS Out	Data Output #20, inverted
53	DO10P	LVDS Out	Data Output #10, non-inverted
54	DO10N	LVDS Out	Data Output #10, inverted
55	DO21P	LVDS Out	Data Output #21, non-inverted
56	DO21N	LVDS Out	Data Output #21, inverted
57	DO11P	LVDS Out	Data Output #11, non-inverted
58	DO11N	LVDS Out	Data Output #11, inverted
59	DO22P	LVDS Out	Data Output #22, non-inverted
60	DO22N	LVDS Out	Data Output #22, inverted

Pin#	Pin Name	Level/Logic	Description
61	CLK_SEL	LVCMOS In	Input Clocking Mode Select High=strobe mode Low=SCI mode This input has an internal pull-up resistor. When left open, strobe mode is active.
62	OE	LVCMOS In	High=enable LVDS outputs Low=set LVDS outputs (data and clock) to static low level. Internal pull-up pulls to high level when input is left open
63	t.b.l.o.		to be left open
64	V_{CC4}		Power supply voltage of decoder
65	V_{EE}		Ground
66	V_{CC3}		Power supply voltage of digital circuitry
67	-SD11	LVCMOS Out low active	Signal Detect Optical Data Channel 11 (on fiber #12) Low=signal of sufficient AC power is present on fiber # 12 High=signal on fiber # 12 is insufficient
68	ENSD	LVCMOS In	High=SD11 and FRAME_DET function enabled. Low=FRAME_DET and SD11 is set to permanent active. PLL is then forced to start lock-on procedure (for test purposes). Internal pull-up pulls to high level when input is left open.
69	t.b.l.o.		to be left open
70	V_{CC2}		Power supply voltage of analog circuitry
71	V_{CC1}		Power supply voltage of preamplifier
72	V_{EE}		Ground

Optical Port

- Designed for Siemens Simplex MT Connector (SMC)
- Port outside dimensions: 15.4 mm x 6.8 mm (width x height)
- MT compatible fiber spacing (250 µm) and alignment pin spacing (4600 µm)
- Alignment pins fixed in module port
- Integrated mechanical keying
- Process plug (SMC dimensions) included with every module
- Cleaning of port and connector interfaces necessary prior to mating

Features of Siemens Simplex MT Connector (SMC)

(as part of optional PAROLI fiber optic cables)
- Uses standardized MT ferrule
- MT compatible fiber spacing (250 µm) and alignment pin spacing (4600 µm)
- Snap-in mechanism
- Ferrule bearing spring loaded
- Not strain-relieved
- Integrated mechanical keying

Cleaning and Soldering Process for Transmitter and Receiver

Special care must be taken to remove residuals from the soldering and washing process, which can impact the mechanical function. Avoid the use of aggressive organic solvents like ketones, ethers, etc. Consult the supplier of the PAROLI modules and the supplier of the solder paste and flux for recommended cleaning solvents.

The following common cleaning solvents will not affect the module: deionized water, ethanol, and isopropyl alcohol. Air-drying is recommended to a maximum temperature of 100°C. Do not use ultrasonics.

During soldering, heat must be applied to the leads only, to ensure that the case temperature never exceeds 100°C. The module must be mounted with a hot-bar soldering process using a SnPb solder type, e.g.. S-Sn63Pb37E, in accordance with ISO 9435.
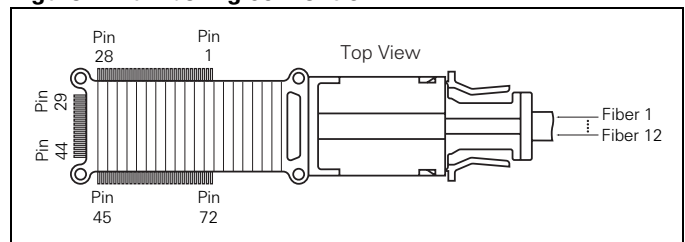
Figure 7. Numbering convention
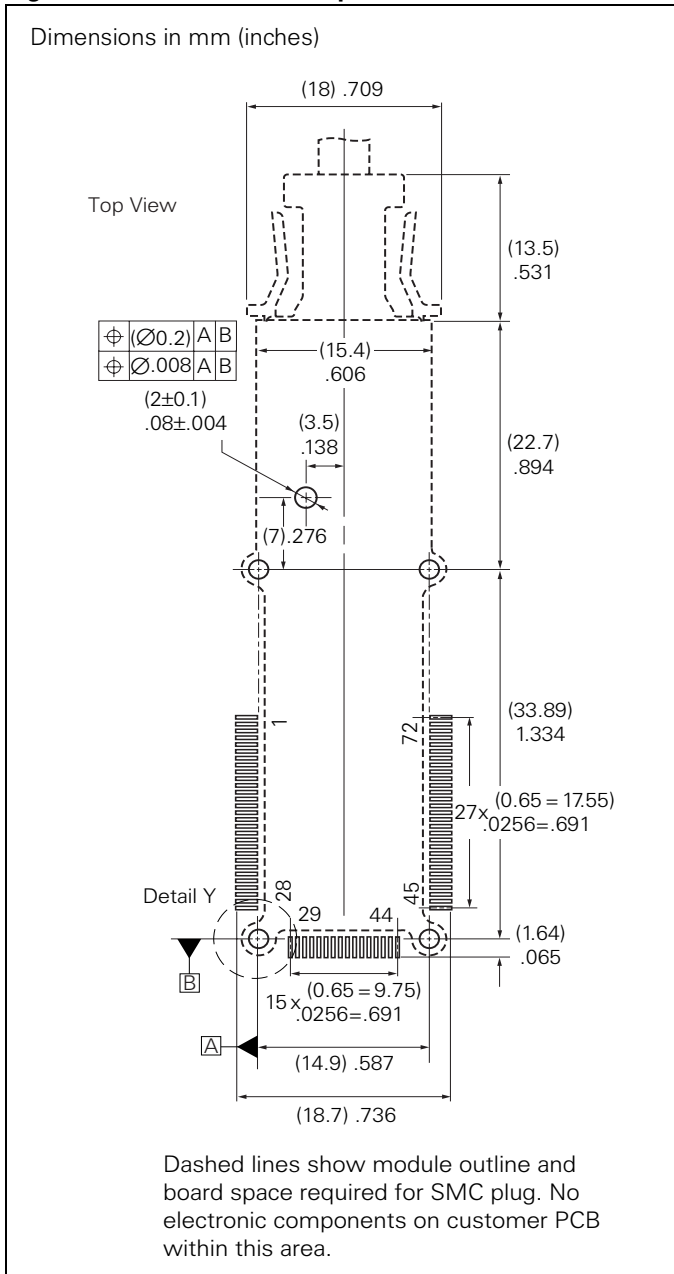
Figure 8. Recommended footprint: receiver

Dimensions in mm (inches)

Top View

Dashed lines show module outline and board space required for SMC plug. No electronic components on customer PCB within this area.

Figure 9. Recommended footprint: transmitter

Dimensions in mm (inches)

Top View

Dashed lines show module outline and board space required for SMC plug. No electronic components on customer PCB within this area.
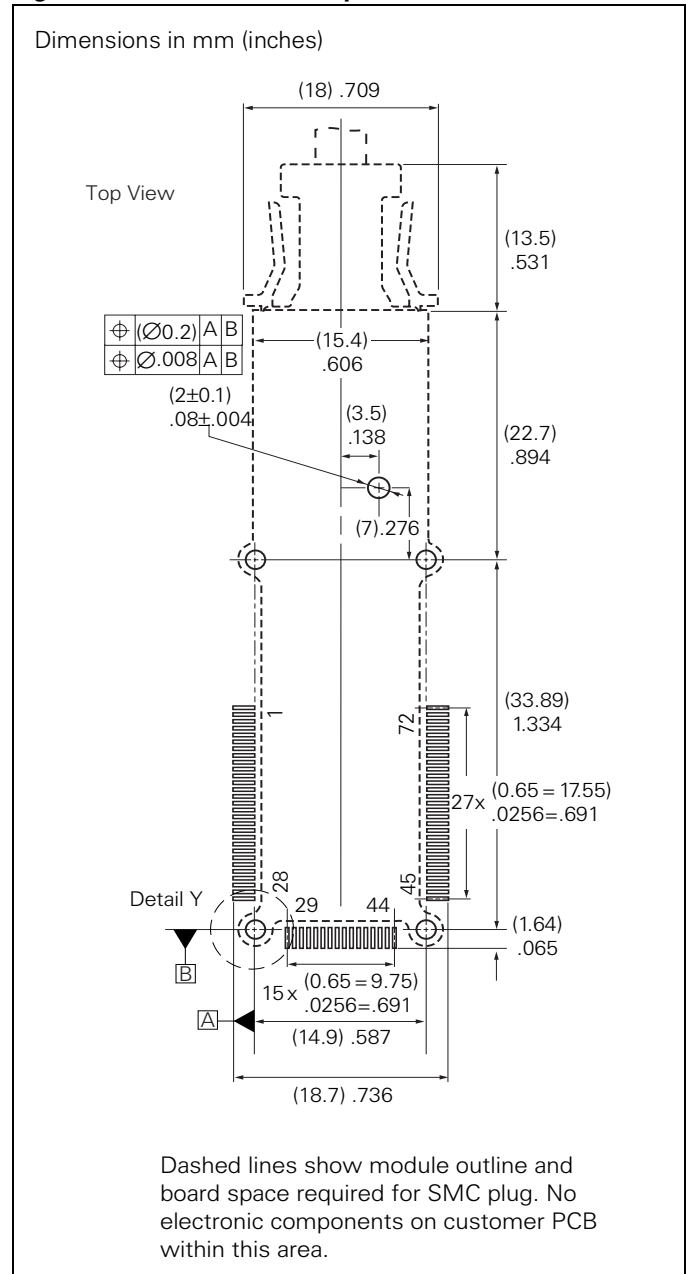
Figure 10. Mounting hole, Detail Y

dashed lines show module outlines

Figure 11. Applications

Board-to-Board

Backplane

Point-to-Point