HD404019/HD4074019 T-49-19-04

—Preliminary—

Description

The HD404019, HD4074019 are CMOS 4-bit single-chip microcomputers in the HMCS400 series. Each device incorporates ROM, RAM, I/O, serial interface, and 2 timer/counters and contains high-voltage I/O pins, including high-current output pins to drive fluorescent displays directly.

Features

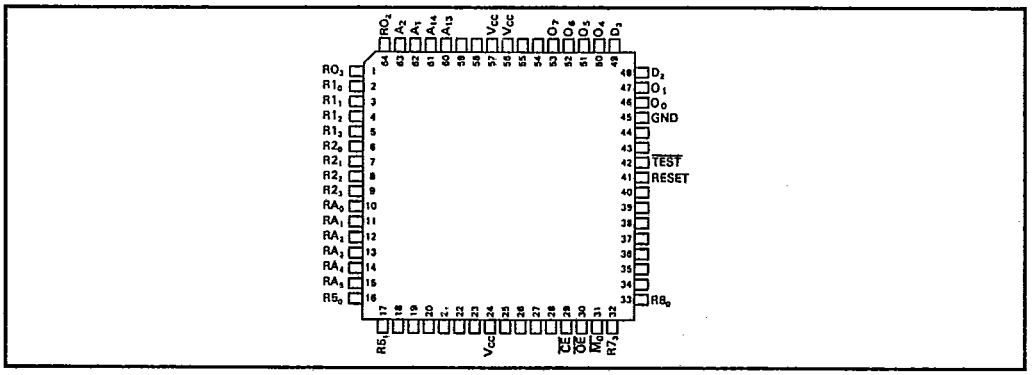
- 4-bit architecture
- 16384 words of 10-bit ROM
  - —Mask ROM: HD404019
  - —PROM: HD4074019
- 992 digits of 4-bit RAM
- 58 I/O pins, including 26 high-voltage I/O pins (40 V max)
- 2 timer/counters
  - —11-bit prescaler
  - —8-bit free running timer/counter
  - —8-bit auto-reload timer/event counter
- Clock synchronous 8-bit serial interface
- Five interrupt sources
  - —External: 2
  - —Timer/counter: 2
  - —Serial interface: 1
- Subroutine stack
  - —Up to 16 levels including interrupts
- Minimum instruction execution time
  - —0.89 μs
- Low power dissipation modes
  - —Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
  - —Stop: Stops instruction execution and clock oscillation while retaining RAM data
- On-chip oscillator
  - —Crystal or ceramic filter
  - —External clock
- Packages
  - —64-pin shrink type plastic DIP
  - —64-pin flat plastic package
  - —64-pin shrink type ceramic DIP with window
- Instruction set compatible with HMCS408: 101 instructions
- High programming efficiency with 10-bit/word ROM: 79 single-word instructions
- Direct branch to all RAM areas
- Direct or indirect addressing of all RAM areas
- Subroutine nesting up to 16 levels including interrupts
- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation-table lookup capability
- Bit manipulation for both RAM and I/O

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device

Ordering Information

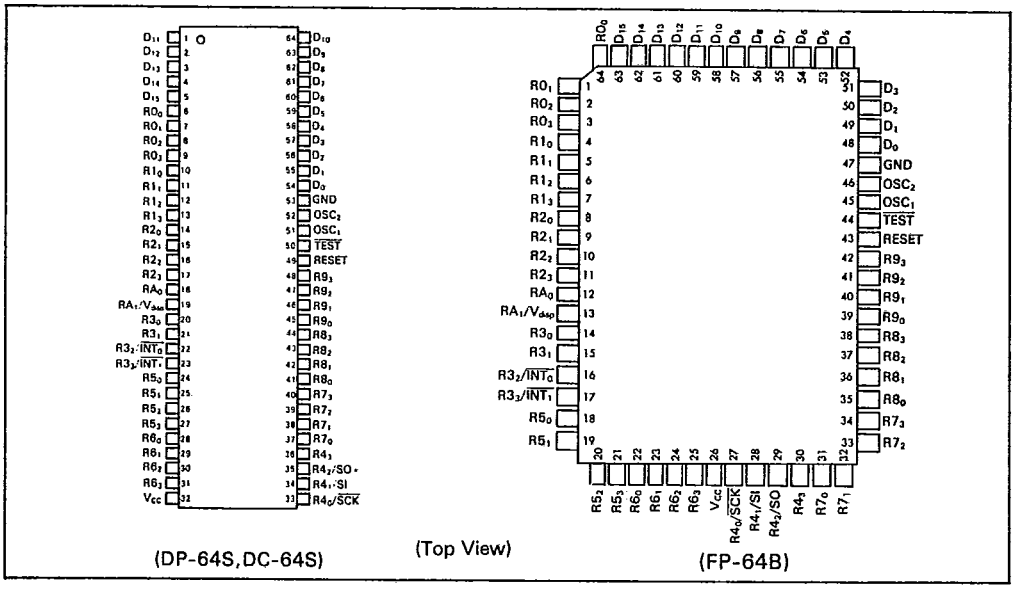
	Part No.	Package
Mask ROM type	HD404019S	DP-64S
	HD404019F	FP-64B
	HD404019H	FP-64A
ZTAT type	HD4074019S	DP-64S
	HD4074019F	FP-64B
	HD4074019C	DC-64S
	HD4074019H	FD-64A



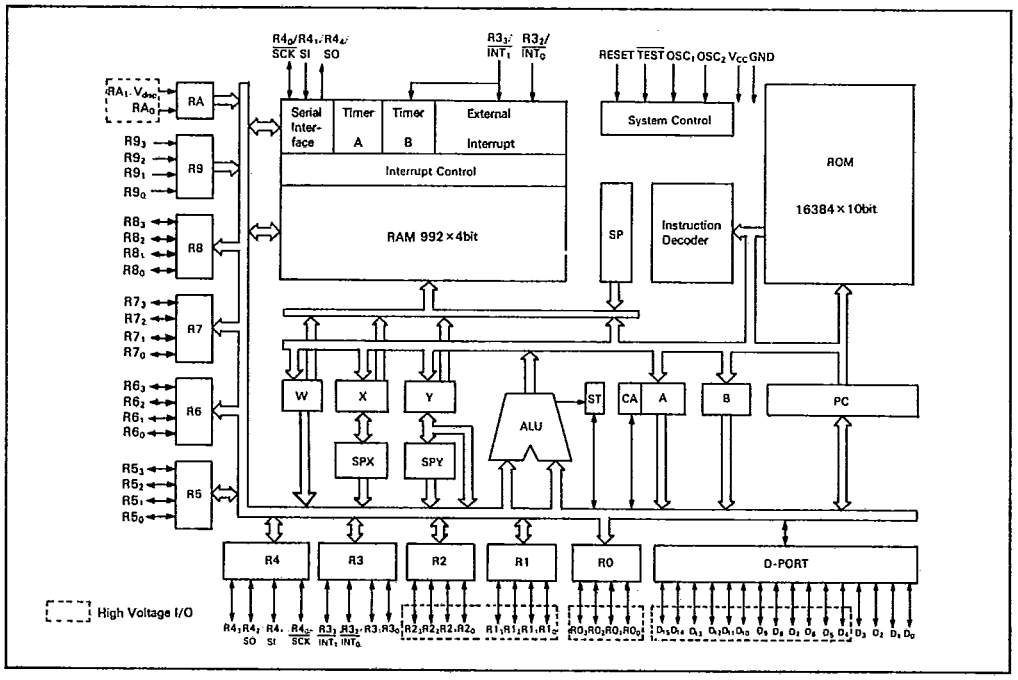
FP-64A

Pin Arrangement

T-49-19-04



Block Diagram



Differences between PROM in Package, EPROM on Package and Mask ROM Types

Item		PROM in Package ZTAT HD4074019			PROM in Package ZTAT HD4074008			EPROM on Package HD614PO80S HD614PO160S	Mask ROM HD404019	Mask ROM HMCS408AC/C/CL			Mask ROM HMCS404AC/C/CL			Mask ROM HMCS402AC/C/CL		
Typical instruction execution time		1 μs			1 μs			1.33 μs	1 μs	1 μs	2 μs	4 μs	1 μs	2 μs	4 μs	1 μs	2 μs	4 μs
Power supply voltage (V)		4.5–5.5			4.5–5.5			4.5–5.5	3.5–6	4.5–6	3.5–6	2.5–6	4.5–6	4–6	2.7–6	4.5–6	4–6	2.7–6
ROM		16,384 words × 10 bit			8,192 words × 10 bit			HN27C64: 4,096 × 10 bit HN4827128: 8,192 × 10 bit HN27C256: 16,384 × 10 bit	16,384 words × 10 bit	8,192 words × 10 bit			4,096 words × 10 bit			2,048 words × 10 bit		
RAM		992 × 4 bit			512 × 4 bit			576 × 4 bit	992 × 4 bit	512 × 4 bit			256 × 4 bit			160 × 4 bit		
I/O pin circuit	Standard pins	NMOS open dain			NMOS open drain			NMOS open drain	Each pin can be without pull-up MOS (NMOS open drain), with pull-up MOS, or CMOS									
	High voltage pins	PMOS open drain			PMOS open drain (Typical 5 V use)			PMOS open drain	Each pin can be without pull-down MOS (PMOS open drain) or with pull-down MOS									
Clock generation	Crystal	○			○			○	○	○			○			○		
	Ceramic	○			○			○	○	○			○			○		
	Resistance	—			—			—	—	—			HMCS404C			HMCS402C		
Pakage	Type	DC-64S (Window)	DP-64S FP-64A	FP-64B	DC-64S (Window)	DP-64S	FP-64 FP-64A	DC-64SP	DP-64S	FP-64B FP-64A	DP-64S	FP-64	DP-64S	FP-64		DP-64S	FP-64	
	Occupied area (mm²)	18.8× 57.3	17×58	18.8× 24.8	18.8× 57.3	17×58	19.6× 25.6 17.2×17.2	23× 57.3	17×58	18.8× 24.8	17×58	19.6× 25.6	17×58	19.6× 25.6		17×58	19.6× 25.6	
	Height from stand off (mm)	5.6 (Max)	5.1 (Max)	2.9 (Max)	5.6 (Max)	5.1 (Max)	2.9 (Max) 2.9 (Max)	7.5 (Max)	5.1 (Max)	2,9 (Max)	5.1 (Max)	2.9 (Max)	5.1 (Max)	2.9 (Max)		5.1 (Max)	2.9 (Max)	

Notes:
DC-64S: 64-pin shrink type ceramic DIP with window
DP-64S: 64-pin shrink type DIP
FP-64: 64-pin flat plastic package (rectangular shape)
FP-64A: 64-pin flat plastic package (square shape)
FP-64B: 64-pin flat plastic package (rectangular shape)
DC-64SP: 64-pin shrink type ceramic piggy back
○: Available
—: Not available

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Pin Description

GND, V_{CC}, V_{disp} (Power)

GND, V_{CC}, and V_{disp} are the power supply pins for the MCU.
Connect GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA_1) is a power supply for high-voltage I/O pins with maximum voltage of 40 V (V_{CC} − 40 V). For details, see Input/Output section.

$\overline{TEST}$ (Test)

$\overline{TEST}$ is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC_1, OSC_2 (Oscillator Connections)

OSC_1 and OSC_2 are input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D_0−D_{15} (D Port)

The D port is an input/output port addressed by the bit. These 16 pins are all input/output pins. D_0 to D_3 are standard and D_4 to D_{15} are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

$R0_0$−$R0_3$, $R1_0$−$R1_3$, $R2_0$−$R2_3$, $R3_0$−$R3_3$, $R4_0$−$R4_3$, $R5_0$−$R5_3$, $R6_0$−$R6_3$, $R7_0$−$R7_3$, $R8_0$−$R8_3$, $R9_0$−$R9_3$, RA_0, RA_1 (R Ports)

R0 to R9 are 4-bit I/O ports. RA is a 2-bit port. R9 and RA are input ports, and R0 to R8 I/O ports. R0, R1, R2, and RA are high-voltage ports, and R3 to R9 are standard ports. Each pin has a mask option which selects its circuit type. The pins $R3_2$, $R3_3$, $R4_0$, $R4_1$, and $R4_2$ are multiplexed with $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI, and SO respectively. For details, see Input/Output section.

$\overline{INT_0}$, $\overline{INT_1}$ (Interrupts)

$\overline{INT_0}$ and $\overline{INT_1}$ are external interrupts for the MCU. $\overline{INT_1}$ can be used as an external event input pin for timer B. $\overline{INT_0}$ and $\overline{INT_1}$ are multiplexed with $R3_2$ and $R3_3$ respectively. For details, see Interrupt section.

$\overline{SCK}$, SI, SO

The transfer clock I/O pin ($\overline{SCK}$), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. $\overline{SCK}$, SI, and SO are multiplexed with $R4_0$, $R4_1$, and $R4_2$ respectively. For details, see Serial Interface Section.

Functional Description

ROM Memory Map

The MCU includes 16384 words × 10 bits of ROM (mask ROM or PROM). It is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area ($0000 to $000F): Locations $0000 through $000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F are reserved for subroutines. CAL instructions branch to subroutines.

Pattern Area ($0000 to $0FFF): Locations $0000 through $0FFF are reserved for ROM data. P instructions can refer to the ROM data as a pattern.

Program Area ($0000 to $3FFF): Locations from $0000 to $1FFF can be used for program code.

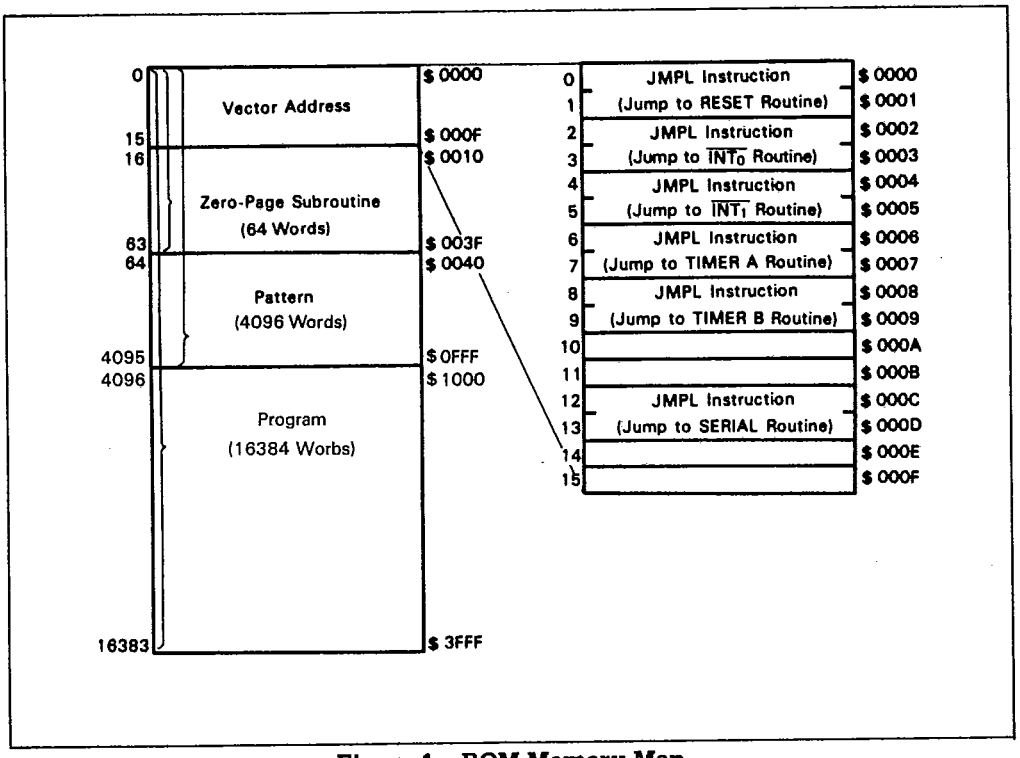

Figure 1. ROM Memory Map

RAM Memory Map

The MCU includes 992 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area ($000 to $003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessable only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

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Special Function Registers Area ($004 to $00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

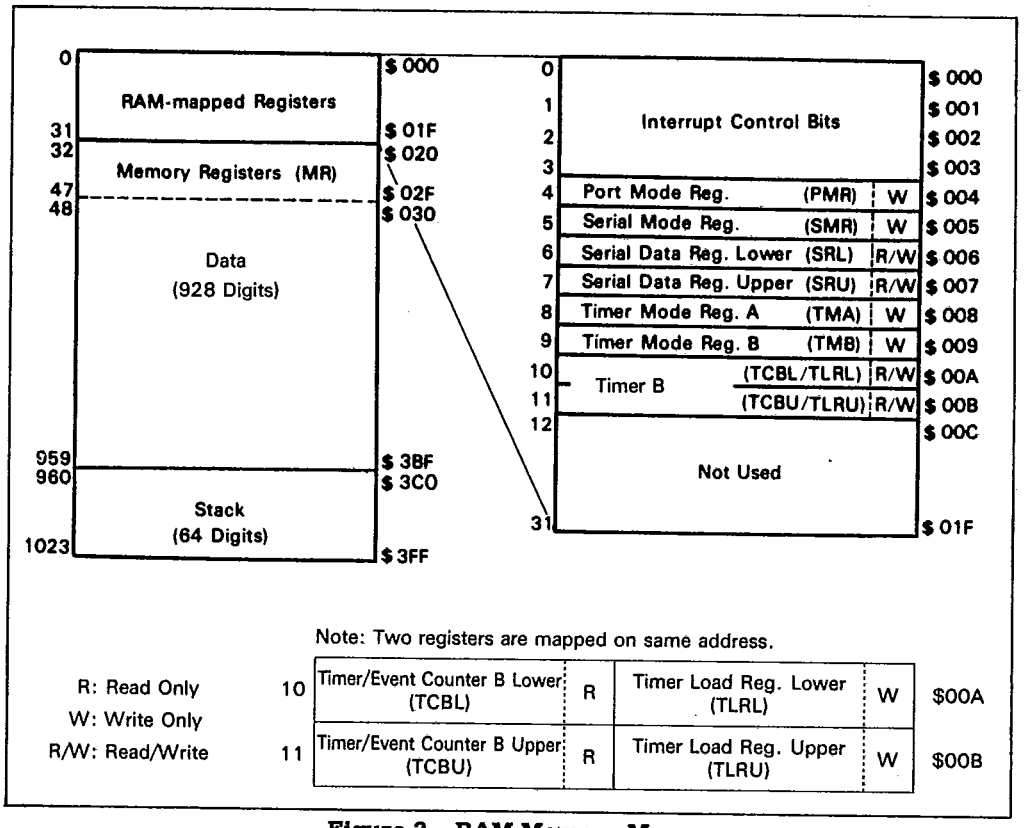


Figure 2. RAM Memory Map

Data Area ($020 to $3BF): 16 digits, $020 through $02F, of the data area are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST), and carry (CA) when subroutine calls (CAL instruction, CALL instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by the RTNI instruction. This area, when not used for a stack, is available as a data area.

	bit 3	bit 2	bit 1	bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	$000
1	IMTA (IM of TIMER A)	IFTA (IF of TIMER A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not Used	Not Used	IMTB (IM of TIMER B)	IFTB (IF of TIMER B)	$002
3	Not Used	Not Used	IMS (IM of SERIAL)	IFS (IF of SERIAL)	$003

IF: Interrupt Request Flag
IM: Interrupt Mask
I/E: Interrupt Enable Flag
SP: Stack Pointer
Note: Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, is reset by the REM/REMD instruction, and is tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore the interrupt request flag is not affected by the SEM/SEMD instruction.
The contents of status becomes invalid when a "Not Used" bit is tested.

Figure 3. Interrupt Control Bit Area Configuration

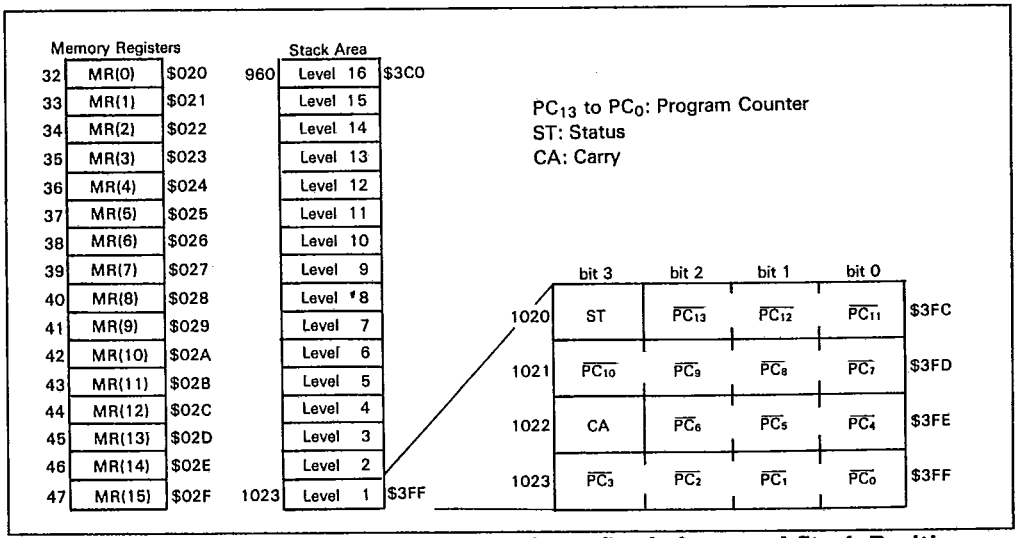


Figure 4. Configuration of Memory Register, Stack Area, and Stack Position

Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register, and the 4-bit X and Y registers indirectly address RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY assist X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL, and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value for the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after a BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack. It is restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) points to the address of the next stack area (up to 16 levels).

The stack pointer is initialized to RAM address $3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the high four bits of the stack pointer are fixed at 1111.

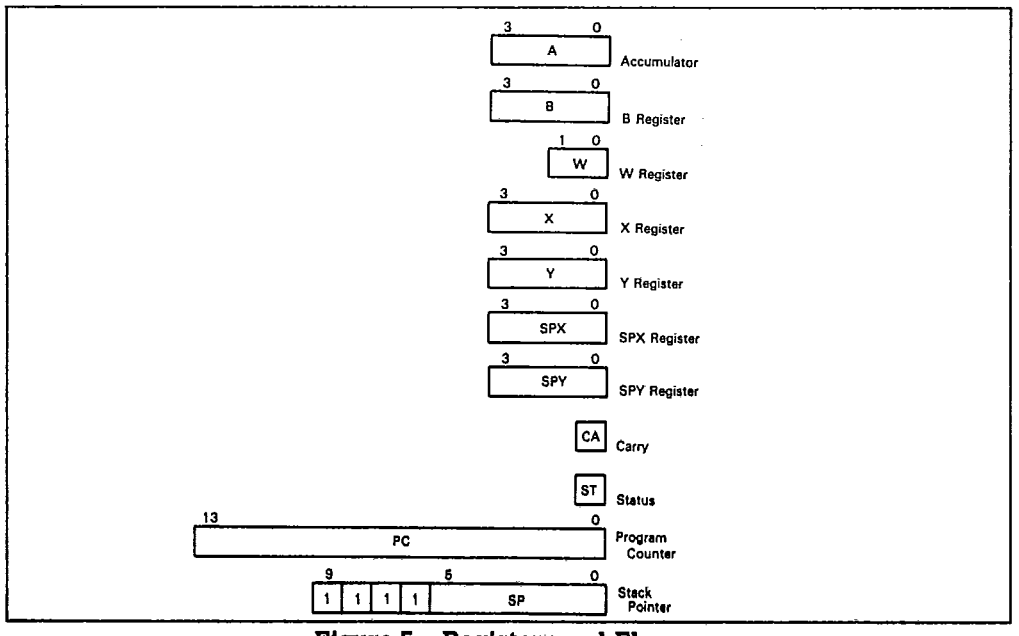


Figure 5. Registers and Flags

The stack pointer is initialized to $3FF by either MCU reset or the RSP bit, reset by a REM/REMD instruction.

Interrupt

Five interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$), timer/counter (timer A, timer B), and serial port (serial). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses control and maintain the interrupt request. The interrupt enable flag (IE) also controls interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on $000 through $003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

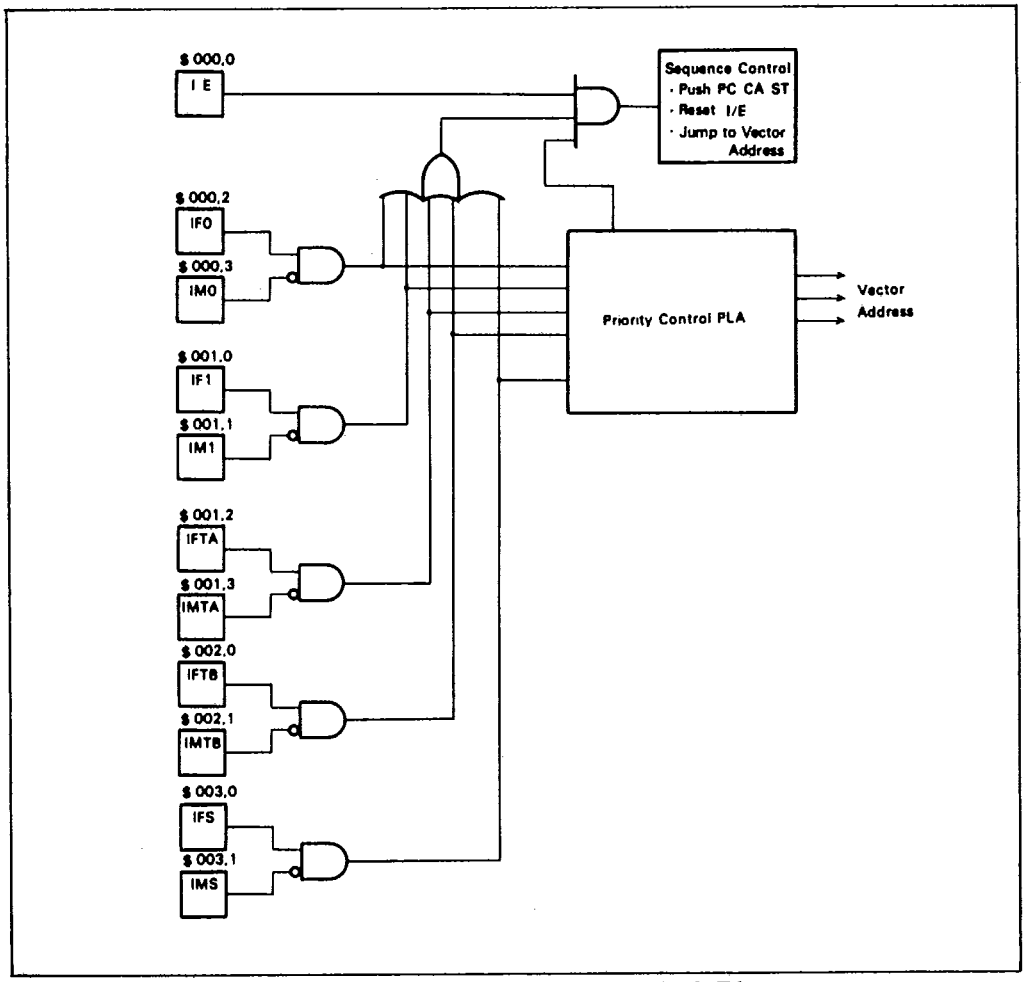


Figure 6. Interrupt Control Circuit Block Diagram

An interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

In each vector address, program JMPL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	–	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
SERIAL	5	$000C

Table 2. Conditions of Interrupt Service

Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	TimerA	TimerB	SERIAL
I/E	1	1	1	1	1
IF0·$\overline{IM0}$	1	0	0	0	0
IF1·$\overline{IM1}$	*	1	0	0	0
IFTA·$\overline{IMTA}$	*	*	1	0	0
IFTB·$\overline{IMTB}$	*	*	*	1	0
IFS·$\overline{IMS}$	*	*	*	*	1

Note: * Don't care

Interrupt Enable Flag (I/E: $000 Bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by the port mode register (PMR: $004). Setting bit 3 and bit 2 of PMR causes $R3_3/\overline{INT_1}$ pin and $R3_2/\overline{INT_0}$ pin to be used as $\overline{INT_1}$ pin and $\overline{INT_0}$ pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$ inputs. (Refer to table 4.)

The $\overline{INT_1}$ input can be used as a clock signal input to timer B. Then timer B counts up at each falling edge of the $\overline{INT_1}$ input. When $\overline{INT_1}$ is used as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted. (Refer to table 5.)

External Interrupt Request Flags (IF0: $000 Bit 2, IF1: $001 Bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$, and $\overline{INT_1}$ inputs respectively.

External Interrupt Masks (IM0: $000 Bit 3, IM1: $001 Bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: $004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT_0}$ pin, $R3_3/\overline{INT_1}$ pin, $R4_1$/SI pin, and $R4_2$/SO pin as shown in table 6. The port mode register will be initialized to $0 by MCU reset. These pins are therefore initially used as ports.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (mask)

Table 6. Port Mode Register

PMR3	$R3_3/\overline{INT_1}$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR2	$R3_2/\overline{INT_0}$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as $\overline{INT_0}$ input pin

PMR1	$R4_1$/SI Pin
0	Used as $R4_1$ port input/output pin
1	Used as SI input pin

PMR0	$R4_2$/SO Pin
0	Used as $R4_2$ port input/output pin
1	Used as SO output pin

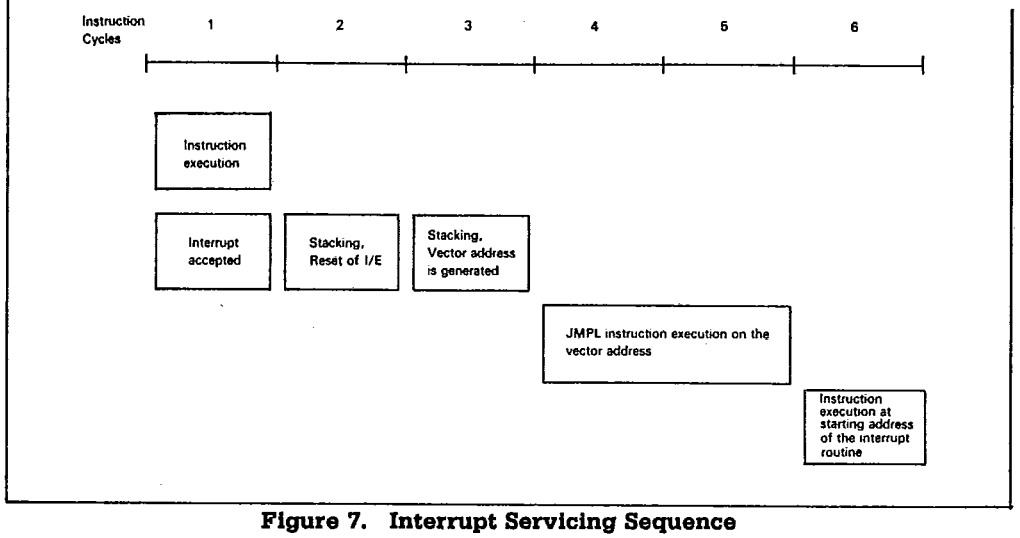


Figure 7. Interrupt Servicing Sequence

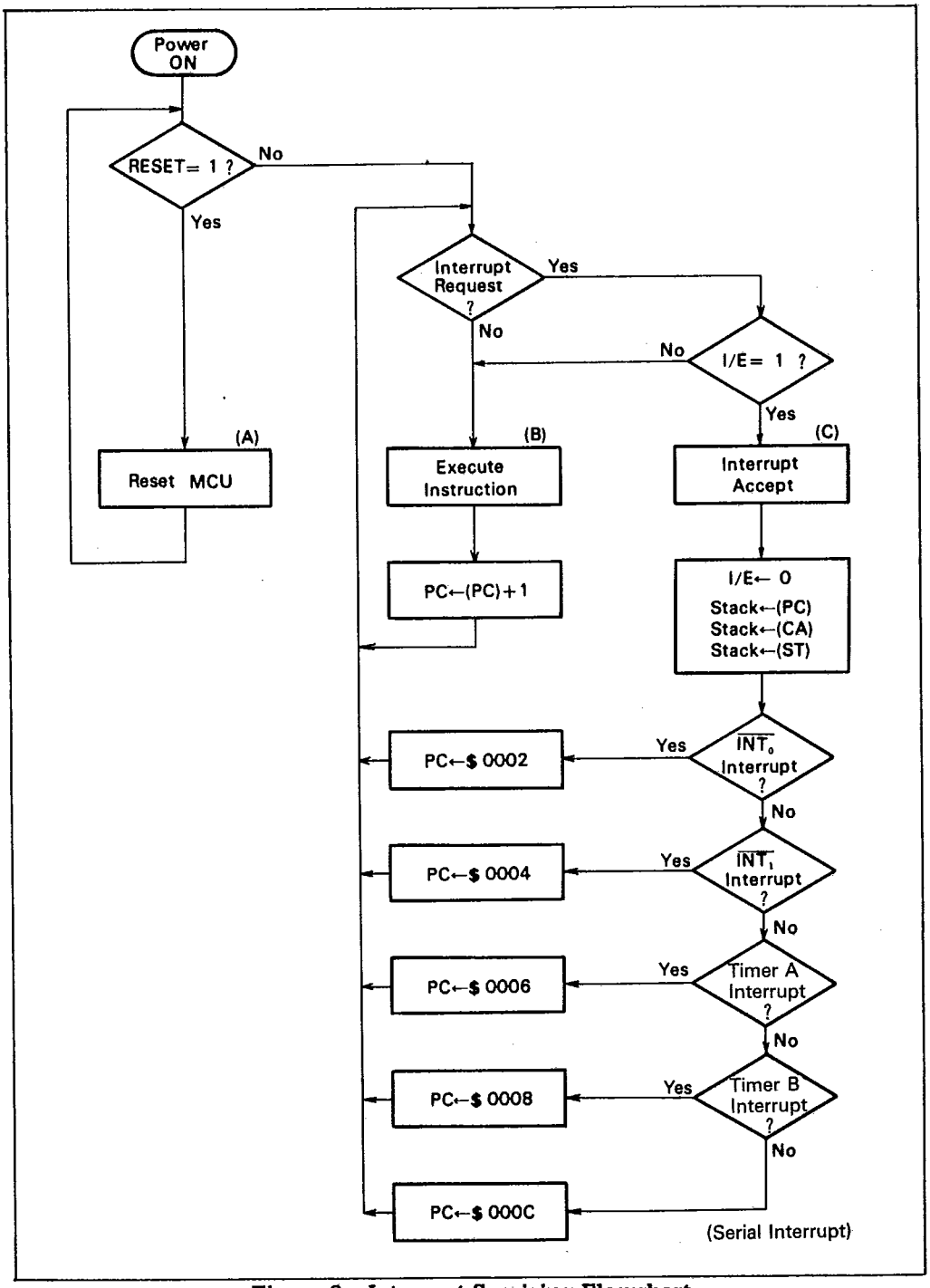


Figure 8. Interrupt Servicing Flowchart

Serial Interface

The serial interface is used to transmit/receive 8-bit data serially. It consists of the serial data register, the serial mode register, the octal counter, and the multiplexer as illustrated in figure 9. Pin $R4_0/\overline{SCK}$ and the transfer clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transfer clock signal.

STS instruction initiates serial interface operations and resets the octal counter to $0. The counter starts to count at the falling edge of the transfer clock ($\overline{SCK}$) signal and increments by one at the rising edge of $\overline{SCK}$. When the octal counter is reset to $0 after eight transfer clock signals, or when a transmit/receive operation is discontinued when the octal counter is reset, the serial interrupt request flag will be set.

Serial Mode Register (SMR: $005): The 4-bit write-only serial mode register controls the $R4_0/\overline{SCK}$, prescaler divide ratio, and transfer clock source as shown in table 7.

The write signal to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from accepting transfer clock, and it also resets the octal counter to $0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

Contents of the serial mode register will be changed on the second instruction cycle after the serial mode register has been written to. Therefore, the STS instruction must be executed after the data in the serial mode register has been changed completely. The serial mode register will be reset to $0 by MCU reset.

Serial Data Register (SRL: $006, SRU: $007): The 8-bit read/write serial data register consists of a low-order digit (SRL: $006) and a high-order digit (SRU: $007).

The data in the serial data register is output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transfer clock signal. At the same time, external data is input from the SI pin to the serial data register, MSB first, synchronously with the rising edge of the transfer clock. Figure 10 shows the I/O timing chart for the transfer clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data can not be guaranteed.

Serial Interrupt Request Flag (IFS: $003 Bit 0): The serial interrupt request flag will be set when the octal counter counts eight transfer clock signals, or when data transfer is discontinued by resetting the octal counter. Refer to table 8.

Serial Interrupt Mask (IMS: $003 Bit 1): The serial interrupt masks the interrupt request. Refer to table 9.

Selection and Change of the Operation Mode: Table 10 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and that in the serial mode register.

Initialize the serial interface by a write signal to the serial mode register when the operation mode is changed.

Table 7. Serial Mode Register

SMR3	$R4_0/\overline{SCK}$
0	Used as $R4_0$ port input/output pin
1	Used as $\overline{SCK}$ input/output pin

			Transfer Clock			
SMR 2	SMR 1	SMR 0	$R4_0/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ Output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ Output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ Output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ Output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ Output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ Output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ Output	System Clock	—	÷ 1
1	1	1	$\overline{SCK}$ Input	External Clock	—	—

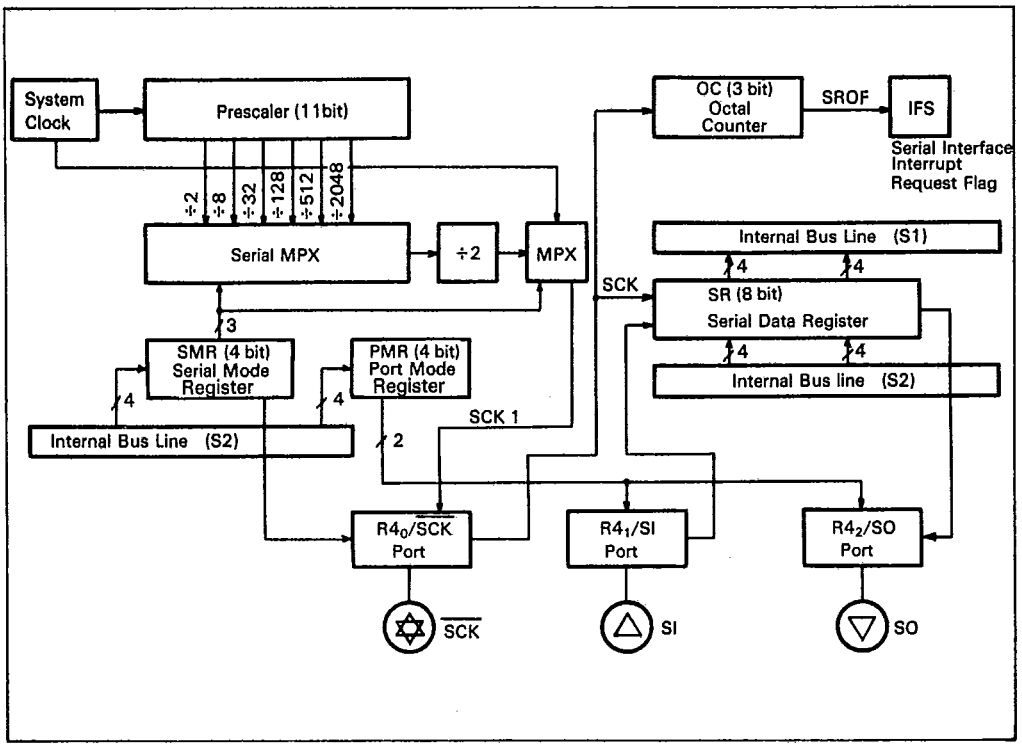


Figure 9. Serial Interface Block Diagram

Operating State of Serial Interface: The serial interface has three operating states, the STS waiting state, SCK waiting state, and transfer state, as shown in figure 11.

The STS waiting state is the initialization state of the serial interface internal state. The serial interface enters this state in one of two ways: either by the operation mode changing through a change in the data in the port mode register, or by data being written into the serial mode register. In this state, the serial interface does not operate even if the transfer clock is applied. If an STS instruction is executed, the serial interface shifts to SCK waiting state.

In this state the falling edge of the first transfer clock causes the serial interface shift to transfer state. While the octal counter counts up and the serial data register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in SCK waiting state while the transfer clock outputs continuously.

The octal counter becomes 000 again after 8 transfer clocks or execution of an STS instruction, so the serial interface returns to SCK waiting state and the serial interrupt request flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output triggered by the execution of an STS instruction, and it stops after 8 clocks.

Table 8. Serial Interrupt Request Flag

Serial Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Serial Interrupt Mask

Serial Interrupt Mask	Interrupt Request
0	Enable
1	Disable (mask)

Table 10. Serial Interface Operation Mode

SMR3	PMR1	PMR0	Serial Interface Operating Mode
1	0	0	Clock continuous output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

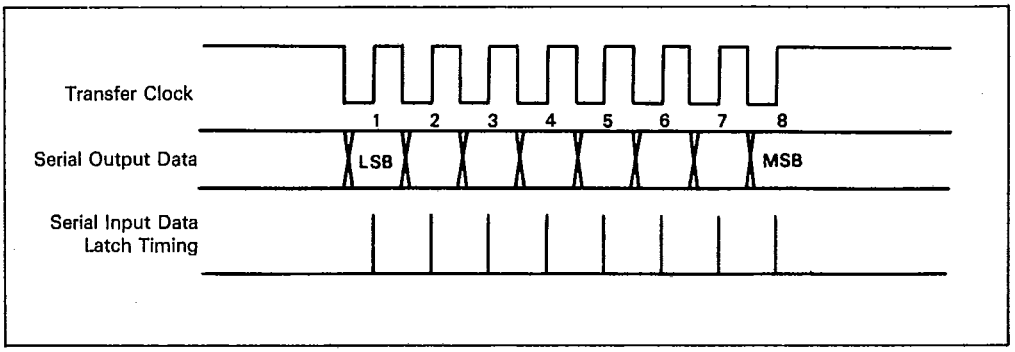


Figure 10. Serial Interface I/O Timing Chart

Transfer Clock Errors Detection Example: The serial interface functions abnormally when the transfer clock is disturbed by external noises. Transfer clock errors can be detected by the procedure shown in figure 12.

If more than 8 transfer clocks occur in the SCK waiting state, the state of the serial interface shifts as follows: first, transfer state, second, SCK waiting state and third, transfer state again. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure sets the serial IRF again.

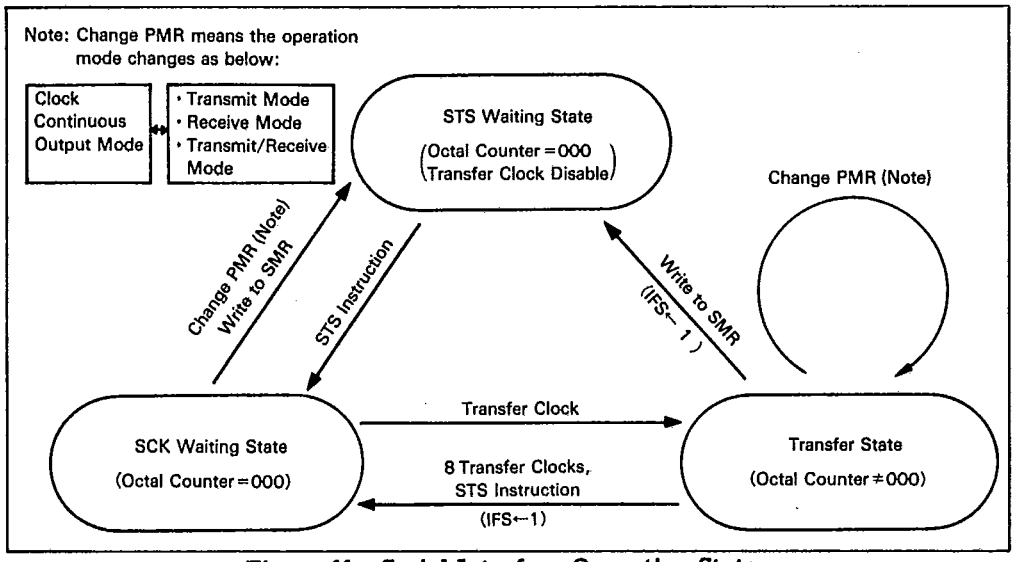


Figure 11. Serial Interface Operation State

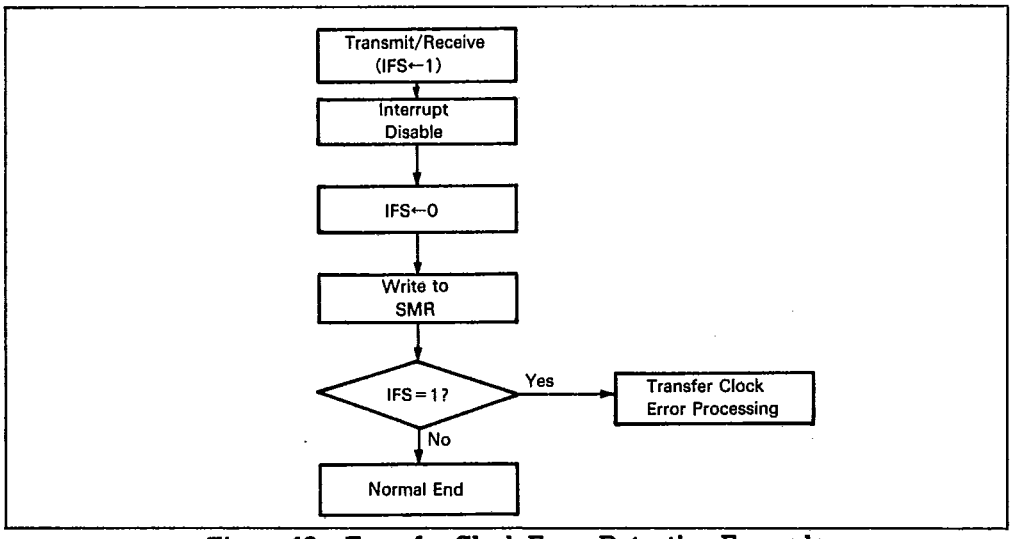


Figure 12. Transfer Clock Error Detection Example

Timer

The MCU contains a prescaler and two timer/counters (timer A, timer B). See figure 13. The prescaler is an 11-bit binary counter, timer A an 8-bit free-running timer/counter, and timer B an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is the system clock signal. The prescaler is initialized to $0000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface. The prescaler divide ratio is selected by timer mode register A (TMA), timer mode register B (TMB), or the serial mode register (SMR).

Timer A Operation: After timer A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A becomes $FF, it generates an overflow and becomes $00. This overflow causes the timer A interrupt request flag (IFTA: $001 bit 2) to go to 1. This timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to timer A are selected by timer mode register A (TMA: $008).

Timer B Operation: Timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio of timer B. When the external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT_1}$ as $\overline{INT_1}$ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to $FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load register. If it is not selected, timer B goes to $00. The timer B interrupt request flag (IFTB:

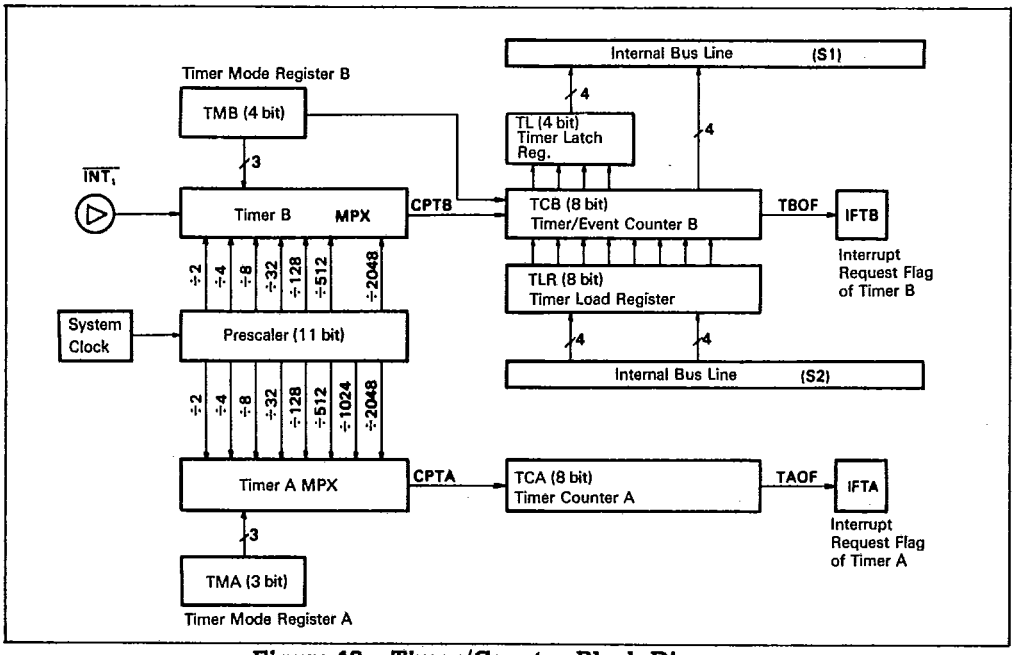


Figure 13. Timer/Counter Block Diagram

$002 bit 0) will be set at this overflow output.

Timer Mode Register A (TMA: $008): Timer mode register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of timer A clock input, as shown in table 11. The timer mode register A is initialized to $0 by MCU reset.

Timer Mode Register B (TMB: $009): Timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 12. The timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Timer B should be initialized by writing data into the timer load register after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 14.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer/event counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B). (Refer to figure 2.)

The timer/event counter can be initialized by writing data into the timer load register. Write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

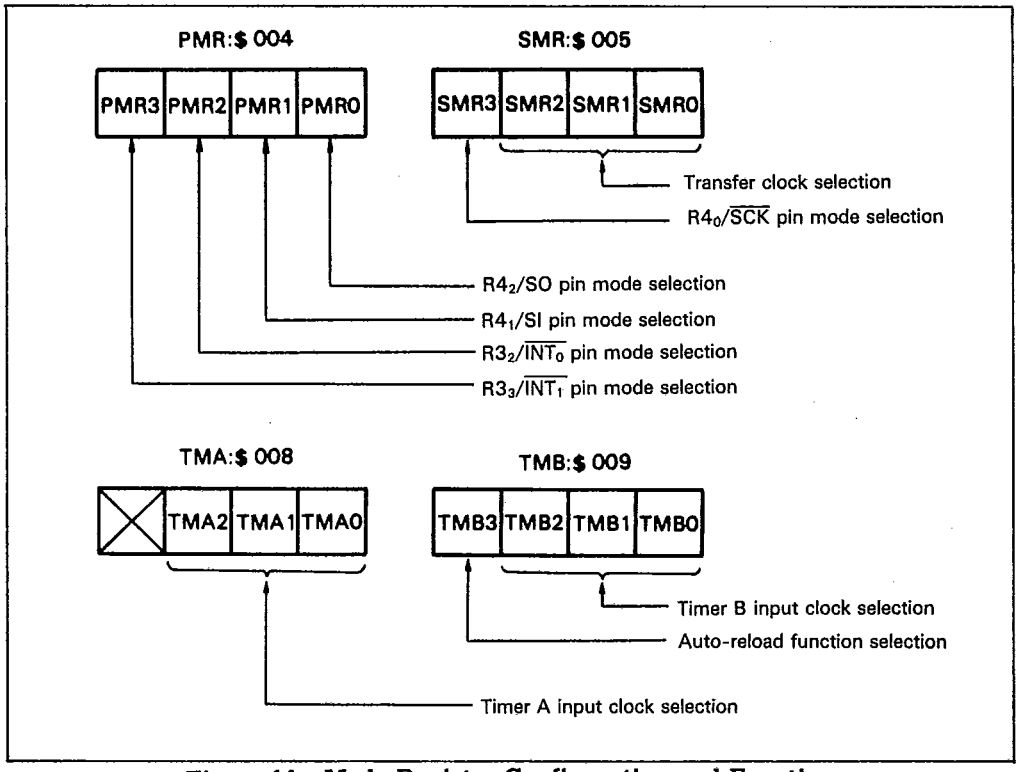


Figure 14. Mode Register Configuration and Function

Timer A Interrupt Request Flag (IFTA: $001 Bit 2): The timer A interrupt request flag is set by the overflow output of timer A (table 13).

Timer A Interrupt Mask (IMTA: $001 Bit 3): The timer A interrupt mask prevents an interrupt request from being generated by the timer A interrupt request flag (table 14).

Timer B Interrupt Request Flag (IFTB: $002 Bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 15).

Timer B Interrupt Mask (IMTB: $002 Bit 1): The timer B interrupt mask prevents an interrupt request from being generated by timer B Interrupt request flag (table 16).

Table 11. Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler Divide Ratio
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB3	Auto-reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (External Event Input)

Table 13. Timer A Interrupt Request Flag

Timer A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. Timer A Interrupt Mask

Timer A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Table 15. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No.
1	Yes

Table 16. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Input/Output

The MCU has 58 I/O pins, 32 standard and 26 high voltage. One of three circuit types can be selected by mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain); and one of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, V_{disp} must be selected for the RA_1/V_{disp} pin via mask option when with pull-down MOS option is selected for at least one high-voltage pin. See table 17 for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected in the manner specified in table 18.

Output Circuit Operation of Standard Pins With Pull-Up MOS: In the standard pin option with pull-up MOS, the circuit shown in figure 15 is used to shorten rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps the PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{HLT}$ signal becomes 0 in stop mode, MOS (A) (B) (C) turn off.

D Port: I/O port D has 16 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See tables 17 and 18 for the classification of standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The eleven R ports in the HD404019/HD4074019 are composed of 36 I/O pins, and 6 input-only pins. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read when the output-only and/or non-existing ports are read.

The $R3_2$, $R3_3$, $R4_0$, $R4_1$, and $R4_2$ pins are multiplexed with the $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI, and SO pins respectively. See tables 17 and 18 for the classification of standard pins, high-voltage pins and selectable circuit types of these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent the malfunction.

High-voltage pins: select without pull-down MOS (PMOS open drain) via mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select without pull-up MOS (NMOS open drain) via mask option and connect to GND on the printed circuit board.

$R4_0/\overline{SCK}$ and $R4_2$/SO should be used as $R4_0$ and $R4_2$ by serial mode register and port mode register respectively.

Table 17. I/O Pin Circuit Types

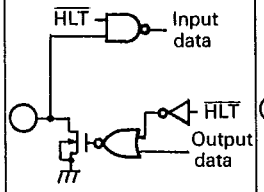
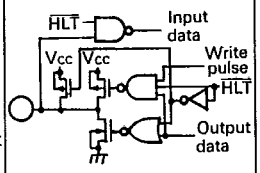
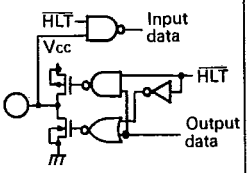
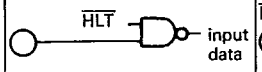
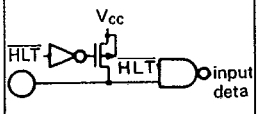
		Without Pull-Up MOS (NMOS Open Drain) (A)	With Pull-Up MOS (B)	CMOS (C)	Applicable Pins
Standard Pins	I/O Common Pins				D_0-D_3 $R3_0-R3_3$ $R4_0-R4_3$ $R5_0-R5_3$ $R6_0-R6_3$ $R7_0-R7_3$ $R8_0-R8_3$
	Input Pins				$R9_0-R9_3$

Table 17. I/O Pin Circuit Types (cont)

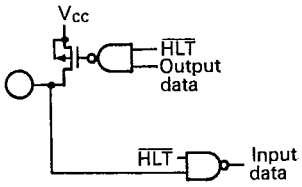
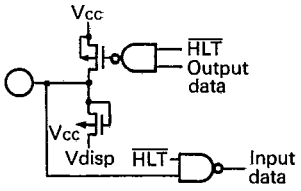
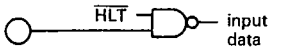
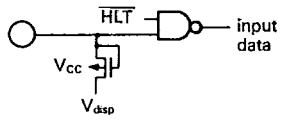
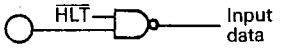
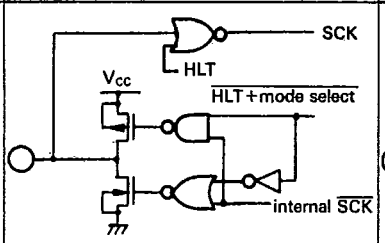
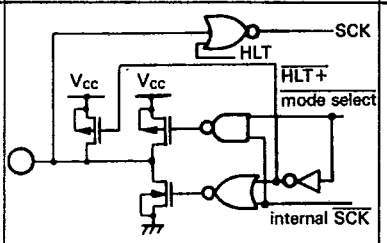
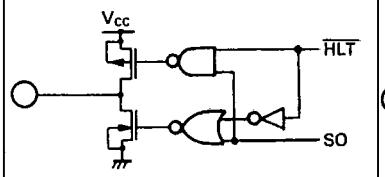
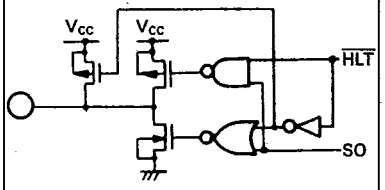
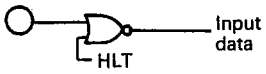
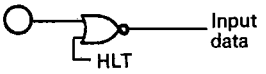
		Without Pull-Down MOS (PMOS Open Drain) (D)	With Pull-Down MOS (E)	Applicable Pins
High Voltage Pins	I/O Common Pins			D_4-D_{15} RO_0-RO_3 $R1_0-R1_3$ $R2_0-R2_3$
	Input Pins			RA_0
	Input Pins			RA_1

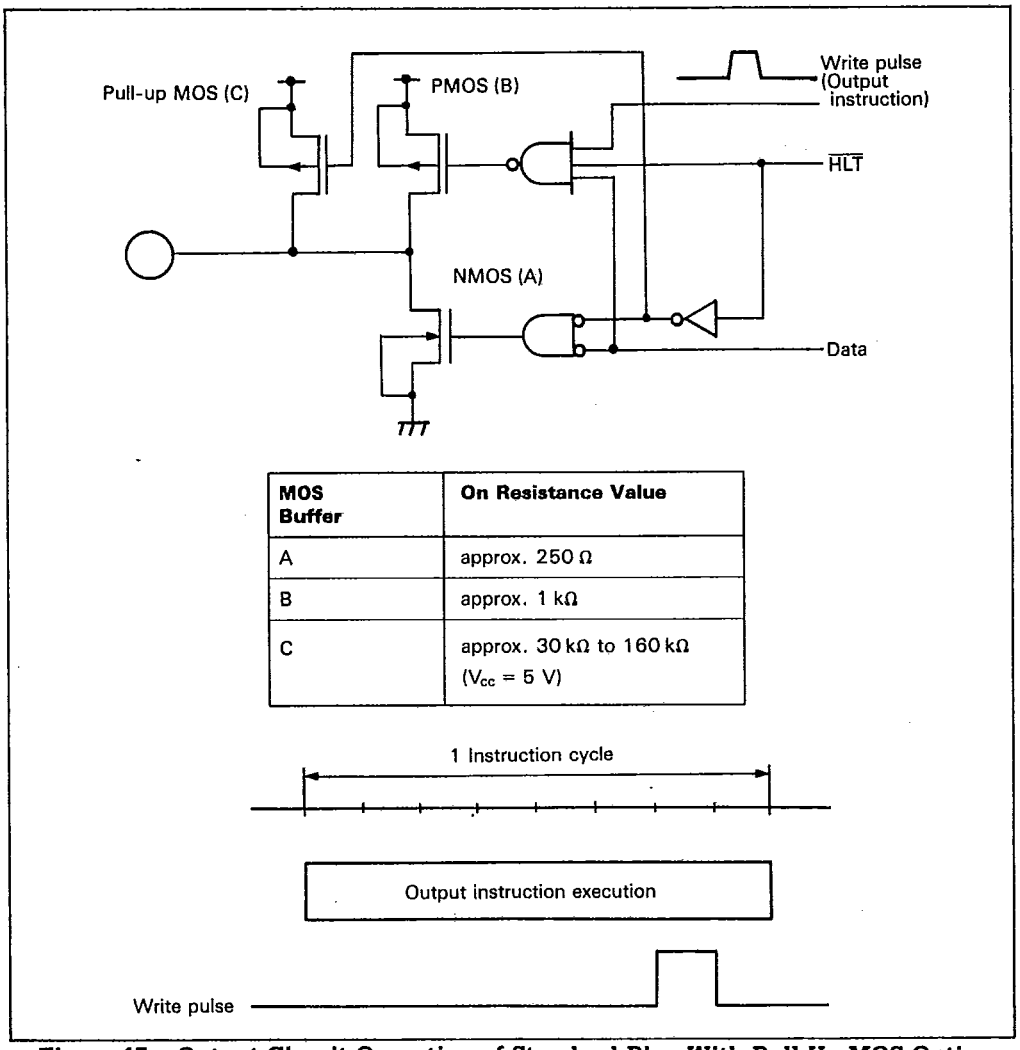
Table 17. I/O Pin Circuit Types (cont)

		Without Pull-Up MOS (NMOS Open Drain) or CMOS (A or C)	With Pull-Up MOS (B)	Applicable Pins
Standard Pins	I/O Common Pins			SCK (Note 2) (Output mode)
	Output Pins			SO
	Input Pins			$\overline{INT_0}$ $\overline{INT_1}$ SI $\overline{SCK}$ (Input mode)

Notes: 1. In the stop mode, $\overline{HLT}$ signal is 0, HLT signal is 1 and I/O pins are in high impedance state.
2. If the MCU is interrupted by serial interface in the external clock input mode, the $\overline{SCK}$ terminal becomes input only.

Table 18. Data Input from Input/Output Common Pins T-49-19-04

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard Pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High Voltage Pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0



MOS Buffer	On Resistance Value
A	approx. 250 Ω
B	approx. 1 kΩ
C	approx. 30 kΩ to 160 kΩ (V_{cc} = 5 V)

Figure 15. Output Circuit Operation of Standard Pins With Pull-Up MOS Option

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 19 shows the parts initialized by MCU reset, and the status of each.

Table 19. Initial Value After MCU Reset

Items			Initial Value by MCU Reset	Contents
Program Counter (PC)			$0000	Execute program from the top of ROM address
Status (ST)			1	Enable to branch with conditional branch instructions
Stack Pointer (SP)			$3FF	Stack level is 0
I/O Pin Output Register	Standard Pin	(A) Without Pull-Up MOS	1	Enable to input
		(B) With Pull-Up MOS	1	Enable to input
		(C) CMOS	1	—
	High-Voltage Pin	(D) Without Pull-Down MOS	0	Enable to input
		(E) With Pull-Down MOS	0	Enable to input
Interrupt Flag	Interrupt Enable Flag (I/E)		0	Inhibit all interrupts
	Interrupt Request Flag (IF)		0	No interrupt request
	Interrupt Mask (IM)		1	Mask interrupt request
Mode Register	Port Mode Register (PMR)		0000	See port mode register
	Serial Mode Register (SMR)		0000	See serial mode register
	Timer Mode Register A (TMA)		000	See timer mode register A
	Timer Mode Register B (TMB)		0000	See timer mode register B
Timer/Counter	Prescaler		$000	—
	Timer/Counter A (TCA)		$00	—
	Timer/Event Counter B (TCB)		$00	—
	Timer Load Register (TLR)		$00	—
	Octal Counter		000	—

T-49-19-04

Table 19. Initial Value After MCU Reset (cont)

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
Serial Data Register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	

Internal Oscillator Circuit

Figure 16 outlines the internal oscillator circuit. Crystal oscillator or ceramic filter oscillator can be selected as the oscillator type. Refer to table 20 to select the type. In addition, see figure 17 for layout of the crystal or ceramic filter.

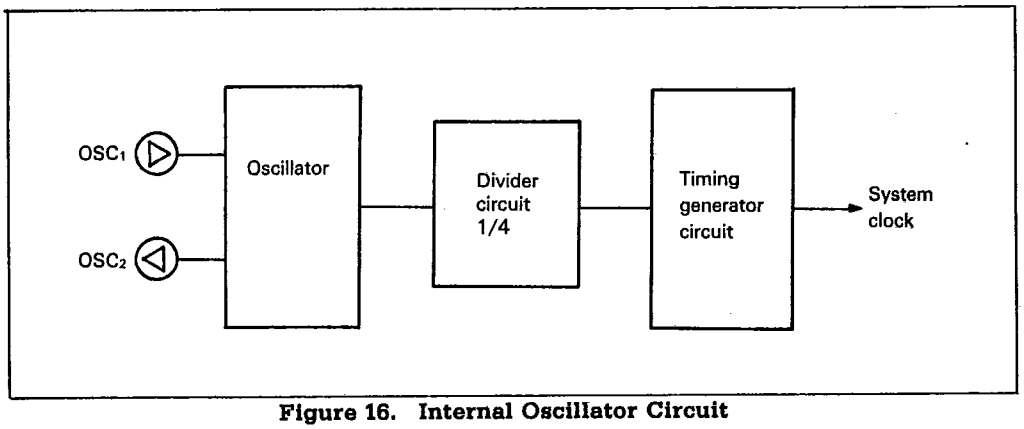


Figure 16. Internal Oscillator Circuit

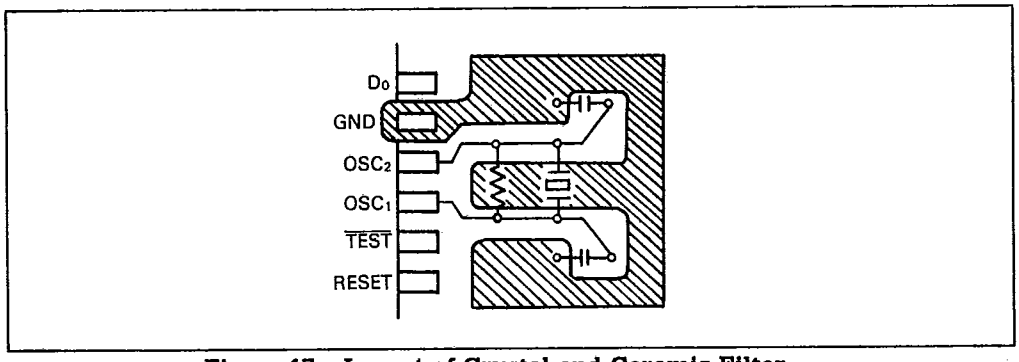
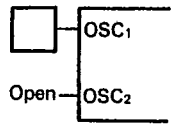
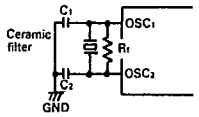
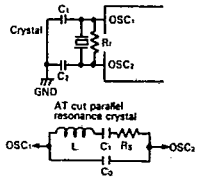


Figure 17. Layout of Crystal and Ceramic Filter

Table 20. Examples of Oscillator Circuits T-49-19-04

	Circuit Configuration	Circuit Constants
External Clock Operation	Oscillator  	
Ceramic Filter Oscillator	 	Ceramic filter CSA4.00MG (Murata) R_f: 1 MΩ ± 20% C_1: 30 pF ± 20% C_2: 30 pF ± 20%
Crystal Oscillator	 	R_f: 1 MΩ ± 20% C_1: 10-22 pF ± 20% C_2: 10-22 pF ± 20% Crystal: equivalent to circuit shown C_0: 7 pF max. R_S: 100 Ω max. f: 1.0—4.5 MHz

Notes : 1. Since the circuit constants change according to the crystal and ceramic filter resonator and stray capacitance of the board, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.
2. Wiring between OSC_1, OSC_2, and elements should be as short as possible, and never cross other wiring. Refer to figure 17.

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 21). Figure 18 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruction puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts, timer/counter and serial interface working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 21. Low Power Dissipation Mode

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Register, flag	Retained	Reset (note 1)
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained (note 2)	High impedance
Timer/counter, serial interface	Active	Stopped
Recovery method	RESET input, interrupt request	RESET input

Notes:
1. The MCU recovers from stop mode by RESET input. Refer to table 19 for the contents of flags and registers.
2. As I/O circuits are active, an I/O current may flow in standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 when an interrupt request asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the latter case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 19 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 20, reset input must be applied for at least t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, X/SPX registers, Y/SPY registers, carry, and serial data register may not retain their contents.

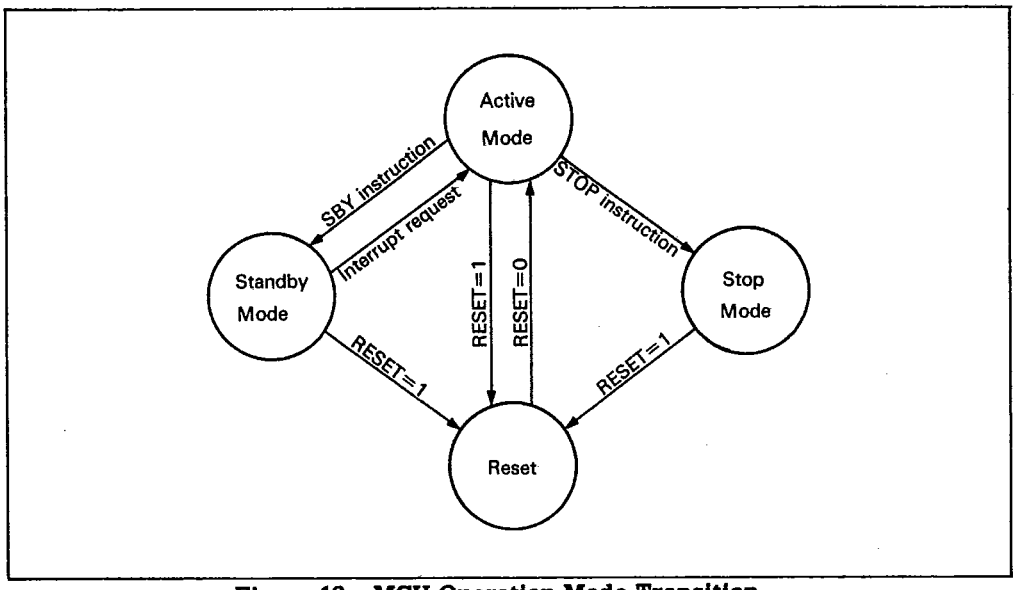


Figure 18. MCU Operation Mode Transition

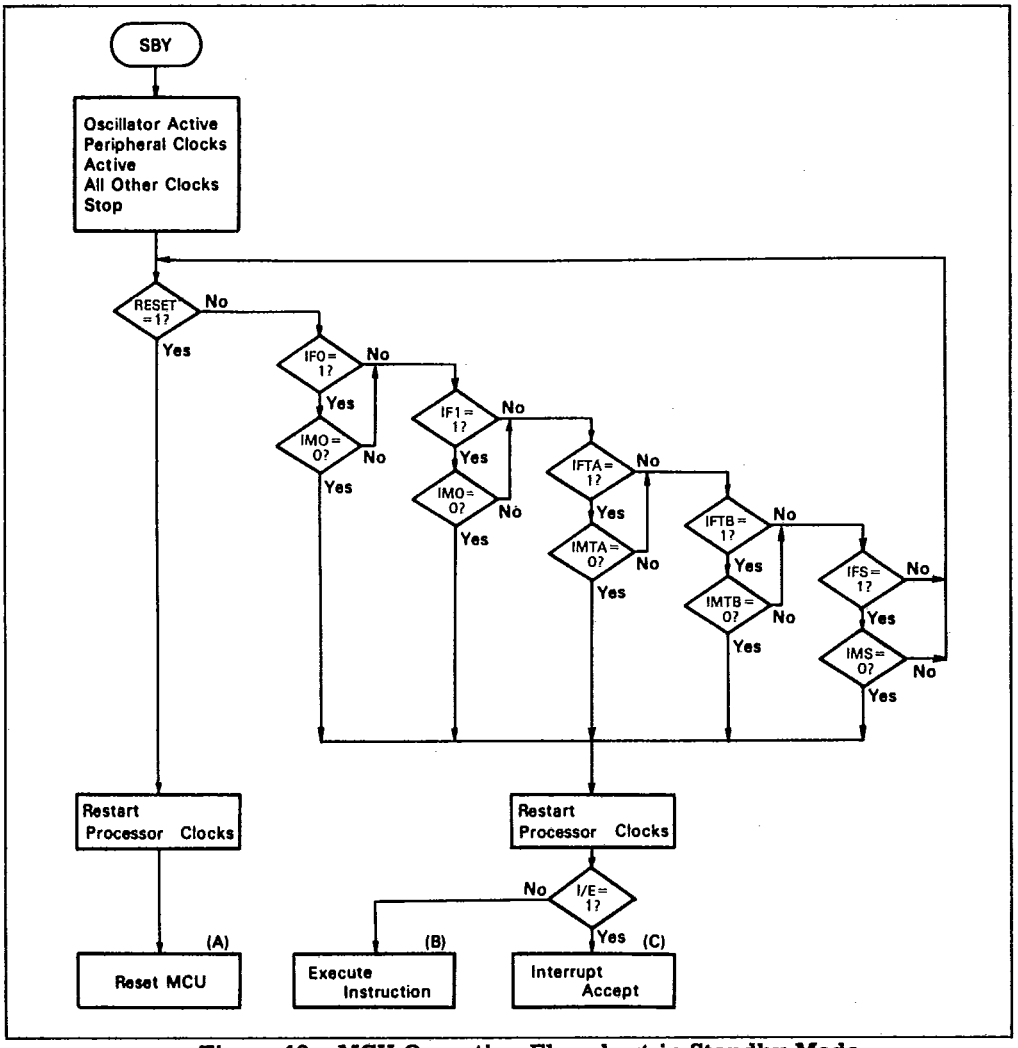


Figure 19. MCU Operating Flowchart in Standby Mode

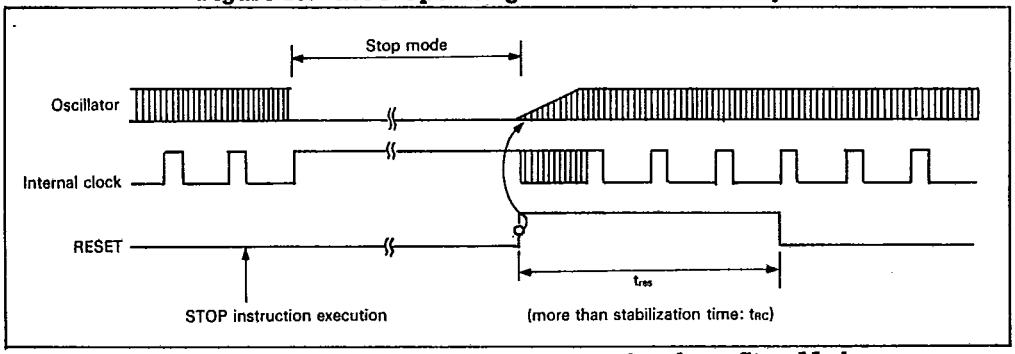


Figure 20. Timing Chart of Recovering from Stop Mode

PROM Mode Pin Description

Table 22 and figure 21 describe the pin functions in PROM mode

Table 22. PROM Mode Signals

Pin No.		MCU Mode		PROM Mode	
DC-64S, DP-64S	FP-64B	Symbol	I/O	Symbol	I/O
1	59	D_{11}	I/O	V_{CC}	
2	60	D_{12}	I/O		
3	61	D_{13}	I/O		
4	62	D_{14}	I/O		
5	63	D_{15}	I/O		
6	64	RO_0	I/O	A_1	I
7	1	RO_1	I/O	A_2	I
8	2	RO_2	I/O	A_3	I
9	3	RO_3	I/O	A_4	I
10	4	$R1_0$	I/O	A_5	I
11	5	$R1_1$	I/O	A_6	I
12	6	$R1_2$	I/O	A_7	I
13	7	$R1_3$	I/O	A_8	I
14	8	$R2_0$	I/O	A_0	I
15	9	$R2_1$	I/O	A_{10}	I
16	10	$R2_2$	I/O	A_{11}	I
17	11	$R2_3$	I/O	A_{12}	I
18	12	RA_0	I	V_{CC}	
19	13	RA_1	I		
20	14	$R3_0$	I/O	A_{13}	I
21	15	$R3_1$	I/O	A_{14}	I
22	16	$R3_2/\overline{INT_0}$	I/O		
23	17	$R3_3/\overline{INT_1}$	I/O		
24	18	$R5_0$	I/O		
25	19	$R5_1$	I/O		
26	20	$R5_2$	I/O		
27	21	$R5_3$	I/O		
28	22	$R6_0$	I/O		
29	23	$R6_1$	I/O		
30	24	$R6_2$	I/O		
31	25	$R6_3$	I/O		
32	26	V_{CC}		V_{CC}	
33	27	$R4_0/\overline{SCK}$	I/O	O_4	I/O
34	28	$R4_1$/SI	I/O	O_5	I/O
35	29	$R4_2$/SO	I/O	O_6	I/O
36	30	$R4_3$	I/O	O_7	I/O
37	31	$R7_0$	I/O	$\overline{CE}$	I
38	32	$R7_1$	I/O	$\overline{OE}$	I
39	33	$R7_2$	I/O		
40	34	$R7_3$	I/O		
41	35	$R8_0$	I/O		
42	36	$R8_1$	I/O		
43	37	$R8_2$	I/O		
44	38	$R8_3$	I/O		
45	39	$R9_0$	I	V_{PP}	
46	40	$R9_1$	I	A_9	I
47	41	$R9_2$	I	$\overline{M_0}$	I
48	42	$R9_3$	I	$\overline{M_1}$	I
49	43	RESET	I	RESET	I
50	44	$\overline{TEST}$	I	$\overline{TEST}$	I
51	45	OSC_1	I		
52	46	OSC_2	O		
53	47	GND		GND	
54	48	D_0	I/O	O_0	I/O
55	49	D_1	I/O	O_1	I/O
56	50	D_2	I/O	O_2	I/O
57	51	D_3	I/O	O_3	I/O
58	52	D_4	I/O		
59	53	D_5	I/O		
60	54	D_6	I/O		
61	55	D_7	I/O		
62	56	D_8	I/O		
63	57	D_9	I/O		
64	58	D_{10}	I/O	V_{CC}	

Note: I/O: Input/Output Pins
I: Input Pins
O: Output Pins

V_{PP} (Program Voltage): V_{PP} is the input for the program voltage (12.5 V ± 0.3 V) for programming the PROM.

$\overline{CE}$ (Chip Enable): $\overline{CE}$ input programs and verifies internal PROM.

$\overline{OE}$ (Output Enable): $\overline{OE}$ is the data output control signal for verify input.

A_0–A_{14} (Address Bus): A_0–A_{14} are address input pins for internal PROM.

O_0–O_7 (PROM Data Bus): O_0–O_7 are the data bus for internal PROM.

$\overline{M}_0$, $\overline{M}_1$ (Mode): $\overline{M}_0$ and $\overline{M}_1$ set PROM mode. PROM mode is set when $\overline{M}_0$, $\overline{M}_1$, and $\overline{TEST}$ pins are low level and RESET pin is high level.

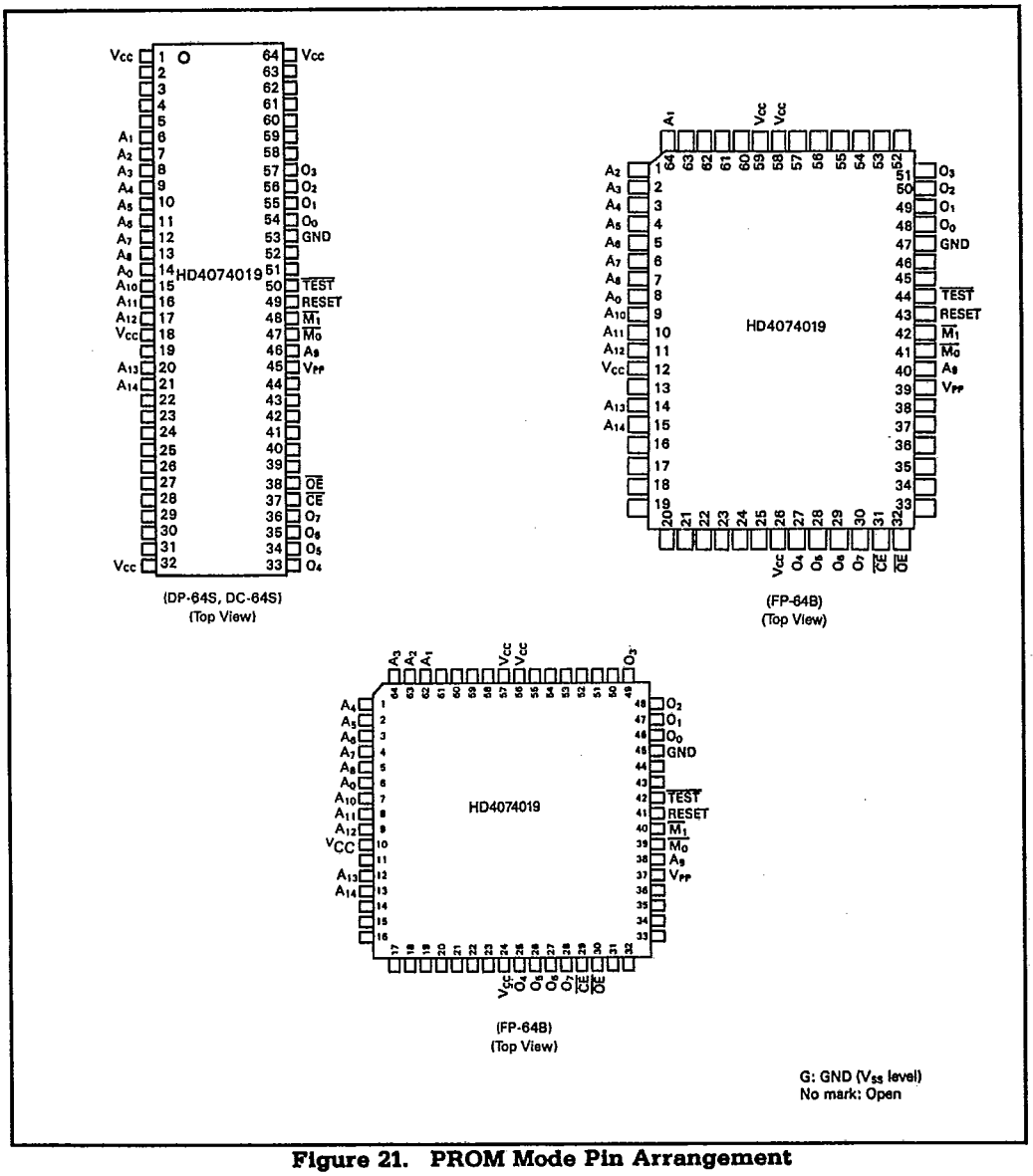


Figure 21. PROM Mode Pin Arrangement

Programmable ROM Operation

The HD4074019's on-chip PROM is programmed in PROM mode (figures 22–24). PROM mode is set by bringing $\overline{TEST}$, $\overline{M_0}$, and $\overline{M_1}$ low, and RESET high as shown in figure 22. In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 64-to-28-pin socket adapter. Table 24 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputer incorporate conversion circuit to use a general perpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, lower 5 bits and upper 5 bits as shown in figure 23. For example, if 8 kwords of on-chip PROM are programmed by a general purpose PROM programmer, 16 kbytes of addresses ($0000-$3FFF) should be specified.

Programming And Verification

The HD4074019 can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 23 shows how programming and verification modes are selected.

Figure 24 is a programming flowchart, and figure 42 is a timing chart. For precautions on PROM programming, refer to Precautions and On-Chip EPROM reliability after programing.

Erasing

PROMs in ceramic window packages can be erased by ultraviolet light. All erased bits become 1s.

Erasing conditions are: ultraviolet (UV) light with wavelength 2537Å with a minimum irradiation of 15W·s/cm². These conditions are satisfied by exposing the LSI to a 12,000 μW/cm² UV source for 15-20 minutes, at a distance of 1 inch.

Precautions

1. Addresses $0000 to $7FFF should be specified if the PROM is programmable by a PROM programmer. Note that the plastic package type cannot be erased and reprogrammed. (Ceramic window packages can be erased and reprogrammed by ultraviolet light.) Data in address space beyond $8000 must be set to $FF.

2. Be careful that the PROM programmer, socket adapter and LSI match. Using the wrong programmer of socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed in the programmer.

3. The PROM should be programmed with V_{PP}=12.5 V. Other PROMs use 21 V. If 21 V is applied to the HD4074019, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP}.

On-Chip EPROM Reliability after Programming

Generally, semiconductors are reliable except for initial failures. Parts can be screened to avoid failures. Exposure to high temperature is a kind of screening which removes PROM memory cells with data hold failures in a short time. This is done to the ZTATs in the wafer stage, so ZTAT data hold charcteristics are high. Exposing the LSI to 150°C after user programming can effectively upgrade these characteristics. Figure 25 shows the recommeded screening flow.

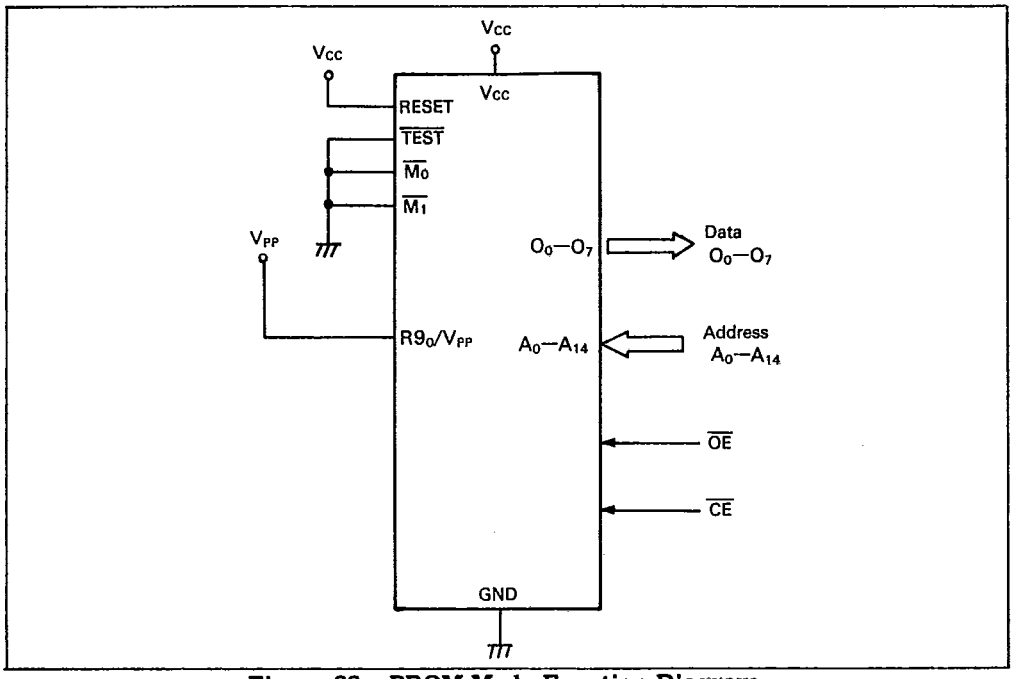


Figure 22. PROM Mode Function Diagram

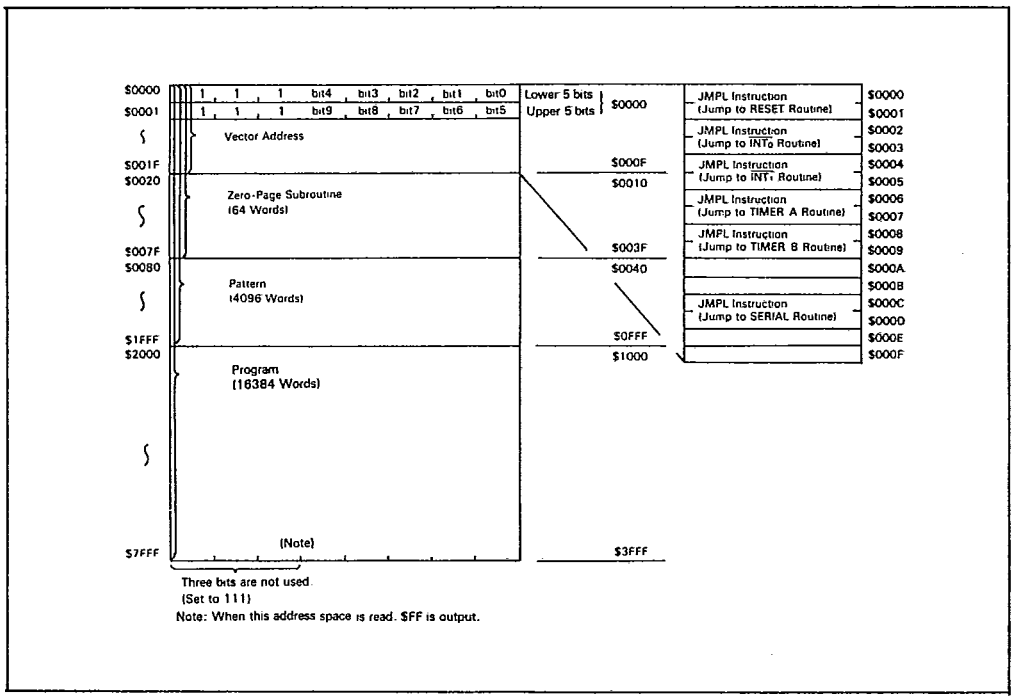


Figure 23. PROM Mode Memory Map

Table 23. PROM Mode Selection

Mode	Pin $\overline{CE}$	Pin $\overline{OE}$	Pin V_{PP}	Pin O_0-O_7
Programming	Low	High	V_{PP}	Data input
Verify	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 24. PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter	
Maker	**Type name**	**Maker**	**Type name**
DATA I/O	22B 29B	Hitachi	TBD
AVAL Corp	PKW-1000 PKW-7000	Hitachi	TBD

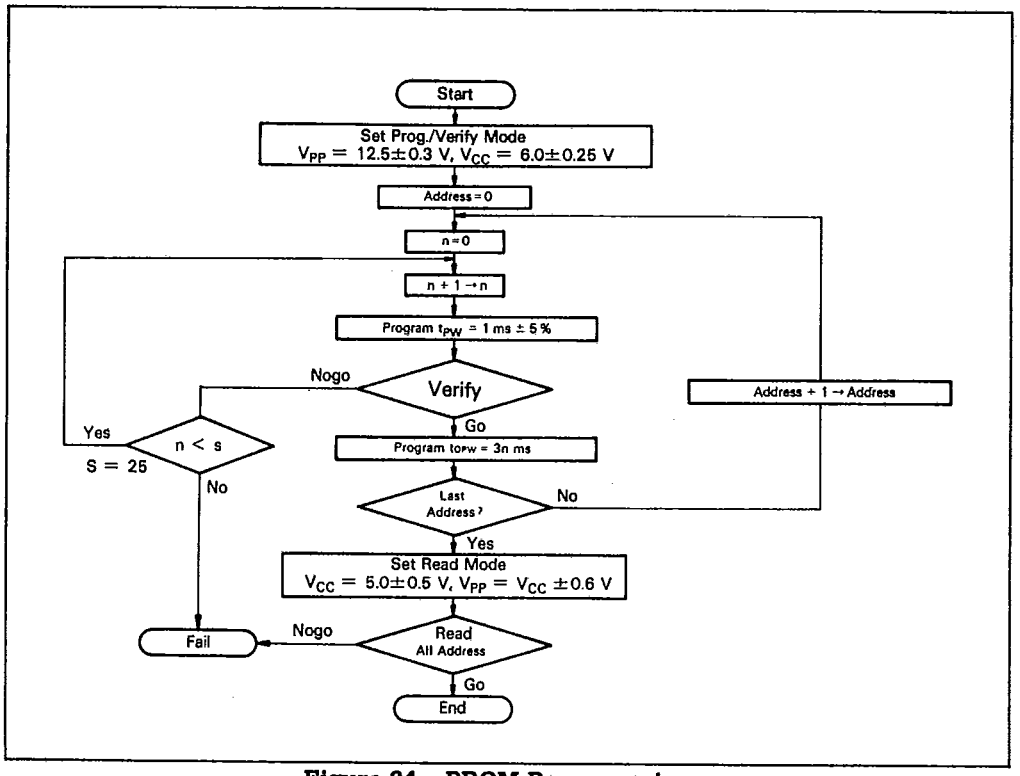
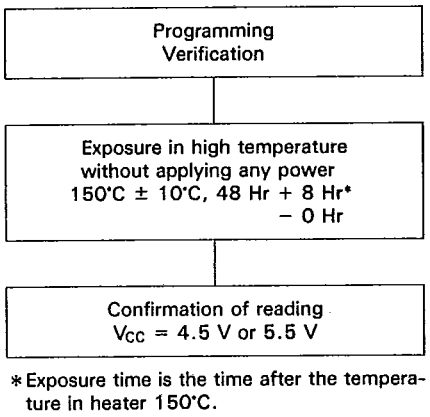


Figure 24. PROM Programming



*Exposure time is the time after the temperature in heater 150°C.

Note: If programming erros occur continuously during programming with one PROM programmer, stop programming and check the PROM programmer or socket adapter.
If trouble occurs in verification after programming, or after exposure to high temperatures, please inform a Hitachi engineer.

Figure 25. Recommended Screening Flow

Addressing Mode

RAM Addressing Mode

As shown in figure 26, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from $020 to $02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four kinds of ROM addressing modes, as shown in figure 27.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with the 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address $0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with the 8-bit immediate data.

When BR is on a page boundary (256n + 255) (figure 28), executing a BR instruction transfers the PC contents to the next page, due to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at $0000-$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low- order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 29). When bit 8 in the referenced ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

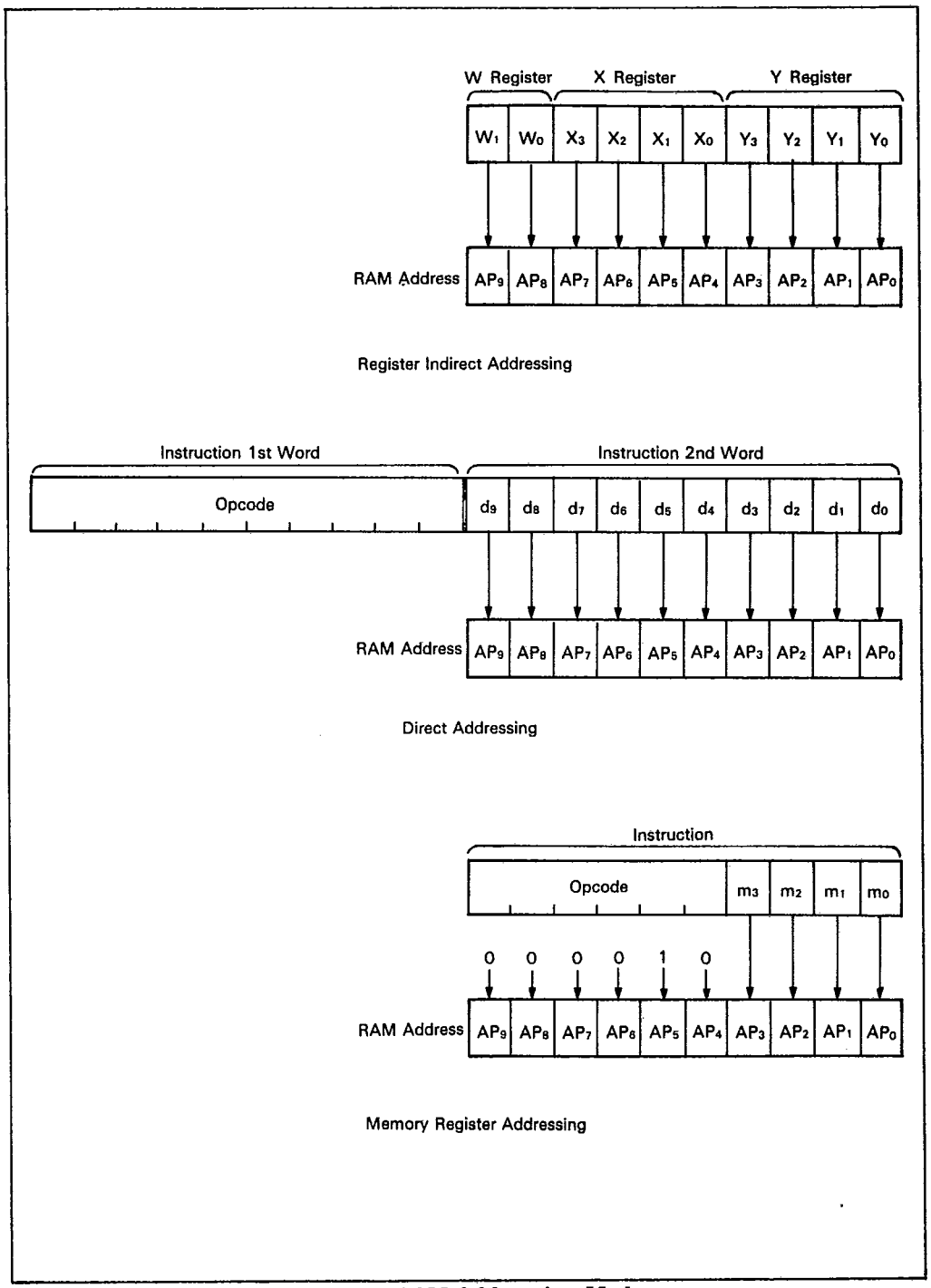


Figure 26. RAM Addressing Modes

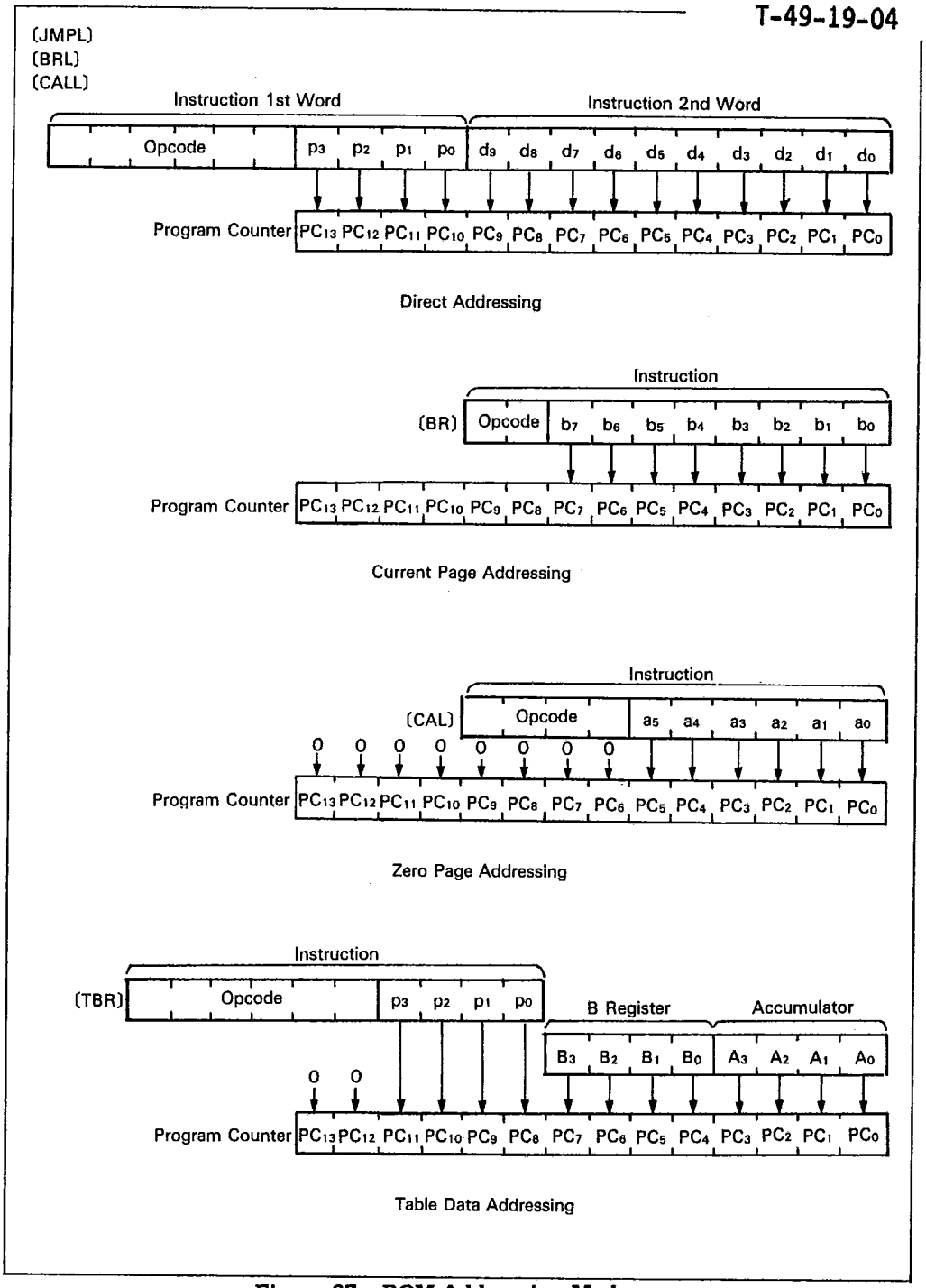


Figure 27. ROM Addressing Modes

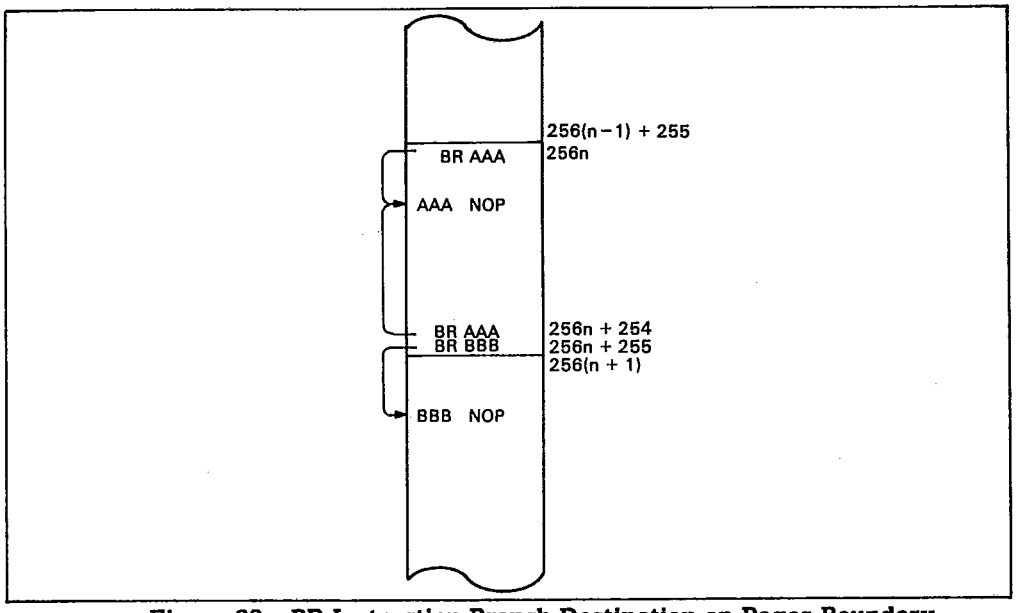


Figure 28. BR Instruction Branch Destination on Pages Boundary

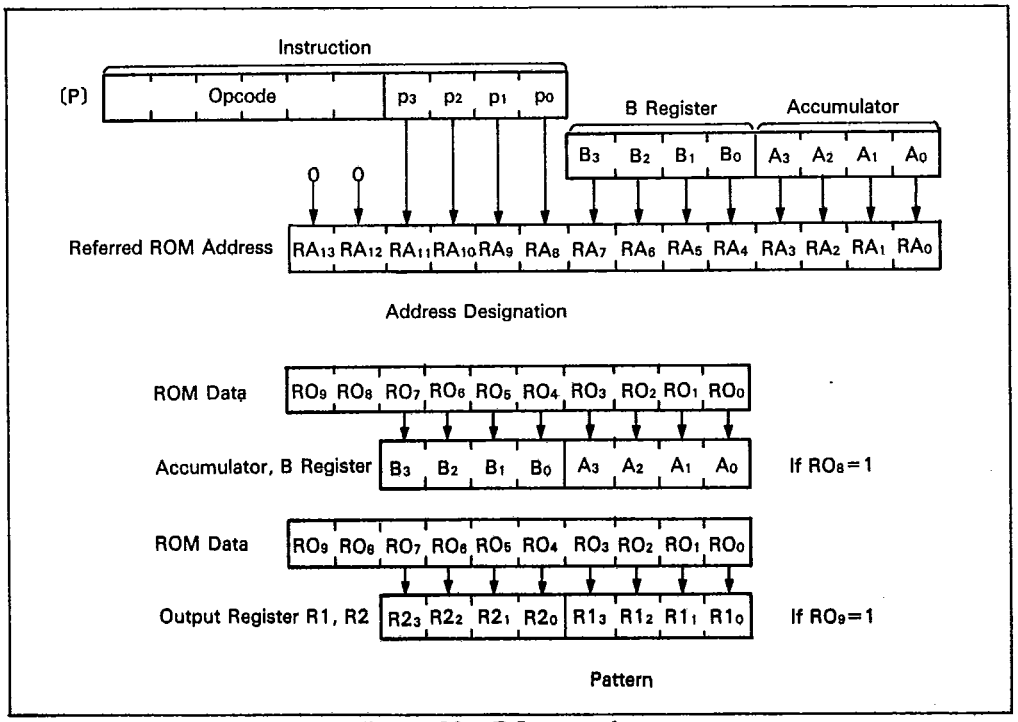


Figure 29. P Instruction

Instruction Set

T-49-19-04

The HD404019, HD4074019 provides 101 instructions which are classified into 10 groups as follows:

1. Immediate instructions
2. Register-to-register instructions
3. RAM address instructions
4. RAM register instructions
5. Arithmetic instructions
6. Compare instructions
7. RAM bit manipulation instructions
8. ROM address instructions
9. Input/output instructions
10. Control instructions

Tables 25-34 list their functions, and table 35 is an opcode map.

Table 25. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i→M, Y+1→Y	NZ	1/1

Table 26. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m) ↔ A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 27. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y−1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y−A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X↔SPX, Y↔SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

Table 28. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X↔SPX, Y↔SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X↔SPX, Y↔SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X↔SPX, Y↔SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X↔SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y−1→Y (X↔SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X↔SPX, Y↔SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X↔SPX, Y↔SPY)		1/1

Note: (XY) and (X) have the following meaning:

1. The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given below).
   The op-code X or Y is assembled as follows.

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X↔SPX, Y↔SPY

2. The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).
   The op-code X is assembled as follows.

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table 29. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i_3 i_2 i_1 i_0	A+i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B−1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A}$+1 →A		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B}$ → B		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA → A OVF→CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A+CA→A OVF→CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M−A−$\overline{CA}$→A NB→CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M−A−$\overline{CA}$→A NB→CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B→A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M→A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∩ M→A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M→A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∪ M→A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M→A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ⊕ M→A	NZ	2/2

Note: ∩ : Logical AND
∪ : Logical OR
⊕ : Exclusive OR

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Table 30. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	i ≦ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≦ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≦ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≦ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≦ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	A ≦ i	NB	1/1

Table 31. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	0 →M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 32. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 →I/E CA Restore	ST	1/3

Table 33. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 34. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Table 35. Opcode Map T-49-19-04

R9	H \ L	R8=0 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	R8=1 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NOP	XSPX	XSPY	XSP XY	AN EM				AM				ORM				LAW				ANEMD				AMD				ORMD			
	1	RTN	RTNI			ALEM				AMC				EORM				LWA				ALEMD				AMCD				EORMD			
	2	INEM i(4)																INEMD i(4)															
	3	ILEM i(4)																ILEMD i(4)															
	4	LBM(XY)				BNEM				LAB				IB				COMB				OR				STS				SBY	STOP		
	5	LMAIY(X)				AYY				LASPY				IY				JMPL p(4)															
	6	NEGA				RED				LASPX							TC	CALL p(4)															
	7	YNEI i(4)																BRL p(4)															
	8	XMA(XY)				SEM n(2)				REM n(2)				TM n(2)				XMAD				SEMD n(2)				REMD n(2)				TMD n(2)			
	9	LAM(XY)				LMA(XY)				SMC				ANM				LAMD				LMAD				SMCD				ANMD			
	A	ROTR	ROTL			DAA				DAS							LAY	LMID i(4)															
	B	TBR p(4)																P p(4)															
	C	XMB(XY)				BLEM				LBA							DB	CAL a(6)															
	D	LMADY(X)				SYY				LYA							DY																
	E	TD				SED				LXA				REC			SEC																
	F	LWI i(2)																															
1	0	LBI i(4)																BR b(8)															
	1	LYI i(4)																															
	2	LXI i(4)																															
	3	LAI i(4)																															
	4	LBR m(4)																															
	5	LAR m(4)																															
	6	REDD m(4)																															
	7	LAMR m(4)																															
	8	AI i(4)																															
	9	LMIIY i(4)																															
	A	TDD m(4)																															
	B	ALEI i(4)																															
	C	LRB m(4)																															
	D	LRA m(4)																															
	E	SEDD m(4)																															
	F	XMRA m(4)																															

1-word/2-cycle Instruction · 1-word/3-cycle Instruction · RAM Direct Address Instruction (2-word/2-cycle) · 2-word/2-cycle Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	− 0.3 to + 7.0	V	
Programming Voltage	V_{PP}	− 0.3 to + 14	V	13
Terminal Voltage	V_T	− 0.3 to V_{CC} + 0.3	V	3
		V_{CC} − 42 to V_{CC} + 0.3	V	4
Total Allowance of Input Current	ΣI_O	50	mA	5
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Total Allowance of Output Current	$-\Sigma I_O$	150	mA	6
Operating Temperature	T_{opr}	− 20 to + 75	°C	
Storage Temperature	T_{stg}	− 55 to + 125	°C	

Notes:
1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
2. All voltages are with respect to GND.
3. Standard pins.
4. High-voltage pins.
5. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
6. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
8. D_0-D_3 and R3−R8.
9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
10. D_0-D_3 and R3−R8.
11. R0−R2.
12. D_4-D_{15}.
13. Applied to HD4074019.

HD4074019 Electrical Characteristics

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DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C, unless otherwise noted.)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, SCK, INT_0, INT_1	0.8 V_{CC}	V_{CC} + 0.3	V		
		OSC_1	V_{CC} − 0.5	V_{CC} + 0.3	V		
		SI	0.7V_{CC}	V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	RESET, SCK, INT_0, INT_1	−0.3	0.2V_{CC}	V		
		OSC_1	−0.3	0.5	V		
		SI	−0.3	0.3V_{CC}	V		
Output High Voltage	V_{OH}	SCK, SO	V_{CC} − 1.0		V	$-I_{OH}$=1.0 mA	
			V_{CC} − 0.5		V	$-I_{OH}$=0.5 mA	
Output Low Voltage	V_{OL}	SCK, SO		0.4	V	I_{OL}=1.6 mA	
Input/Output Leakage Current	$\|I_{IL}\|$	RESET, SCK, INT_0, INT_1, OSC_1, SI, SO		1	μA	V_{in} = 0 V to V_{CC}	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}		TBD	mA	V_{CC} = 5 V	2,5
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}		TBD	mA	Maximum logic operation V_{CC} = 5 V	3,5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}		TBD	μA	V_{in}(TEST) = V_{CC} − 0.3 V to V_{CC}, V_{in}(RESET) = 0 V to 0.3 V	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2		V		

Notes:
1. Excluding pull-up MOS current and output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, TEST: V_{CC}
   - D_0-D_3, R3—R9: V_{CC}
   - D_4-D_{15}, R0-R2, RA_0, RA_1: V_{disp}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - Serial interface: Stop
   - RESET: GND
   - TEST: V_{CC}
   - D_0-D_3, R3—R9: V_{CC}
   - D_4-D_{15}, R0-R2, RA_0, RA_1 : V_{disp}

4. Excluding pull-down MOS current.
5. When f_{osc} = x MHz, estimate the current dissipation as follows:
   Max value @ x MHz = x/4 × (max value @ 4 MHz)

Input/Output Characteristics for Standard Pin
(V_{CC} = 5 V ± 10%, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C, unless otherwise noted.)

Item	Symbol	Pin	Min	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D_0-D_3, R3-R5 R9	0.7V_{CC}	V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	D_0-D_3, R3-R5 R9	−0.3	0.3V_{CC}	V		
Output Low Voltage	V_{OL}	D_0-D_3, R3-R8		0.4	V	I_{OL} = 1.6 mA	
Input/Output Leakage Current	$\|I_{IL}\|$	D_0-D_3, R3-R8, $R9_1$-$R9_3$		1	µA	V_{in} = 0 V to V_{CC}	1
		$R9_0$		20	µA		

Note: 1. Pull-up MOS current and output buffer current are excluded.

Input/Output Characteristics for High Voltage Pin
(V_{CC} = 5 V ± 10%, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C, unless otherwise noted.)

Item	Symbol	Pin	Min	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D_4-D_{15}, R0, R1, R2, RA_0, RA_1	0.7 V_{CC}	V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	D_4-D_{15}, R0, R1, R2, RA_0, RA_1	V_{CC} − 40	0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D_4-D_{15}	V_{CC} − 3.0		V	− I_{OH} = 15 mA, V_{CC} = 5 V	
			V_{CC} − 2.0		V	− I_{OH} = 10 mA, V_{CC} = 5 V	
			V_{CC} − 1.0		V	− I_{OH} = 4 mA, V_{CC} = 5 V	
		R0-R2	V_{CC} − 3.0		V	− I_{OH} = 3 mA, V_{CC} = 5 V	
			V_{CC} − 2.0		V	− I_{OH} = 2 mA, V_{CC} = 5 V	
			V_{CC} − 1.0		V	− I_{OH} = 0.8 mA, V_{CC} = 5 V	
Output Low Voltage	V_{OL}	D_4-D_{15}, R0-R2		V_{CC} − 34	V	150 kΩ to V_{CC} − 40	
Input/Output Leakage Current	$\|I_{IL}\|$	D_4-D_{15}, R0-R2, RA_0, RA_1		20	µA	V_{in} = V_{CC} − 40 V, V_{CC}	1

Note: 1. Pull-down MOS current and output buffer current are excluded.

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AC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC_1, OSC_2	0.2	4	4.5	MHz	divide by 4	
Instruction Cycle Time	t_{cyc}		0.89	1	20	μs	divide by 4	
Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2			20	ms		1
External Clock High, Low Level Width	t_{CPH}, t_{CPL}	OSC_1	92			ns	divide by 4	2
External Clock Rise Time	t_{CPr}	OSC_1			20	ns		2
External Clock Fall Time	t_{CPf}	OSC_1			20	ns		2
$\overline{INT_0}$ High Level Width	t_{IOH}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_0}$ Low Level Width	t_{IOL}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_1}$ High Level Width	t_{I1H}	$\overline{INT_1}$	2			t_{cyc}		3
$\overline{INT_1}$ Low Level Width	t_{I1L}	$\overline{INT_1}$	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins exept $R9_0$			30	pF	f = 1 MHz, V_{in} = 0 V	
		$R9_0$			180	pF		
RESET Fall Time	t_{RSTf}				20	ms		4

Notes:
1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage after power-on, or after RESET goes high. At power-on or STOP mode release, RESET must be kept high for at least t_{RC}. Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit. (See figure 30)
2. See figure 31.
3. See figure 32.
4. See figure 33.

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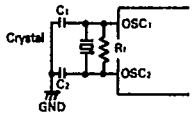
Serial Interface Timing Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C, unless otherwise noted.)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$ (Output)	1		t_{cyc}		1. 2
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	$\overline{SCK}$ (Output)	0.4		t_{cyc}		1. 2
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	$\overline{SCK}$ (Output)		40	ns		1. 2
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$ (Input)	1		t_{cyc}		1
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	$\overline{SCK}$ (Input)	0.4		t_{cyc}		1
Transfer Clock END Detect High Level Width	t_{SCKHD}	$\overline{SCK}$ (Input)	1		t_{cyc}		1
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	$\overline{SCK}$ (Input)		40	ns		1
Serial Output Data Delay Time	t_{DSO}	SO		300	ns		1. 2
Serial Input Data Set-up Time	t_{SSI}	SI	100		ns		1
Serial Input Data Hold Time	t_{HSI}	SI	200		ns		1

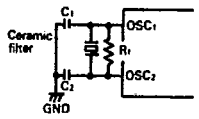
Note: 1. See figure 34
2. See figure 35

Crystal oscillator



Crystal: 4.194304 MHz NC-18C (Nihon Denpa Kogyo)
R_f: 1 MΩ ± 20 %
C_1: 22 pF ± 20 %
C_2: 22 pF ± 20 %

Ceramic filter oscillator



Ceramic filter: CSA 4.00 MG (Murata)
R_f: 1 MΩ ± 20 %
C_1: 30 pF ± 20 %
C_2: 30 pF ± 20 %

Figure 30. Oscillator Circuit

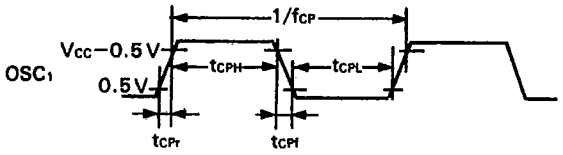


Figure 31. Oscillator Timing

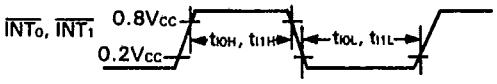


Figure 32. Interrupt Timing

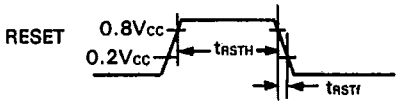
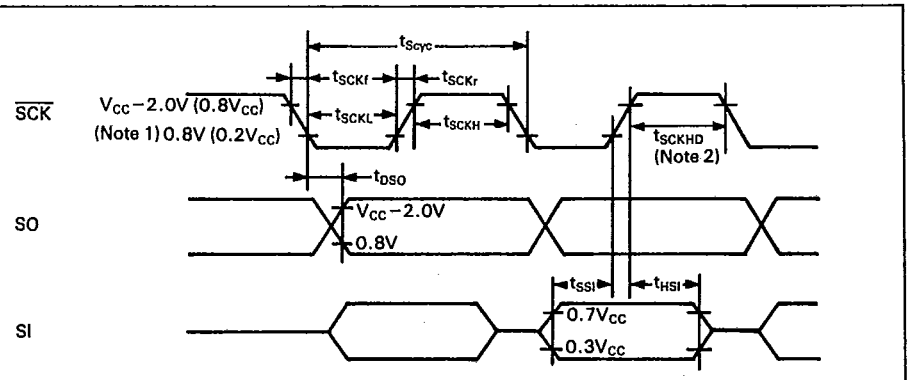


Figure 33. Reset Timing



Notes: 1. $V_{CC}-2.0V$ and 0.8V are the threshold voltage for transfer clock output. $0.8V_{CC}$ and $0.2V_{CC}$ are the threshold voltage for transfer clock input.
2. After 8 clocks are transferred through $\overline{SCK}$, at least t_{SCKHD} must pass before the next serial interface transfer clock comes into $\overline{SCK}$. If the next transfer clock comes into $\overline{SCK}$ within t_{SCKHD}, the serial interface request flag can't be set.

Figure 34. Timing Diagram of Serial Interface

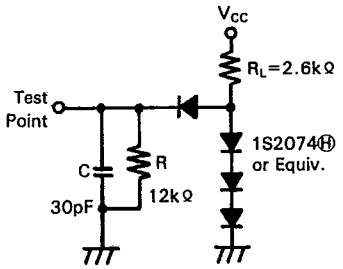


Figure 35. Timing Load Circuit

HD404019 Electrical Characteristics

DC Characteristics

(V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$	0.8V_{CC}	V_{CC} + 0.3	V		
		SI	0.7V_{CC}	V_{CC} + 0.3	V		
		OSC_1	V_{CC} − 0.5	V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$	−0.3	0.2V_{CC}	V		
		SI	−0.3	0.3V_{CC}	V		
		OSC_1	−0.3	0.5	V		
Output High Voltage	V_{OH}	SCK, SO	V_{CC} − 1.0		V	− I_{OH} = 1.0 mA	
			V_{CC} − 0.5		V	− I_{OH} = 0.5 mA	
Output Low Voltage	V_{OL}	SCK, SO		0.4	V	I_{OL} = 1.6 mA	
Input/Output Leakage Current	$\lvert I_{IL} \rvert$	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1		1	μA	V_{in} = 0 V to V_{CC}	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}		TBD	mA	V_{CC} = 5 V; f_{osc} = 4 MHz, ÷ 4	2, 5

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}		TBD	mA	V_{CC} = 5 V; f_{osc} = 4 MHz, ÷ 4	3, 5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}		TBD	μA	$V_{in}(\overline{TEST}) = V_{CC} - 0.3$ V to V_{CC}; V_{in}(RESET) = 0 V to 0.3 V	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2		V		

Notes:
1. Excluding pull-up MOS current and output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0-D_3, R3-R9: V_{CC}
   - D_4-D_{15}, R0-R2, RA_0, RA_1: V_{disp}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - Serial interface: Stop
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0-D_3, R3-R9: V_{CC}
   - D_4-D_{15}, R0-R2, RA_0, RA_1: V_{disp}
4. Excluding pull-down MOS current.
5. When f_{osc} = x MHz, estimate the current dissipation as follows:
   Max value @ x MHz = x/4 × (max value @ 4 MHz)

Input/Output Characteristics for Standard Pins
(V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D_0-D_3, R3-R5, R9	0.7V_{CC}		V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	D_0-D_3, R3-R5, R9	−0.3		0.3V_{CC}	V		
Output High Voltage	V_{OH}	D_0-D_3, R3-R8	V_{CC} − 1.0			V	$-I_{OH}$ = 1.0 mA	1
		D_0-D_3, R3-R8	V_{CC} − 0.5			V	$-I_{OH}$ = 0.5 mA	1
Output Low Voltage	V_{OL}	D_0-D_3, R3-R8			0.4	V	I_{OL} = 1.6 mA	
Input/Output Leakage Current	$\lvert I_{IL} \rvert$	D_0-D_3, R3-R9			1	μA	V_{in} = 0 V to V_{CC}	2
Pull-Up MOS Current	$-I_p$	D_0-D_3, R3-R9	TBD	TBD	TBD	μA	V_{CC} = 5 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins with CMOS output selected by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins with pull-up MOS selected by mask option.

Input/Output Characteristics for High Voltage Pins
(V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D_4-D_{15}, R0, R1, R2, RA_0, RA_1	0.7 V_{CC}		V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	D_4-D_{15}, R0, R1, R2, RA_0, RA_1	V_{CC} − 40		0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D_4-D_{15}	V_{CC} − 3.0			V	− I_{OH}=15 mA, V_{CC} = 5 V ± 20%	
			V_{CC} − 2.0			V	− I_{OH}=10 mA, V_{CC} = 5 V ± 20%	
			V_{CC} − 1.0			V	− I_{OH}= 4 mA	
		R0-R2	V_{CC} − 3.0			V	− I_{OH} = 3 mA, V_{CC} = 5 V ± 20%	
			V_{CC} − 2.0			V	− I_{OH} = 2 mA, V_{CC} = 5 V ± 20%	
			V_{CC} − 1.0			V	− I_{OH} = 0.8 mA	
Output Low Voltage	V_{OL}	D_4-D_{15}, R0-R2			V_{CC} − 37	V	V_{disp} = V_{CC} − 40 V	1
		D_4-D_{15}, R0-R2			V_{CC} − 37	V	150 kΩ to V_{CC} − 40 V	2
Input/Output Leakage Current	$\lvert I_{IL} \rvert$	D_4-D_{15}, R0-R2, RA_0, RA_1			20	μA	V_{in} = V_{CC} − 40 V to V_{CC}	3
Pull-Down MOS Current	I_d	D_4-D_{15}, R0-R2, RA_0, RA_1	TBD	TBD	TBD	μA	V_{disp} = V_{CC} − 35 V, V_{in} = V_{CC}	4

Notes:
1. Applied to I/O pins with pull-down MOS selected by mask option.
2. Applied to I/O pins without pull-down MOS (PMOS open drain) selected by mask option.
3. Pull-down MOS current and output buffer current are excluded.
4. Applied to I/O pins with pull-down MOS selected by mask option.

AC Characteristics

(V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC_1, OSC_2	0.2	4	4.5	MHz	divide by 4	
Instruction Cycle Time	t_{cyc}		0.89	1	20	μs		
Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2			20	ms		1
External Clock High, Low Level Width	t_{CPH}, t_{CPL}	OSC_1	92			ns	divide by 4	2
External Clock Rise Time	t_{CPr}	OSC_1			20	ns		2
External Clock Fall Time	t_{CPf}	OSC_1			20	ns		2
$\overline{INT_0}$ High Level Width	t_{I0H}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_0}$ Low Level Width	t_{I0L}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_1}$ High Level Width	t_{I1H}	$\overline{INT_1}$	2			t_{cyc}		3
$\overline{INT_1}$ Low Level Width	t_{I1L}	$\overline{INT_1}$	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			30	pF	f = 1 MHz, V_{in} = 0 V	
RESET Fall Time	t_{RSTf}				20	ms		4

Notes:
1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage (3.5 V) after power-on, or after RESET goes high. At power-on or stop mode release, RESET must be kept high for at least t_{RC}. Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit. (See figure 36)
2. See figure 37.
3. See figure 38.
4. See figure 39.

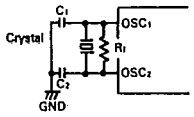
Serial Interface Timing Characteristics

(V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$ (Output)	1		t_{cyc}		1. 2
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	$\overline{SCK}$ (Output)	0.4		t_{cyc}		1. 2
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	$\overline{SCK}$ (Output)		40	ns		1. 2
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$ (Input)	1		t_{cyc}		1
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	$\overline{SCK}$ (Input)	0.4		t_{cyc}		1
Transfer Clock END Detect High Level Width	t_{SCKHD}	$\overline{SCK}$ (Input)	1		t_{cyc}		1
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	$\overline{SCK}$ (Input)		40	ns		1
Serial Output Data Delay Time	t_{DSO}	SO		300	ns		1. 2
Serial Input Data Set-up Time	t_{SSI}	SI	100		ns		1
Serial Input Data Hold Time	t_{HSI}	SI	200		ns		1

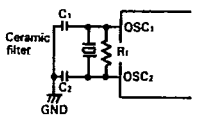
Notes: 1. See figure 40.
2. See figure 41.

Crystal oscillator



Crystal: 4.194304 MHz NC-18C (Nihon Denpa Kogyo)
R_f: 1 MΩ ± 20 %
C_1: 22 pF ± 20 %
C_2: 22 pF ± 20 %

Ceramic filter oscillator



Ceramic filter: CSA 4.00 MG (Murata)
R_f: 1 MΩ ± 20%
C_1: 30 pF ± 20 %
C_2: 30 pF ± 20 %

Figure 36. Oscillator Circuit

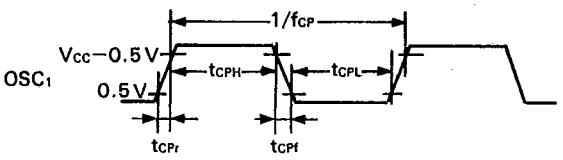


Figure 37. Oscillator Timing

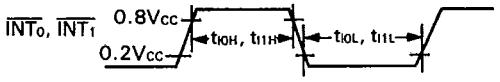


Figure 38. Interrupt Timing

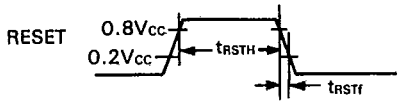
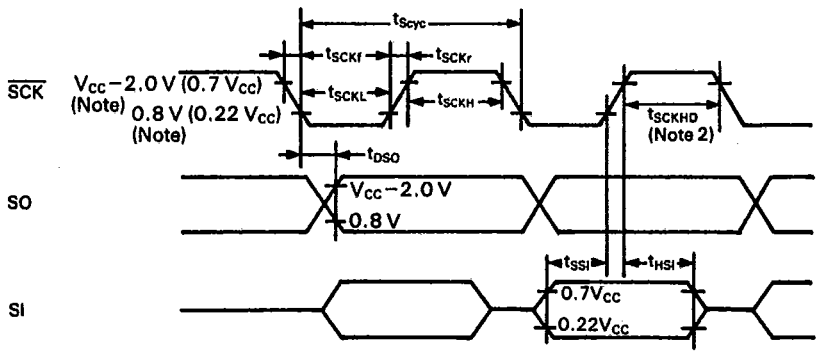


Figure 39. Reset Timing



Notes: 1. $V_{CC}-2.0$ V and 0.8 V are the threshold voltages for transfer clock output. $0.7V_{CC}$ and $0.22V_{CC}$ are the threshold voltages for transfer clock input.
2. After 8 clocks are transferred through $\overline{SCK}$, at least t_{SCKHD} must pass before the next serial interface transfer clock comes into $\overline{SCK}$. If the next transfer clock comes into $\overline{SCK}$ within t_{SCKHD}, the serial interface request flag can't be set.

Figure 40. Timing Diagram of Serial Interface

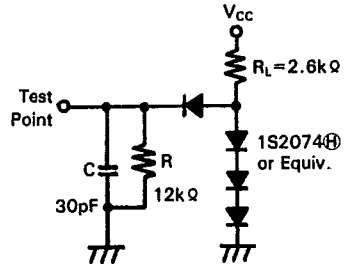


Figure 41. Timing Load Circuit

Programming Electrical Characteristics for HD4074019 Write and Verify Mode

T-49-19-04

DC Characteristics

(V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, V_{SS} = 0 V, T_a = 25°C ± 5°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	V_{IH}	2.2		V_{CC}+0.3	V	
Input low voltage	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	V_{IL}	−0.3		0.8	V	
Output high voltage	O_0–O_7	V_{OH}	2.4			V	I_{OH} = −200 μA
Output low voltage	O_0–O_7	V_{OL}			0.4	V	I_{OL} = 1.6 mA
Input leakage current	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	$\|I_{LI}\|$			2	μA	V_{in} = 5.25 V/0.5 V
V_{CC} current		I_{CC}			30	mA	
V_{PP} current		I_{PP}			40	mA	

AC Characteristics

(V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25°C ± 5°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Address set-up time	t_{AS}	2			μs	Fig. 42 Input Pulse level: 0.8–2.2 V Input rise/fall time ≤ 20 ns Timing reference level { input: 1.0 V, 2.0 V { output: 0.8 V, 2.0 V
$\overline{OE}$ set-up time	t_{OES}	2			μs	
Data set-up time	t_{DS}	2			μs	
Address hold time	t_{AH}	0			μs	
Data hold time	t_{DH}	2			μs	
Output disable delay time	t_{DF}			130	ns	
V_{PP} set-up time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ pulse width when overprogramming	t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time	t_{VCS}	2			μs	
Data output delay time	t_{OE}	0		500	ns	

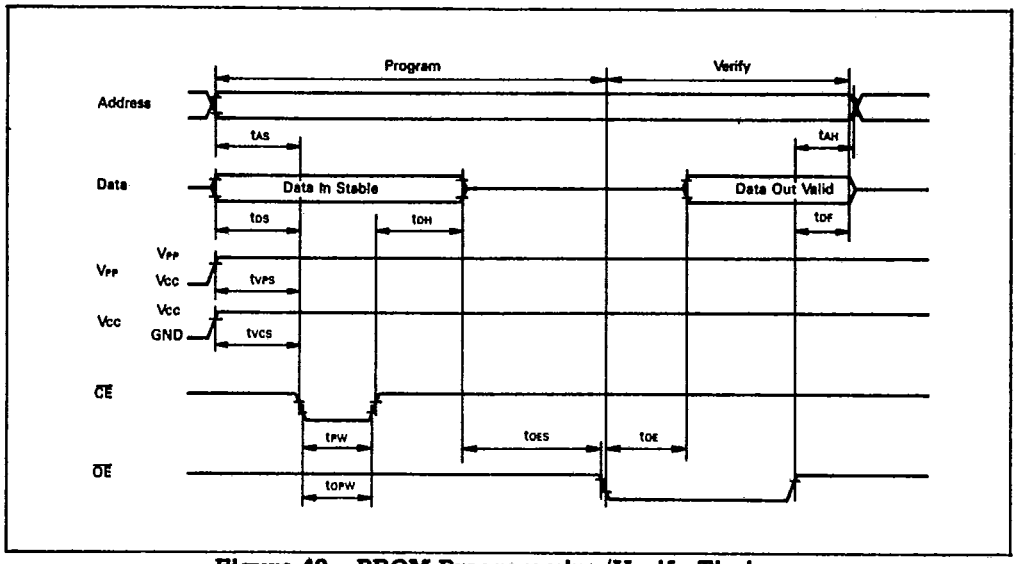


Figure 42. PROM Programming/Verify Timing

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Read Mode

DC Characteristics

(V_{CC} = 5 V ± 10%, V_{PP} = V_{CC} ± 0.6 V, T_a = 25°C ± 5°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Leakage Current	I_{LI}			1	μA	V_{CC} = 5.5 V, V_{in} = GND to V_{CC}
Output Leakage Current	I_{LO}			1	μA	V_{CC} = 5.5 V, V_{out} = GND to V_{CC}
Program Current	I_{PP}		1	100	μA	V_{PP} = V_{CC} + 0.6 V
Current Dissipation Active Mode	I_{CC}			30	mA	
Input Voltage	V_{IL}	−0.3		0.8	V	
	V_{IH}	2.2		V_{CC}+0.3	V	
Output Voltage	V_{OL}			0.40	V	I_{OL} = 1.6 mA
	V_{OH}	2.4			V	I_{OH} = −200 μA

AC Characteristics

(V_{CC} = 5 V ± 10%, V_{PP} = V_{CC} ± 0.6 V, T_a = 25°C ± 5°C, unless otherwise noted)

Item	Symbol	Min	Max	Unit	Test Condition	Note
Access Time	t_{ACC}		500	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	
$\overline{CE}$ Output Delay Time	t_{CE}		500	ns	$\overline{OE}$ = V_{IL}	
$\overline{OE}$ Output Delay Time	t_{OE}	10	150	ns	$\overline{CE}$ = V_{IL}	
Output Disable Delay Time	t_{DF}	0	105	ns	$\overline{CE}$ = V_{IL}	1
Data Output Hold Time	t_{OH}	0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	

Note: 1. t_{DF} is defined when output becomes open because output level cannot be defined.

Switching characteristics
Input Pulse Level 0.8 to 2.2 V
Input Rise/Fall Time ≦ 20 ns

Output Load 1TTL Gate + 100 pF
Input/Output Timing Reference Level Output: 1 V, 2 V
Input: 0.8 V, 2 V

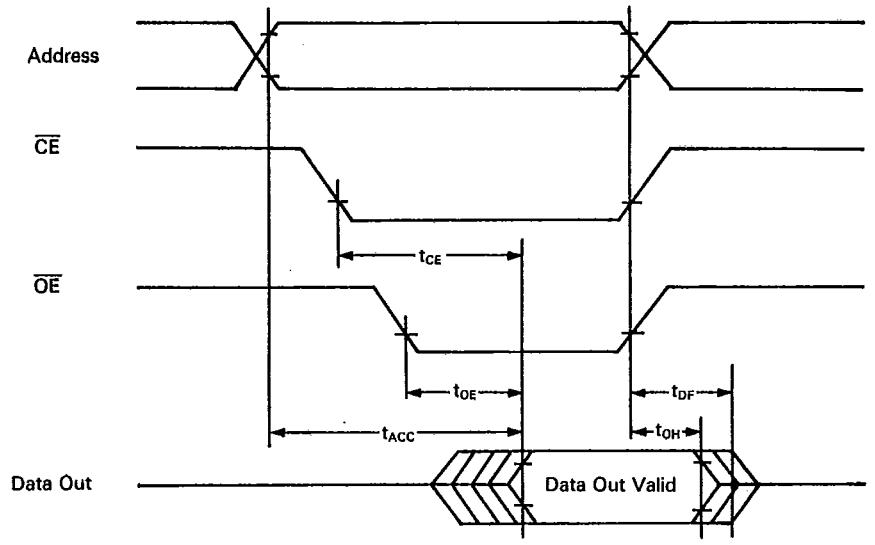

Figure 44. PROM Read Timing

HD404019
MASK OPTION LIST

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

* Please enter check marks in ☐ (■, x, ✓).

(1) I/O Option

Note (I/O options masked by ☒ are not available.)

PIN			INPUT/OUTPUT	I/O OPTION A	B	C	D	E
D_0		Standard Pins	Input/Output					
D_1			Input/Output					
D_2			Input/Output					
D_3			Input/Output					
D_4		High Voltage Pins	Input/Output					
D_5			Input/Output					
D_6			Input/Output					
D_7			Input/Output					
D_8			Input/Output					
D_9			Input/Output					
D_{10}			Input/Output					
D_{11}			Input/Output					
D_{12}			Input/Output					
D_{13}			Input/Output					
D_{14}			Input/Output					
D_{15}			Input/output					
$R0_0$	R0	High Voltage Pins	Input/Output					
$R0_1$			Input/Output					
$R0_2$			Input/Output					
$R0_3$			Input/Output					
$R1_0$	R1		Input/Output					
$R1_1$			Input/Output					
$R1_2$			Input/Output					
$R1_3$			Input/Output					
$R2_0$	R2		Input/Output					
$R2_1$			Input/Output					
$R2_2$			Input/Output					
$R2_3$			Input/Output					

PIN			INPUT/OUTPUT	I/O OPTION A	B	C	D	E
$R3_0$	R3	Standard Pins	Input/Output					
$R3_1$			Input/Output					
$R3_2$			Input/Output					
$R3_3$			Input/Output					
$R4_0$	R4		Input/Output					
$R4_1$			Input/Output					
$R4_2$			Input/Output					
$R4_3$			Input/Output					
$R5_0$	R5		Input/Output					
$R5_1$			Input/Output					
$R5_2$			Input/Output					
$R5_3$			Input/Output					
$R6_0$	R6		Input/Output					
$R6_1$			Input/Output					
$R6_2$			Input/Output					
$R6_3$			Input/Output					
$R7_0$	R7		Input/Output					
$R7_1$			Input/Output					
$R7_2$			Input/Output					
$R7_3$			Input/Output					
$R8_0$	R8		Input/Output					
$R8_1$			Input/Output					
$R8_2$			Input/Output					
$R8_3$			Input/Output					
$R9_0$	R9		Input					
$R9_1$			Input					
$R9_2$			Input					
$R9_3$			Input					
RA_0	RA	High Voltage Pin	Input					
RA_1			Input	Please Mark on RA_1/V_{disp}				

* Please enter "0" in applicable item for I/O option selection.
A; Without Pull-up MOS (NMOS Open Drain) B; With Pull-up MOS
C; CMOS (not be used as Input)
D; Without Pull-down MOS (PMOS Open Drain) E; With Pull-down MOS

HD404019/HD4074019

T-49-19-04

(2) RA_1/V_{disp}

RA_1/V_{disp}
☐ RA_1: Without Pull-down MOS (D)
☐ V_{disp}

* Please enter check marks (■, X, ✓) in applicable item.

(3) Package

Package
☐ DP-64S (shrink package)
☐ FP-64B

* Please enter check marks (■, X, ✓) in applicable item.

Note) RA_1/V_{disp} has to be selected as V_{disp} pin even if one high voltage pin is specified as "E".

(4) Divider (DIV)

Clock divide ratio
■ Divided-by-4

(5) ROM Code Media

ROM Code Media
☐ EPROM: Emulator Type
☐ EPROM: EPROM On-Package Microcomputer Type

Check List of Application

(A) Oscillator (CPG option)

CPG option	☐ Ceramic Filter
	☐ Crystal
	☐ External Clock

* Please enter check marks (■, X, ✓) in applicable item.