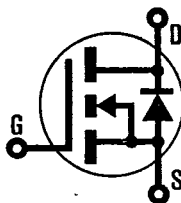




HEXFET® TRANSISTORS IRFF110

**N-CHANNEL
POWER MOSFETs
TO-39 PACKAGE**



IRFF111

IRFF112

IRFF113

100 Volt, 0.6 Ohm HEXFET®

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

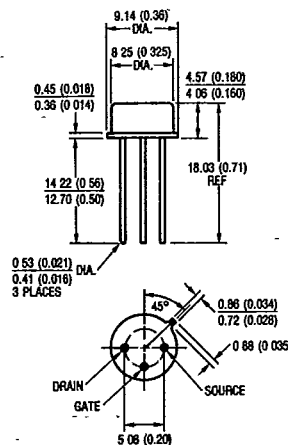
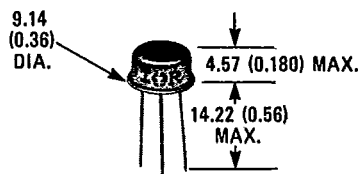
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability

Product Summary

Part Number	V _{DS}	R _{DS(on)}	I _D
IRFF110	100V	0.6Ω	3.5A
IRFF111	60V	0.6Ω	3.5A
IRFF112	100V	0.8Ω	3.0A
IRFF113	60V	0.8Ω	3.0A

CASE STYLE AND DIMENSIONS



Conforms to JEDEC Outline TO-205AF (TO-39)
Dimensions in Millimeters and (Inches)

IRFF110, IRFF111, IRFF112, IRFF113 Devices

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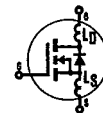
Absolute Maximum Ratings

Parameter	IRFF110	IRFF111	IRFF112	IRFF113	Units
V_{DS} Drain - Source Voltage ①	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM} Pulsed Drain Current ③	14	14	12	12	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	15 (See Fig. 14)				W
Linear Derating Factor	0.12 (See Fig. 14)				W/K ④
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
T_{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	IRFF110	100	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$
	IRFF112	—	—	—	V	
	IRFF111	60	—	—	V	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$
$I_{D(on)}$ On-State Drain Current ②	IRFF110	3.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, V_{GS} = 10\text{V}$
	IRFF111	—	—	—	A	
	IRFF112	3.0	—	—	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRFF110	—	0.5	0.6	Ω	$V_{GS} = 10\text{V}, I_D = 1.5\text{A}$
	IRFF111	—	—	—	Ω	
	IRFF112	—	0.6	0.8	Ω	
g_{fs} Forward Transconductance ②	ALL	1.0	1.5	—	S (U)	$V_{DS} > I_{D(on)} \times R_{DS(on) \text{ max.}}, I_D = 1.5\text{A}$
C_{iss} Input Capacitance	ALL	—	135	200	pF	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0 \text{ MHz}$ See Fig. 10
C_{oss} Output Capacitance	ALL	—	80	100	pF	
C_{rss} Reverse Transfer Capacitance	ALL	—	20	25	pF	$V_{DD} = 0.5 BV_{DSS}, I_D = 1.5\text{A}, Z_o = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
$t_{d(on)}$ Turn-On Delay Time	ALL	—	10	20	ns	
t_r Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	15	25	ns	
t_f Fall Time	ALL	—	10	20	ns	$V_{GS} = 10\text{V}, I_D = 8.0\text{A}, V_{DS} = 0.8 \text{ Max. Rating.}$ See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	
Q_{gs} Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	8.33	K/W ④	
R_{thJA} Junction-to-Ambient	ALL	—	—	175	K/W ④	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF110 IRFF111	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRFF112 IRFF113	—	—	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF110 IRFF111	—	—	14	A	
		IRFF112 IRFF113	—	—	12	A	
V_{SD}	Diode Forward Voltage ②	IRFF110 IRFF111	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 3.5\text{A}, V_{GS} = 0\text{V}$
		IRFF112 IRFF113	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 3.0\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	200	—	ns	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.0	—	μC	$T_J = 150^\circ\text{C}, I_F = 3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

④ $\text{K/W} = ^\circ\text{C/W}$
 $\text{W/K} = \text{W}/^\circ\text{C}$

③ Repetitive Rating: Pulse width limited by max. junction temperature.
See Transient Thermal Impedance Curve (Fig. 5).

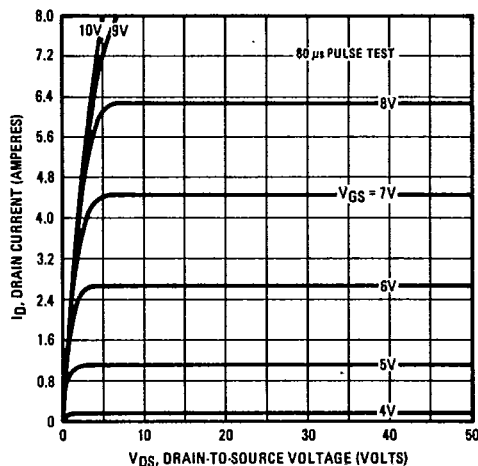


Fig. 1 — Typical Output Characteristics

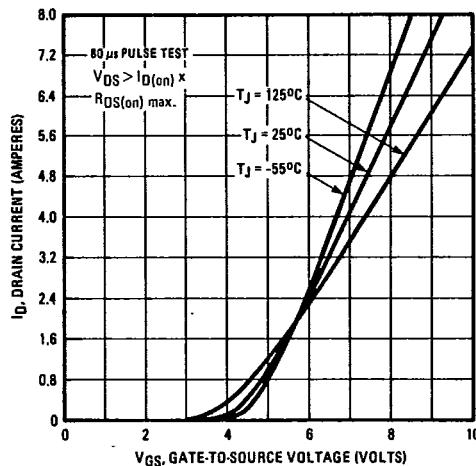


Fig. 2 — Typical Transfer Characteristics

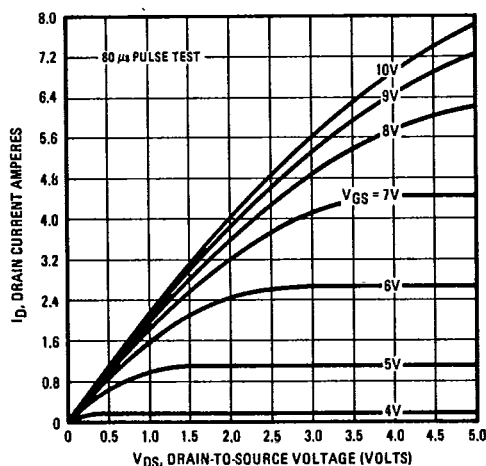


Fig. 3 — Typical Saturation Characteristics

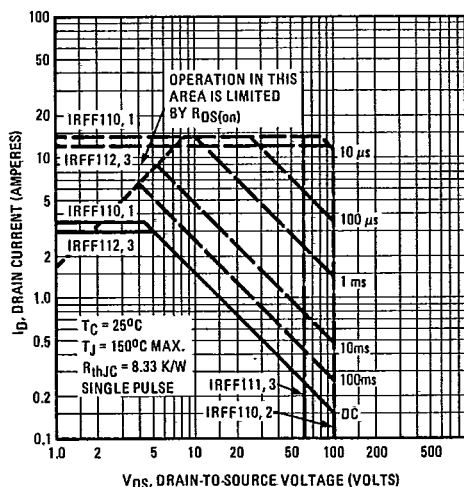


Fig. 4 — Maximum Safe Operating Area

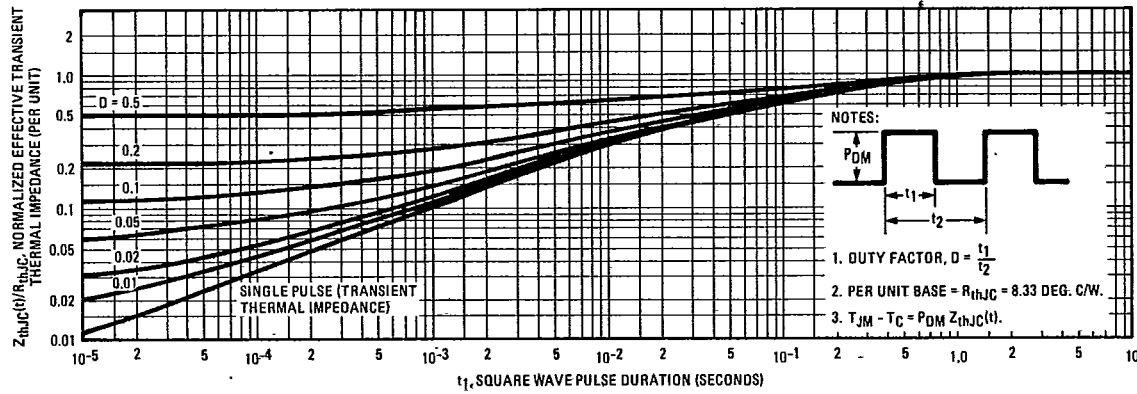


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

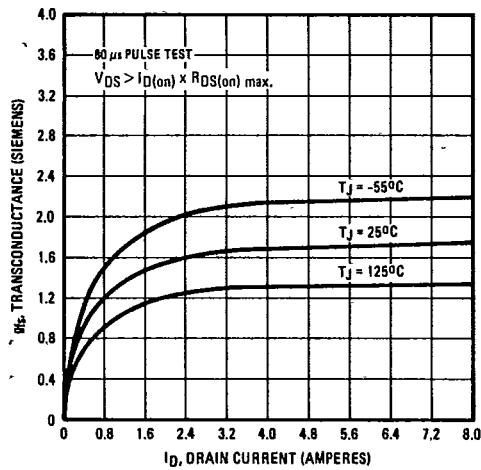


Fig. 6 - Typical Transconductance Vs. Drain Current

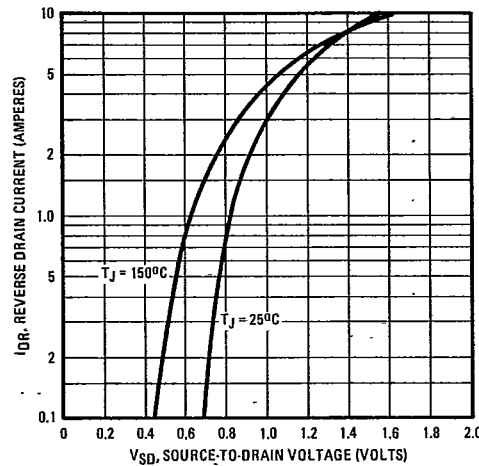


Fig. 7 - Typical Source-Drain Diode Forward Voltage

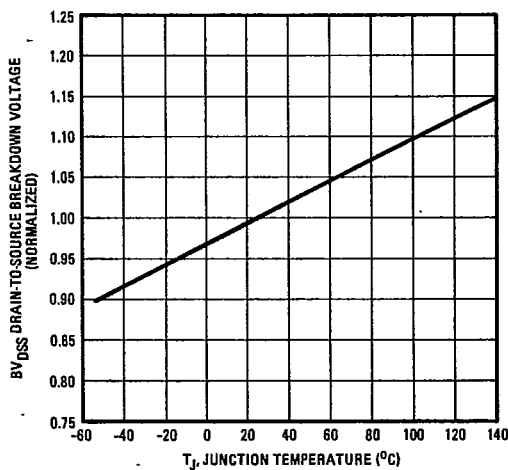


Fig. 8 - Breakdown Voltage Vs. Temperature

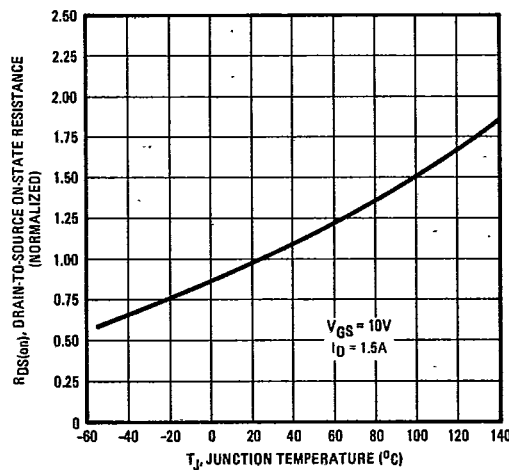


Fig. 9 - Normalized On-Resistance Vs. Temperature

IRFF110, IRFF111, IRFF112, IRFF113 Devices

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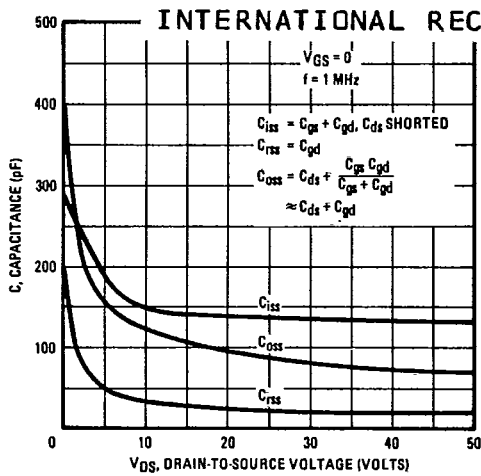


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

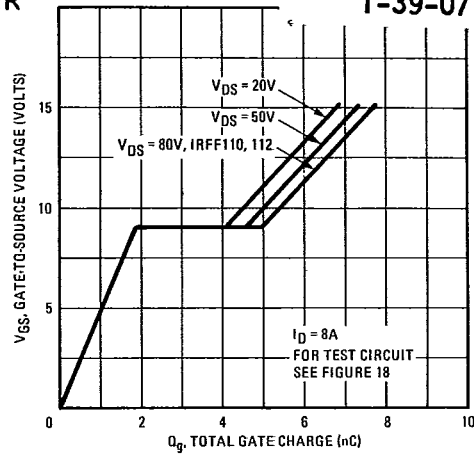


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

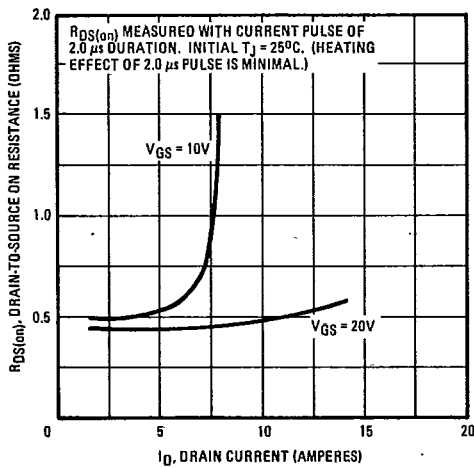


Fig. 12 - Typical On-Resistance Vs. Drain Current

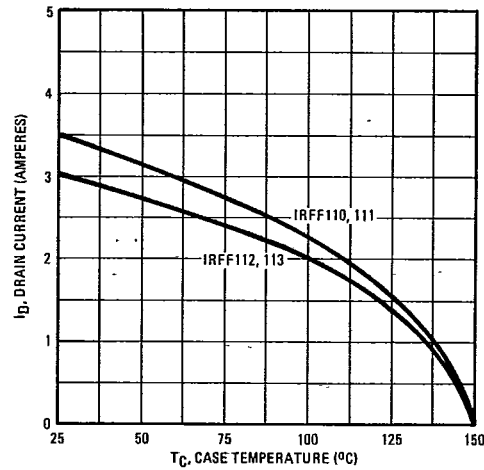


Fig. 13 - Maximum Drain Current Vs. Case Temperature

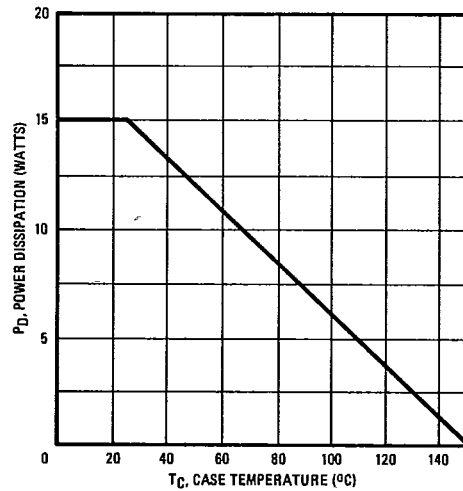


Fig. 14 - Power Vs. Temperature Derating Curve

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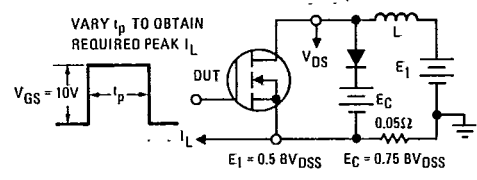


Fig. 15 - Clamped Inductive Test Circuit

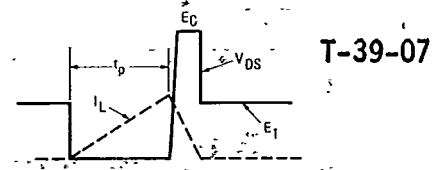


Fig. 16 - Clamped Inductive Waveforms

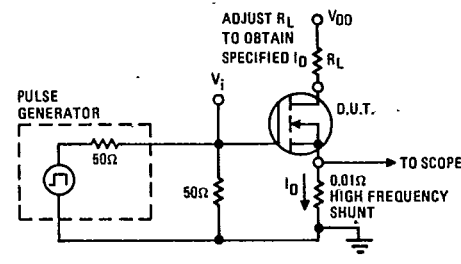


Fig. 17 - Switching Time Test Circuit

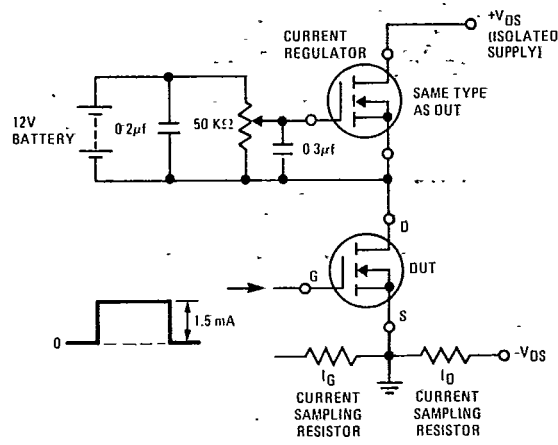
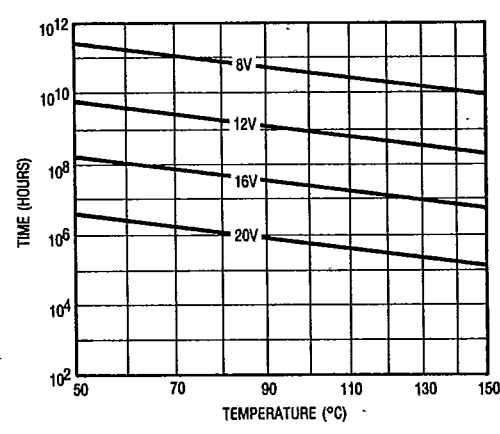


Fig. 18 - Gate Charge Test Circuit



*Fig. 19 - Typical Time to Accumulated 1% Gate Failure

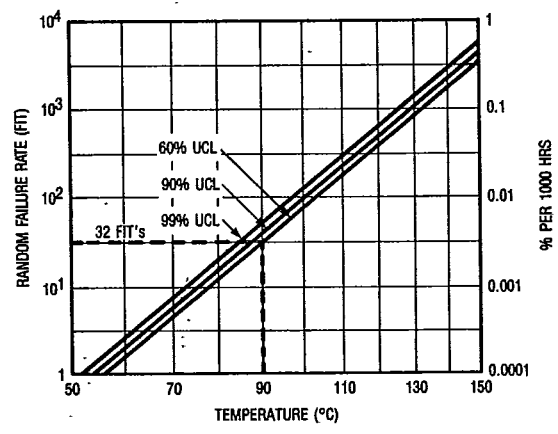


Fig. 20 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.