Advance Information

MPC755CE/D
Rev. 2, 6/2002

MPC755 RISC Microprocessor Chip Errata

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This document details all known silicon errata for the MPC755 and MPC745. Table 1 provides a revision history for this chip errata document.

Table 1. Document Revision History

Document Revision	Significant Changes
Revs. 0–1	Earlier releases of document
Rev. 2	Added Errors 6 and 7

Table 2 describes the devices to which the errata in this document apply and provides a cross-reference to match the revision code in the processor version register to the revision level marked on the part.

Table 2. Revision Level to Part Marking Cross-Reference

MPC755 Revision	Part Marking	Processor Version Register
1.0		0008 3100
1.1		0008 3101
2.0		0008 3200
2.7	D	0008 3202
2.8	E	0008 3203

Table 3 summarizes all known errata and lists the corresponding silicon revision level to which it applies. A ‘Y’ entry indicates the erratum applies to a particular revision level, while a ‘—’ entry means it does not apply.

Table 3. Summary of Silicon Errata and Applicable Revision

No.	Problem	Description	Impact	Work Around	Present in Version:		
					1.0	1.1	2.*x*
1	VOLTDET in 360 BGA connected to V_{DD}	The VOLTDET is connected to V_{DD} rather than $L2OV_{DD}$ in the 360 BGA package.	Cannot use this signal to set voltage reference for SRAM I/O (if required).	Use alternative reference.	Y	Y	N
2	L2ZZ pin incorrectly active low	The L2ZZ pin in PB2 mode is incorrectly made an active low signal.	Cannot use this feature to put the SRAMs into a ZZ power saving mode.	Do not connect the L2ZZ pin to the SRAM.	Y	N	N
3	System bus inoperable in PLL bypass mode.	In PLL bypass mode, incorrect data may be sampled from the system bus interface.	Cannot run the processor at system bus speeds.	None exists.	Y	Y	N
4	Additional BAT registers non-functional	Hits in the added BAT registers may not disable TLB interactions.	New feature.	Use the standard 4 IBAT and 4 DBAT registers only.	Y	Y	N
5	L2ZZ pin always low	The L2ZZ pin was tied low as a workaround for errata 2.	PB2: Cannot use this feature to put the SRAMs into a ZZ power mode during sleep. PB3: Cannot use as $\overline{ADS}$ pin for this type of SRAM.	PB2: Use L2CR clock stop bit for same low power. PB3: None exists.	N	Y	N
6	L2 address parity does not work.	Incorrect parity may be generated when writing a cache line to the L2, causing a subsequent parity error when the cache line is read.	L2 address parity cannot be used.	None	Y	Y	Y
7	Single-beat, cache-inhibited stores discarded in L2 test mode.	Single-beat, cache-inhibited stores are discarded and do not propagate to the system bus when L2 test support mode is enabled.	Systems requiring the ability to perform single-beat cache-inhibited stores while in L2 test mode may experience memory corruption or system hangs.	1. Use Private Memory mode to test L2 cache. OR 2. Configure cache-inhibited space as write-through (WIMG=11xx) if transactions must propagate to system bus	Y	Y	Y

Error No. 1: VOLTDET in 360 BGA package connected to V_{DD}

Overview:

The VOLTDET signal is connected to V_{DD} rather than $L2OV_{DD}$ in the 360 BGA package.

Detailed Description:

The VOLTDET signal of the MPC755 (360 BGA) is intended to indicate the voltage level present at the L2 cache interface as a reference for SRAM I/O. In affected devices, however, this signal is internally connected to V_{DD} rather than $L2OV_{DD}$.

Projected Impact:

This signal cannot be used to set the voltage reference for SRAM I/O (if required).

Work Arounds:

An alternative reference may be used.

Projected Solution:

Fixed in MPC755 Rev. 2.0

Error No. 2: L2ZZ pin incorrectly active low

Overview:

The L2ZZ pin in PB2 mode is incorrectly made an active low signal.

Detailed Description:

The L2ZZ pin should be an active high output used to enable low-power mode for L2 memory devices supporting this feature. In affected devices, however, this signal is erroneously an active low output.

Projected Impact:

Cannot use this feature to put the SRAMs into a power-saving mode.

Work Around:

Do not use low-power mode feature of SRAM.

Projected Solution:

Fixed in MPC755 Rev. 1.1

Error No. 3: System bus inoperable in PLL bypass mode.

Overview:

In PLL bypass mode, the system bus may be inoperable.

Detailed Description:

In PLL-bypass mode, incorrect data may be captured from 60x bus interface, causing processor hangs and data corruption.

Projected Impact:

Cannot operate in PLL bypass mode.

Work Arounds:

None

Projected Solution:

Fixed in MPC755 Rev. 2.0

Error No. 4: Additional BAT registers non-functional

Overview:

Hits in the added BAT registers may not disable TLB interactions.

Detailed Description:

During address translation, BAT registers are checked first. If an effective address hits in a BAT, the TLB should be ignored. In affected devices, however, an effective address that hits in one of the additional BAT registers will still propagate to the TLB, causing incorrect device behavior.

Projected Impact:

Additional BAT registers cannot be used.

Work Arounds:

Use the standard 4 IBAT and 4 DBAT registers only.

Projected Solution:

Fixed in MPC755 Rev. 2.0

Error No. 5: L2ZZ pin always low

Overview:

The L2ZZ pin is internally tied low.

Detailed Description:

The L2ZZ pin should be an active high output used to enable low-power mode for L2 memory devices supporting this feature. In affected devices, however, this signal is erroneously tied low.

Projected Impact:

PB2: Cannot use this feature to put the SRAMs into a low-power mode during sleep.

PB3: Cannot use as ADS pin for this type of SRAM.

Work Arounds:

None

Projected Solution:

Fixed in MPC755 Rev. 2.0

Error No. 6: L2 address parity does not work

Overview:

L2 address parity generation does not work correctly.

Detailed Description:

Incorrect parity may be generated when writing a cache line to the L2 cache. Because the correct algorithm is used when checking parity for a read, a parity error occurs when the cache line is subsequently read.

Projected Impact:

L2 address parity cannot be used.

Work Arounds:

None

Projected Solution:

Under review

Error No. 7: Single-beat, cache-inhibited stores discarded in L2 test mode.

Overview:

Single-beat, cache-inhibited stores are discarded when L2CR[L2TS] is set.

Detailed Description:

Single-beat, cache-inhibited stores are discarded and do not propagate to the system bus when L2 test support mode is enabled.

Projected Impact:

Systems requiring the ability to perform single-beat cache-inhibited stores while in L2 test mode may experience memory corruption or system hangs.

Work Around:

1. Use Private Memory mode to test the L2 cache.

OR

2. Configure cache-inhibited space as write-through (WIMG=11xx) if transactions must propagate to system bus while in L2 test support mode. These settings are not defined in the architecture but are useful to overcome this erratum.

Projected Solution:

Under review

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