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T-46-19-13

Advanced Micro Devices

PAL22V10-7

7.5 ns 24-Pin TTL Versatile PAL® Device

DISTINCTIVE CHARACTERISTICS

- 7.5 ns propagation delay and 91 MHz f_{MAX}
- 10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Extensive third-party software and programmer support through FusionPLD℠ partners
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

GENERAL DESCRIPTION

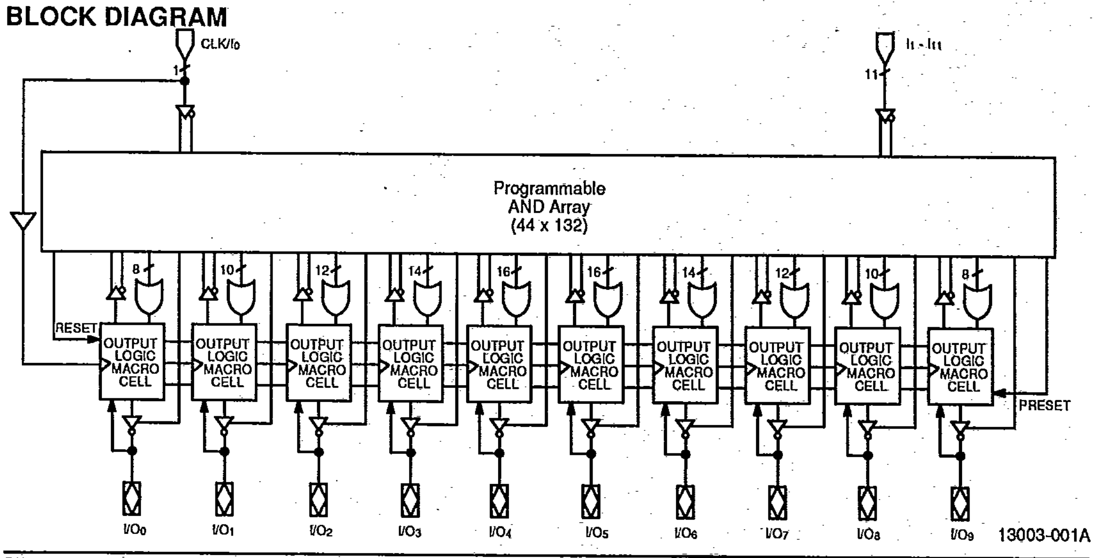
The PAL22V10-7 is a high-speed version of the popular PAL22V10 programmable logic device. With a 7.5 ns maximum propagation delay time and 91 MHz maximum frequency, the PAL22V10-7 is ideal for high-performance applications. The PAL22V10-7 is pin-compatible with the other PAL22V10 devices.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram.) The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two fuses controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PAL22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. See page 15 for certified development systems, and page 17 for approved programmers.

BLOCK DIAGRAM



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Publication# 16102 Rev. B Amendment/0
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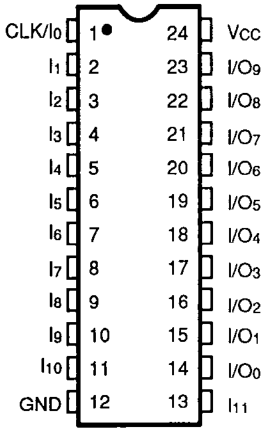
CONNECTION DIAGRAMS
Top View

SKINNYDIP



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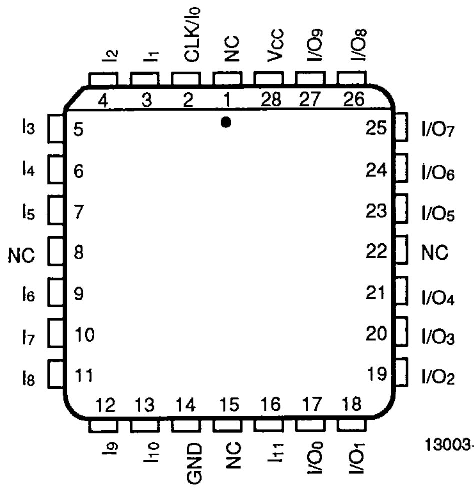
PLCC



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Note:
Pin 1 is marked for orientation.

PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
V_{CC}	Supply Voltage

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ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

PAL 22 V 10 -7 P C

FAMILY TYPE
PAL = Programmable Array Logic

NUMBER OF ARRAY INPUTS

OUTPUT TYPE
V = Versatile

NUMBER OF OUTPUTS

SPEED
-7 = 7.5 ns t_{PD}

PACKAGE TYPE
P = 24-Pin 300-mil Plastic SKINNYDIP (PD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

OPTIONAL PROCESSING
Blank = Standard Processing

Valid Combinations	
PAL22V10-7	PC, JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PAL22V10 utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The device provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL22V10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PAL22V10 has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls initially are connected to ground (0) through a programmable fuse, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

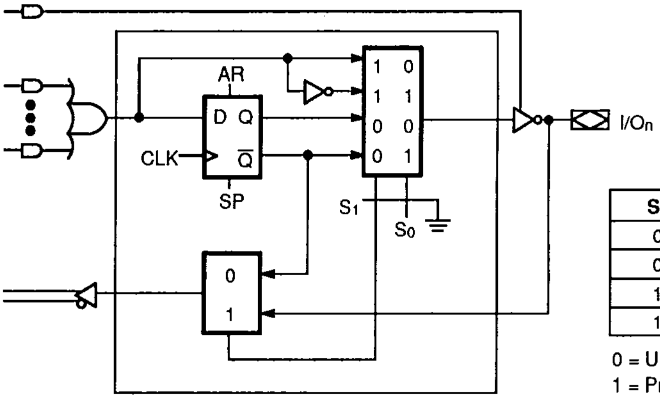
The PAL22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Registered Output Configuration

Each macrocell of the PAL22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Unprogrammed fuse
1 = Programmed fuse

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Figure 1. Output Logic Macrocell Diagram

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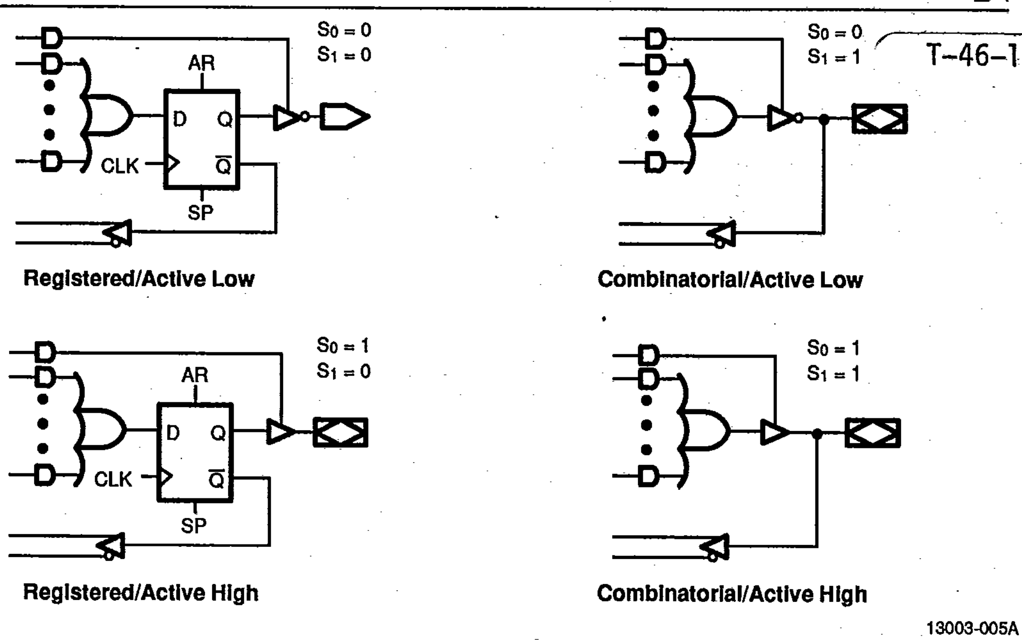

Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions.

Preset/Reset

For initialization, the PAL22V10 has Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum. Details on power-up reset can be found on page 14.

Register Preload

The register on the PAL22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL22V10 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed, and preload will be disabled.

Quality and Testability

The PAL22V10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

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Technology

The PAL22V10 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven TiW fuses for reliable operation.

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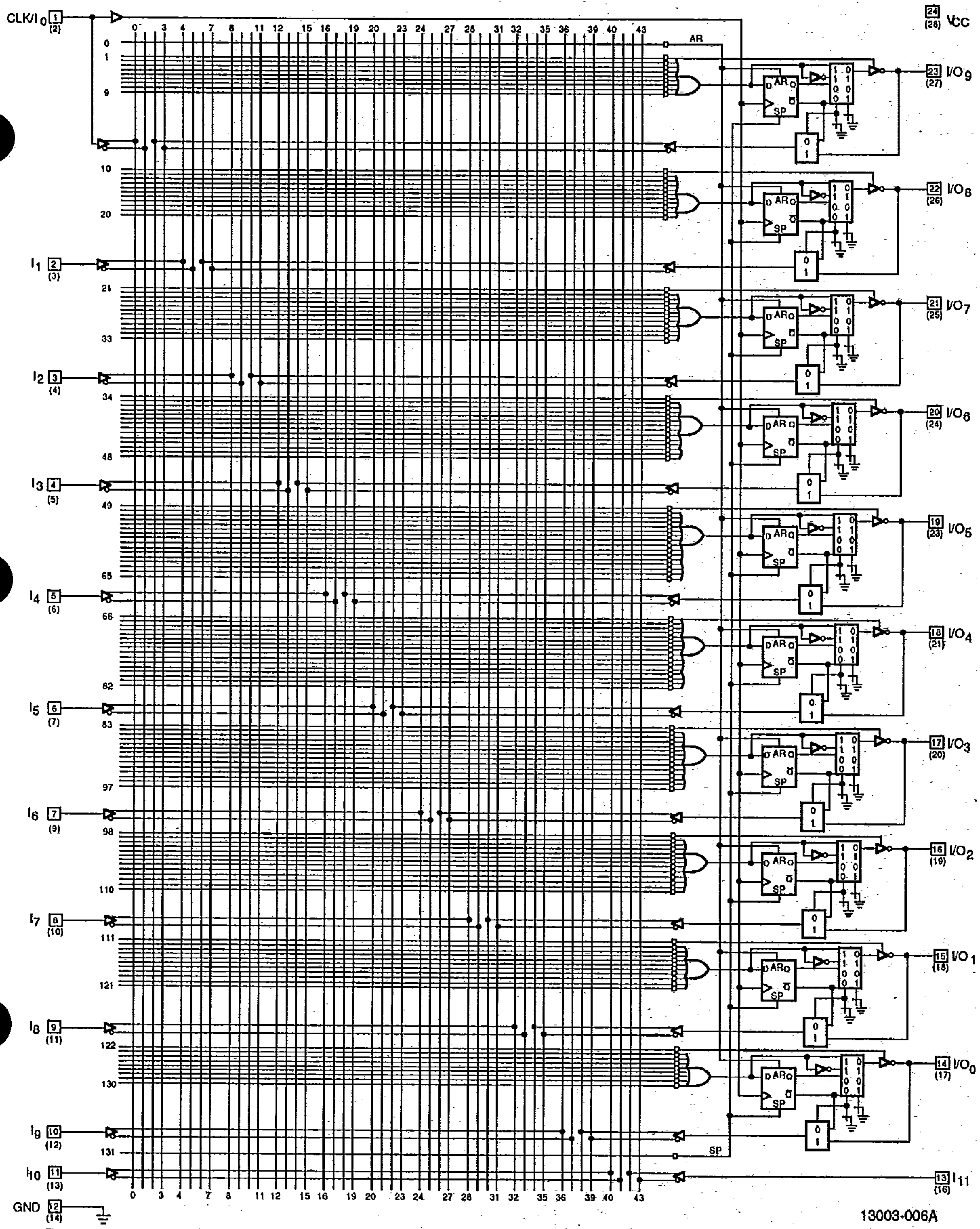
LOGIC DIAGRAM
SKINNYDIP (PLCC/LCC) Pinouts



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

T-46-19-13

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.			−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			−100	µA
			CLK		−150	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.			220	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		5	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	7.5	ns
t_S	Setup Time from Input, Feedback or SP to Clock			5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	6	ns
t_{AR}	Asynchronous Reset to Registered Output				12	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			5		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	91		MHz
		Internal Feedback (f_{CNT})		110		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				8	ns
t_{ER}	Input to Output Disable Using Product Term Control				7.5	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

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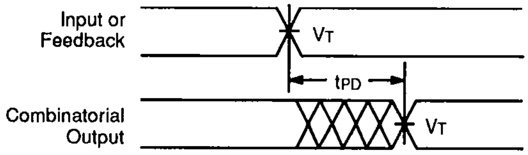
SWITCHING WAVEFORMS



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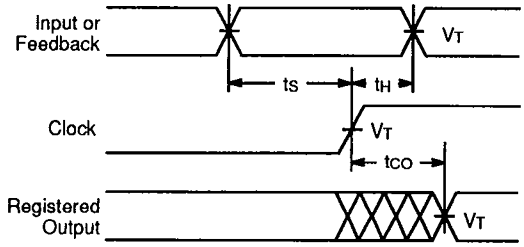
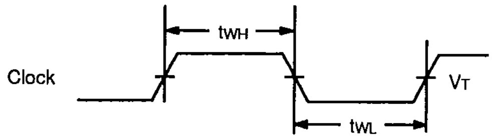
Combinatorial Output



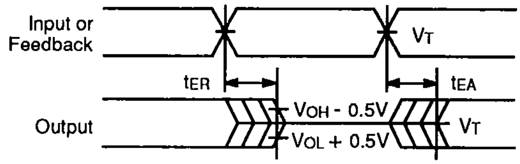
13003-011B

Registered Output



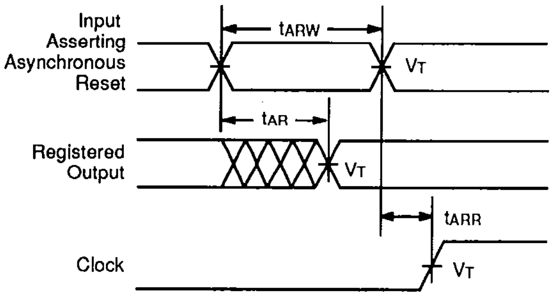
13003-009B

Clock Width



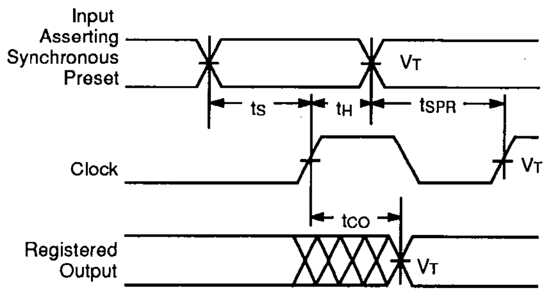
13003-013B

Input to Output Disable/Enable



13003-010B

Asynchronous Reset



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Synchronous Preset

Notes:

1. $V_T = 1.5$ V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–4 ns typical.

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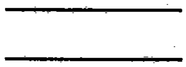
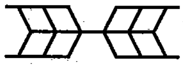
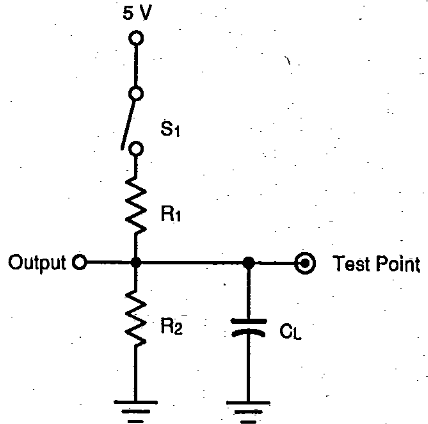
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



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Specification	S1	CL	Commercial R1	Commercial R2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	300 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5 V L → Z: V_{OL} + 0.5 V

f_{MAX} Parameters

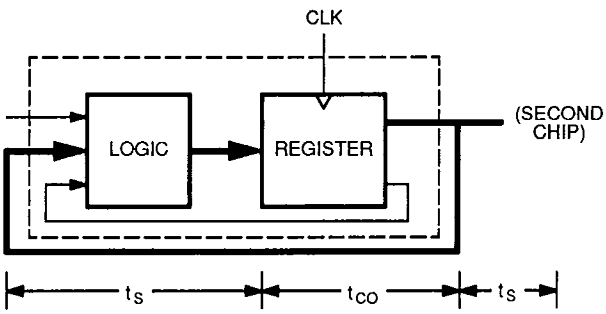
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external".

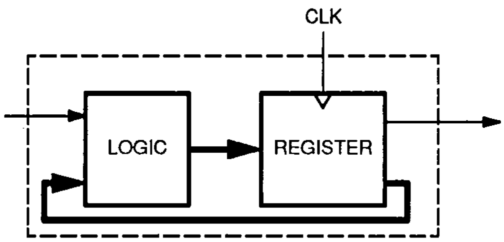
The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design, therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback".

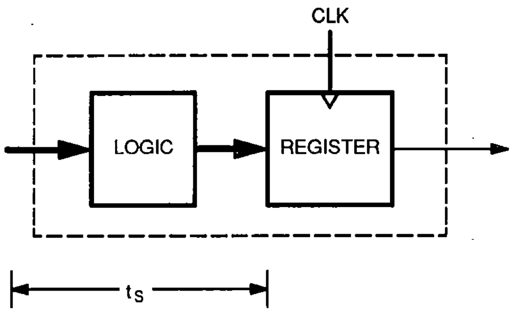
f_{MAX} external and f_{MAX} no feedback are calculated parameters. f_{MAX} external is calculated from t_S and t_{CO}, and f_{MAX} no feedback is calculated from t_{WL} and t_{WH}. f_{MAX} internal is measured.



f_{MAX} External; $1/(t_S + t_{CO})$



f_{MAX} Internal (f_{CNT})



f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

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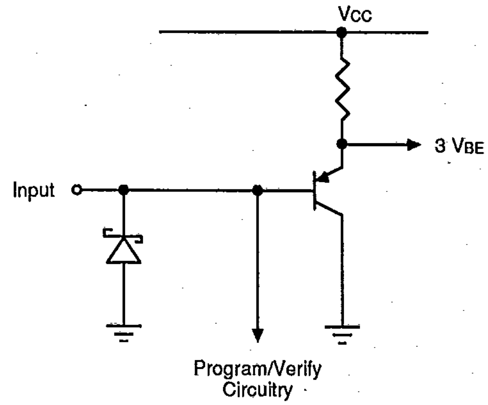
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



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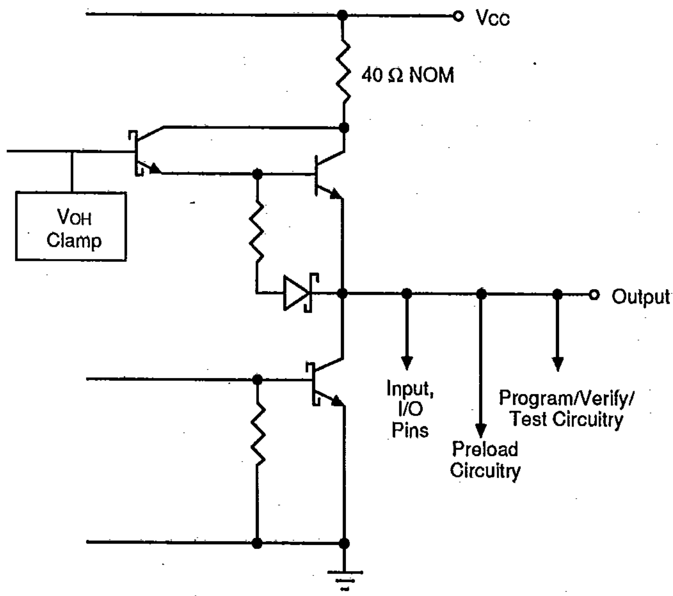
Typical Output



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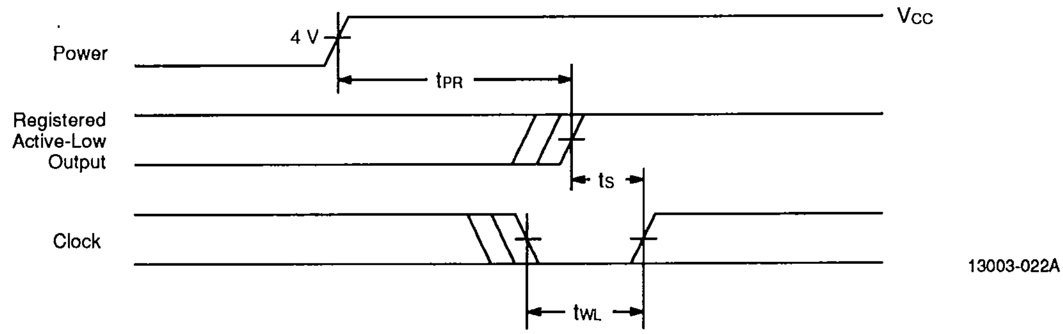
POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

MANUFACTURER	COMPILERS
Advanced Micro Devices, Inc. 901 Thompson Place MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	PALASM® Software Rev. 2.2 or later
Cadence (Valid) Design Systems, Inc. 555 River Oaks Parkway San Jose, CA 95134 (408) 943-1234	Composer™ PLD Option SystemPLD™
Capilano Computing Systems, Ltd. 960 Quayside Dr., Suite 406 New Westminster, B.C. Canada V3M 6G2 (800) 444-9064 or (604) 522-6200	MacABEL™ Software
Data I/O 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™-4 Software Rev. 2.0 or later Contact Data I/O
ISDATA GmbH Daimlerstr. 51 D-7500 Karlsruhe 21 Germany 0721/75 10 87 or (408) 373-7359 (U.S.)	LOG/iC™ Software
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Software
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155	PLDesigner® Software
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Programmable Logic Design Tools
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 422-4660 or (508) 480-0881	ViewPLD Synthesis Contact Viewlogic
MANUFACTURER	**SCHEMATIC EDITORS AND LIBRARIES**
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Schematic Design Tools
Data I/O 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 322-8246 or (206) 881-6444	FutureNet® Schematic Designer

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

MANUFACTURER	SIMULATORS
ALDEC Company, Inc. 3525 Old Conejo Rd., Suite 111 Newbury Park, CA 91320 (805) 499-6867	SUSIE™
Cadence (Valid) Design Systems, Inc. 555 River Oaks Parkway San Jose, CA 95134 (408) 943-1234	RapidSIM™
iNt GmbH Bunsenstrasse 6 D-8033 Martinsreid/Munich Germany (89) 857-6667	PLDlab90/PLDsim90
Logic Automation Inc. 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690-6900	SmartModel® Libraries
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Digital Simulation Tools
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 422-4660 or (508) 480-0881	Viewsim/SD™
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Software
Data I/O 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	PLDtest™ Plus Software
iNt GmbH Bunsenstrasse 6 D-8033 Martinsreid/Munich Germany (89) 857-6667	PLDlab90/PLDcheck90

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APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

Manufacturer	Programmer Configuration
Advanced Micro Devices, Inc. 901 Thompson Pl. Sunnyvale, CA 94088 (800) 222-9323 or (408) 732-2400	LabPro™ Rev. 1.0
Advin Systems, Inc. 1050-L East Duane Avenue Sunnyvale, CA 94086 (408) 243-7000	U40 Rev. 10.10 U84 Rev. 10.10
BP Microsystems 10681 Haddington, Suite #190 Houston, TX 77043 (800) 225-2102 or (713) 461-9430	PLD-1128 Rev. 1.47F
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	UniSite™ DIP: Rev. 2.0 PLCC: Rev. 2.0 Model 2900 Rev. 1.10 System 29A, 29B LogicPak™ 303A-V04 Adapter 303A-011A/B-V01 Adapter 3033A-011B-V03 Model 60 DIP: Rev. V03 PLCC: Rev. V12 Family/Pinout Codes: 97-28
Digelec, Inc. 20144 Plummer St. Chatsworth, CA 91311 (800) 367-8750 or (818) 701-9677 or 25 Galgaley Haplada St. Herzliya B46722, Israel 52-55-9615	Model 860 Rev. A1.2
Logical Devices, Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	ALLPRO™ Rev. 2.1
SMS North America, Inc. 16552 NE 135th Pl. Redmond, WA 98052 (800) 331-7766 or (206) 883-8447 or SMS Im Morgental 13 D-8994 Hergatz, Germany 07522-5018	Sprint-Plus Rev. 3.21 Expert Rev. 3.21

Note:

The PAL22V10-7 utilizes the PAL22V10-10 programming algorithm.

APPROVED PROGRAMMERS (Continued) (subject to change)

Manufacturer	Programmer Configuration
Micropross Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq, France (20) 47.90.40	ROM 3000 Rev. 5.83
Stag Microsystems 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire UK AL7 1JT 707-332148	ZL30 Rev. 30A31 PPZ Module Zm2200 Rev. 35 Family/Pinout Code: 91070
System General Corp. 244 S. Hillview Dr. Milpitas, CA 95035 (408) 263-6667 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Rd., Shin Diau Taipei, Taiwan 2-917-3005	SGUP-85 Rev. 4.30

Note:
The PAL22V10-7 utilizes the PAL22V10-10 programming algorithm.