Data Sheet July 1999 File Number 2270.3

## 25A, 50V, 0.047 Ohm, Logic Level, N-Channel Power MOSFET

The RFP25N05L is an N-Channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. The RFP25N05L was designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA09871.

## Ordering Information

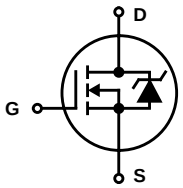
| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| RFP25N05L | TO-220AB | RFP25N05L |

NOTE: When ordering, include the entire part number.

## Features

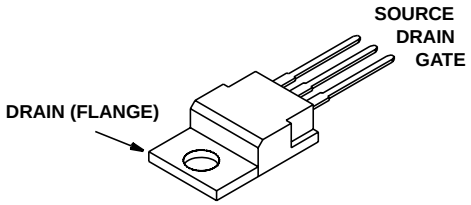
- 25A, 50V
- $r_{DS(ON)} = 0.047\Omega$
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

## Symbol




## Packaging

JEDEC TO-220AB



## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | RFP25N05L | UNITS |
|---|---|---|---|
| Drain to Source Voltage (Note 1) | $V_{DS}$ | 50 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) (Note 1) | $V_{DGR}$ | 50 | V |
| Continuous Drain Current | $I_D$ | 25 | A |
| Pulsed Drain Current (Note 3) | $I_{DM}$ | 65 | A |
| Single Pulse Avalanche Energy Rating (See Figures 4, 15, and 16) | | Refer to UIS SOA Curve | |
| Gate to Source Voltage | $V_{GS}$ | ±10 | V |
| Maximum Power Dissipation | $P_D$ | 60 | W |
| Linear Derating Factor above $25^oC$ | | 0.48 | $W/^oC$ |
| Operating and Storage Temperature | $T_J$, $T_{STG}$ | -55 to 150 | $^oC$ |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | $^oC$ |
| Package Body for 10s, See Techbrief 334 | $T_{pkg}$ | 260 | $^oC$ |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $T_J = 25^oC$ to $125^oC$.

## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250µA (Figure 10) | | 50 | - | - | V |
| Gate to Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250µA (Figure 9) | | 1.0 | - | 2.0 | V |
| Gate to Source Leakage | $I_{GSS}$ | $V_{GS}$ = ±10V, $V_{DS}$ = 0V | | - | - | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 40V, $V_{GS}$ = 0V | | - | - | 1.0 | µA |
| | | $T_C = 150^oC$ | | - | - | 50 | µA |
| Drain to Source On Resistance (Note 2) | $r_{DS(ON)}$ | $V_{GS}$ = 5V, $I_D$ = 25A | (Figures 7, 8) | - | - | 0.047 | Ω |
| | | $V_{GS}$ = 4V, $I_D$ = 25A | | - | - | 0.056 | Ω |
| Turn-On Time | $t_{(ON)}$ | $V_{DD}$ = 25V, $I_D$ =12.5A<br>$R_L$ = 2Ω, $R_{GS}$ = 5Ω<br>(Figures 15, 16) | | - | - | 60 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 15 | - | ns |
| Rise Time | $t_r$ | | | - | 35 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 40 | - | ns |
| Fall Time | $t_f$ | | | - | 14 | - | ns |
| Turn-Off Time | $t_{(OFF)}$ | | | - | - | 100 | ns |
| Total Gate Charge<br>(Gate to Source + Gate to Drain) | $Q_{g(TOT)}$ | $V_{GS}$ = 0 - 10V | $V_{DD}$ = 40V, $I_D$ = 25A,<br>$R_L$ = 1.6Ω<br>(Figures 17, 18) | - | - | 80 | nC |
| Gate Charge at 5V | $Q_{g(5)}$ | $V_{GS}$ = 0 - 5V | | - | - | 45 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS}$ = 0 - 1V | | - | - | 3.0 | nC |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | | | - | - | 2.083 | $^oC/W$ |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | | | - | - | 80 | $^oC/W$ |

## Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Source to Drain Diode Voltage | $V_{SD}$ | $I_{SD}$ = 25A | - | - | 1.5 | V |
| Diode Reverse Recovery Time | $t_{rr}$ | $I_{SD}$ = 25A, $dI_{SD}/dt$ = 100A/µs | - | - | 125 | ns |

NOTES:

2. Pulse Test: Pulse width ≤ 80µs, duty cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by Max junction temperature.

## Typical Performance Curves Unless Otherwise Specified

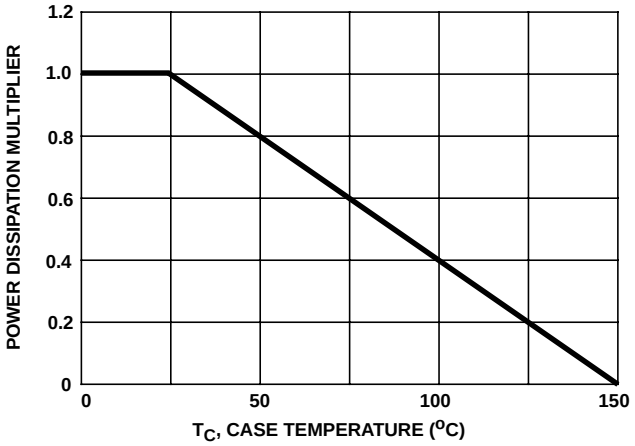



FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

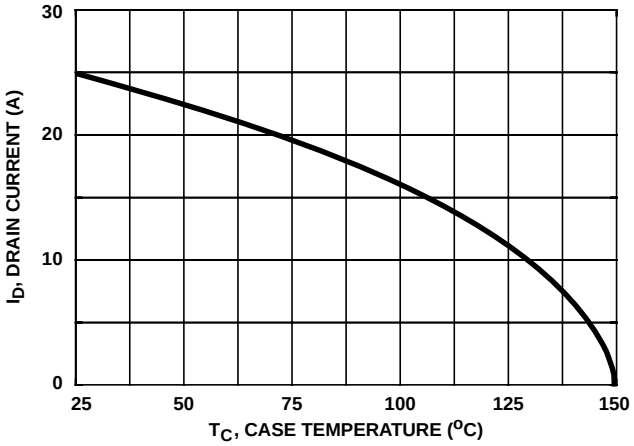



FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

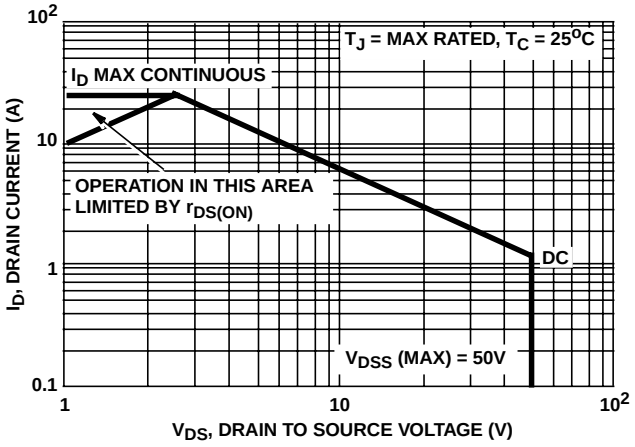



FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

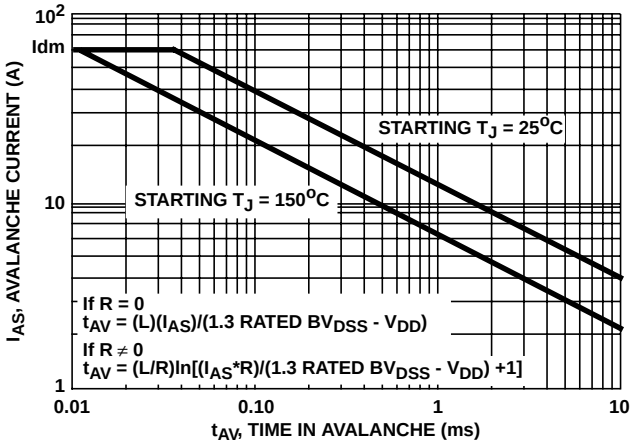



FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING SOA (SINGLE PULSE UIS SOA)

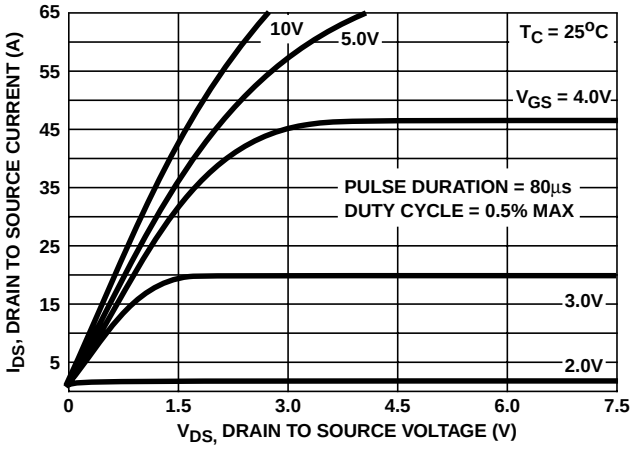



FIGURE 5. SATURATION CHARACTERISTICS

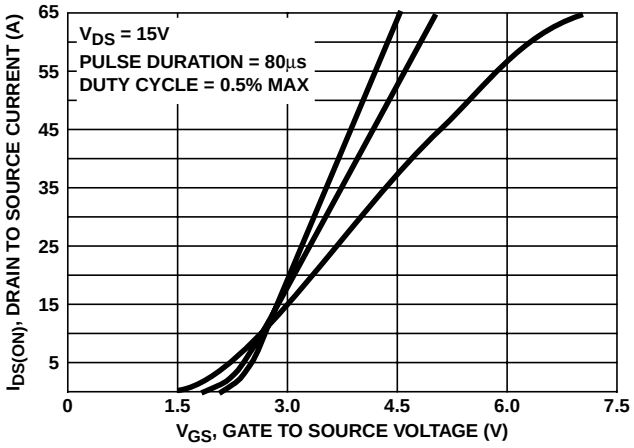



FIGURE 6. TRANSFER CHARACTERISTICS

## Typical Performance Curves Unless Otherwise Specified (Continued)

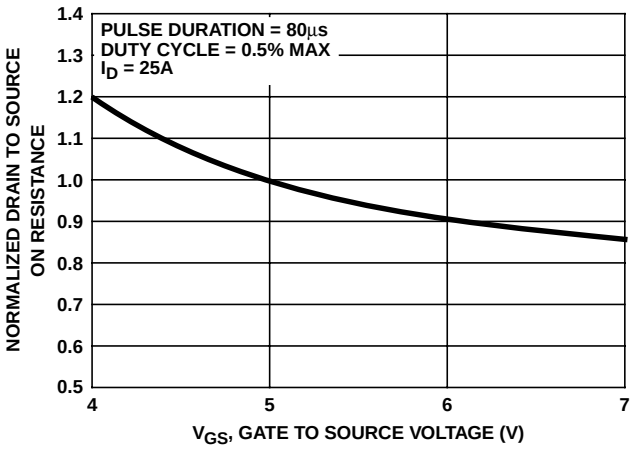



FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

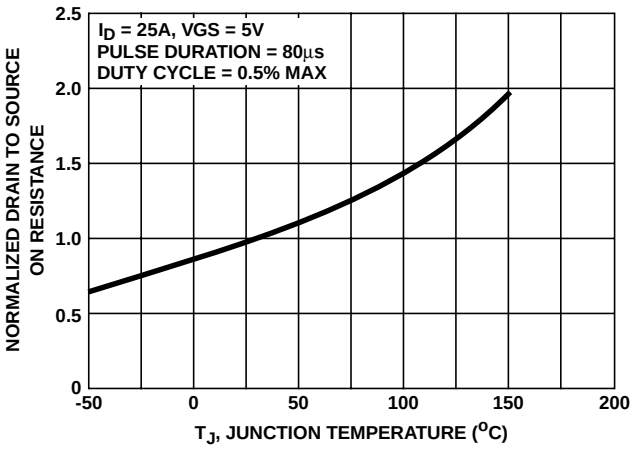



FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

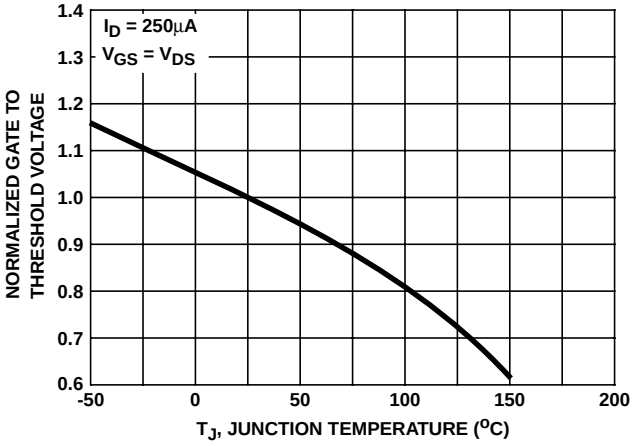



FIGURE 9. NORMALIZED GATE TO THRESHOLD vs JUNCTION TEMPERATURE

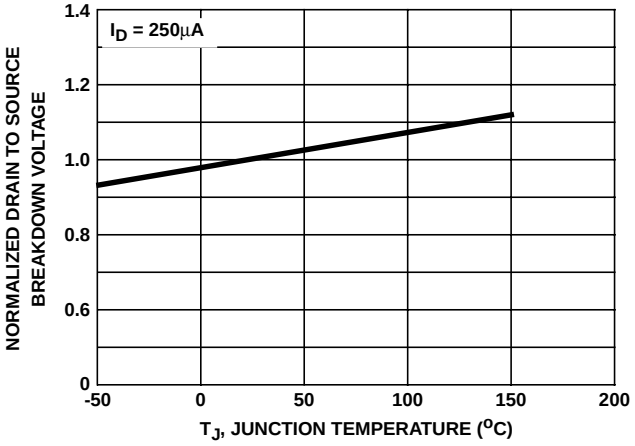



FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

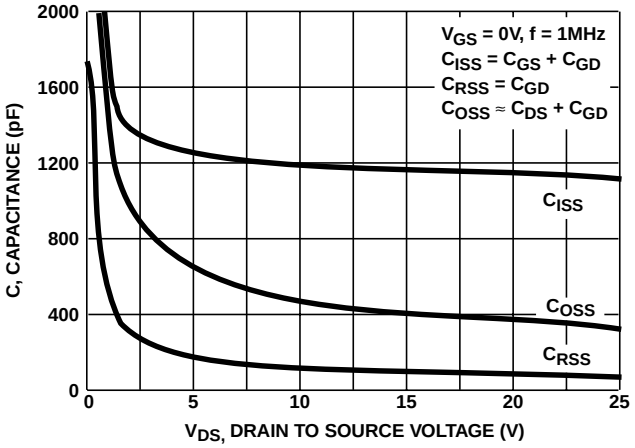
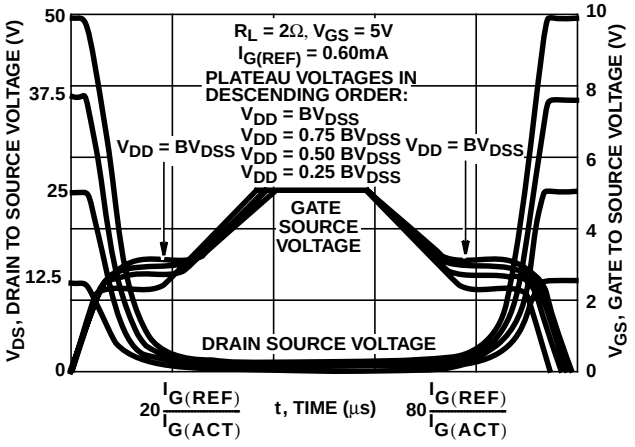



FIGURE 11. CAPACITANCE vs VOLTAGE




NOTE: Refer to Intersil Application Notes AN7254 and AN7260

FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

## Test Circuits and Waveforms

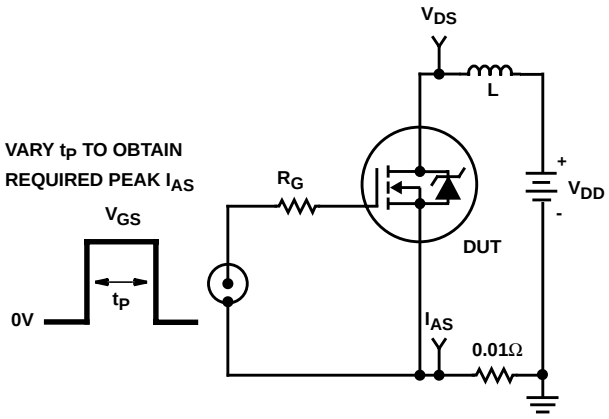



FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

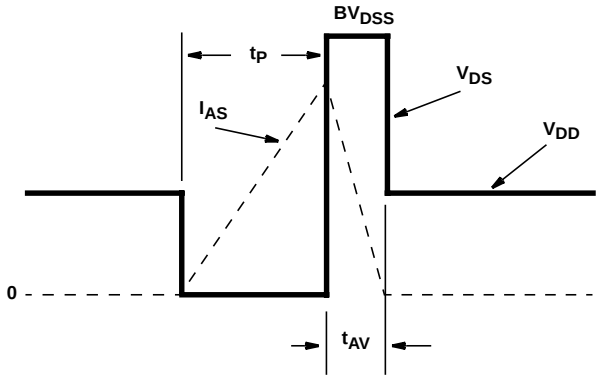



FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

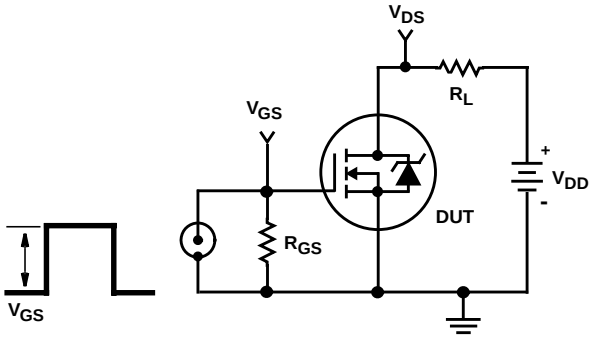



FIGURE 15. SWITCHING TIME TEST CIRCUIT

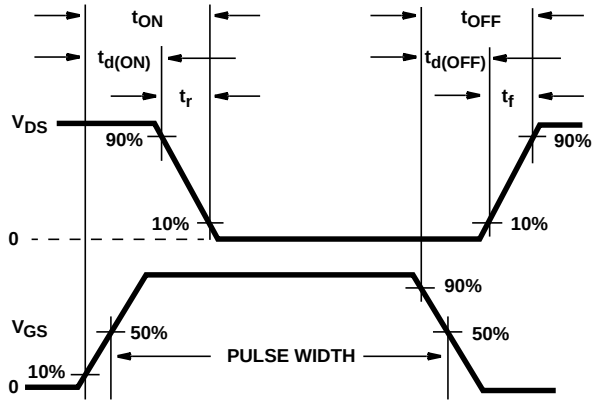



FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

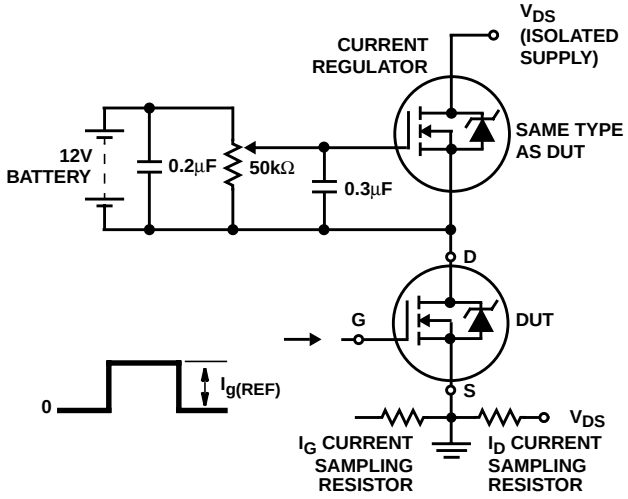



FIGURE 17. GATE CHARGE TEST CIRCUIT

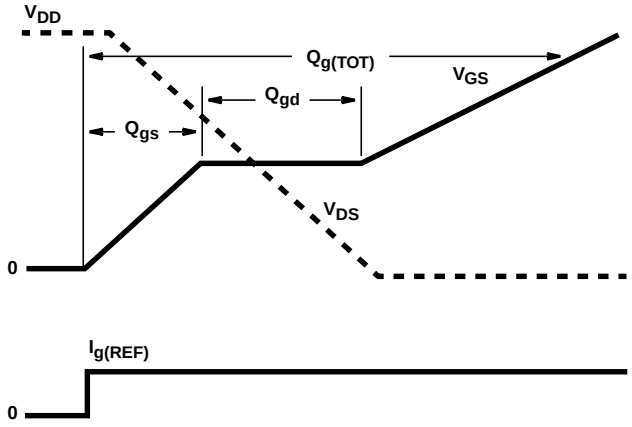



FIGURE 18. GATE CHARGE WAVEFORMS

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