STAC9750_MB - Main Board Audio Reference Design Overview

SCOPE: The STAC9750 Main Board reference design provides a complete 2-channel audio solution with digital audio I/O.

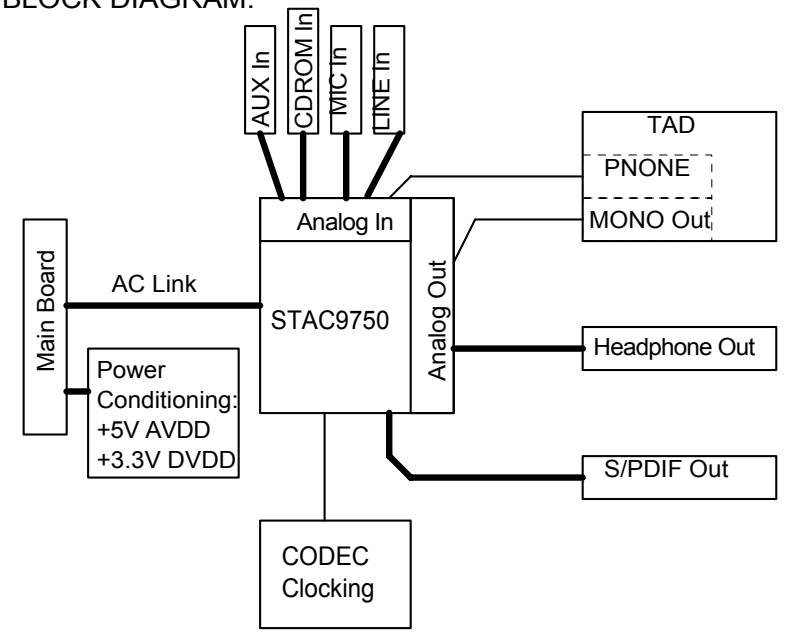
UNIQUE COMPONENTS:

1) STAC9750 Audio Codec with 48-TQFP, 9.0mm tip-to-tip, package.
2) 24.576 MHz crystal in Epson MA-306 package, use dual MA-306/CA-301 layout.
3) ZR78L05 in SOT-223.
4) Radial lead capacitors PCB footprints are listed in PackageDiameter/LeadSpacing/LeadDiameter form.
5) EIA prefix footprint surface mount components (EIA abcd) have dimensions of a.b mm by c.d mm.
6) SMT prefix footprint surface mount components (SMT wxyz) have dimensions of 0.wx inches by 0.yz inches.

REVISION HISTORY:

1) 7/06/01 - Original release.
2) 8/21/01 - Changed PLL mode table for CA3.
2) 12/28/01 - changed AFILT caps to 820pF.
3) 5/9/03 - Added SPDIF Enable/Disable resistor option.

BLOCK DIAGRAM:



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Title
Sigmatel Main Board Reference Design Overview

Size		Rev
A	STAC9750_MB	A3

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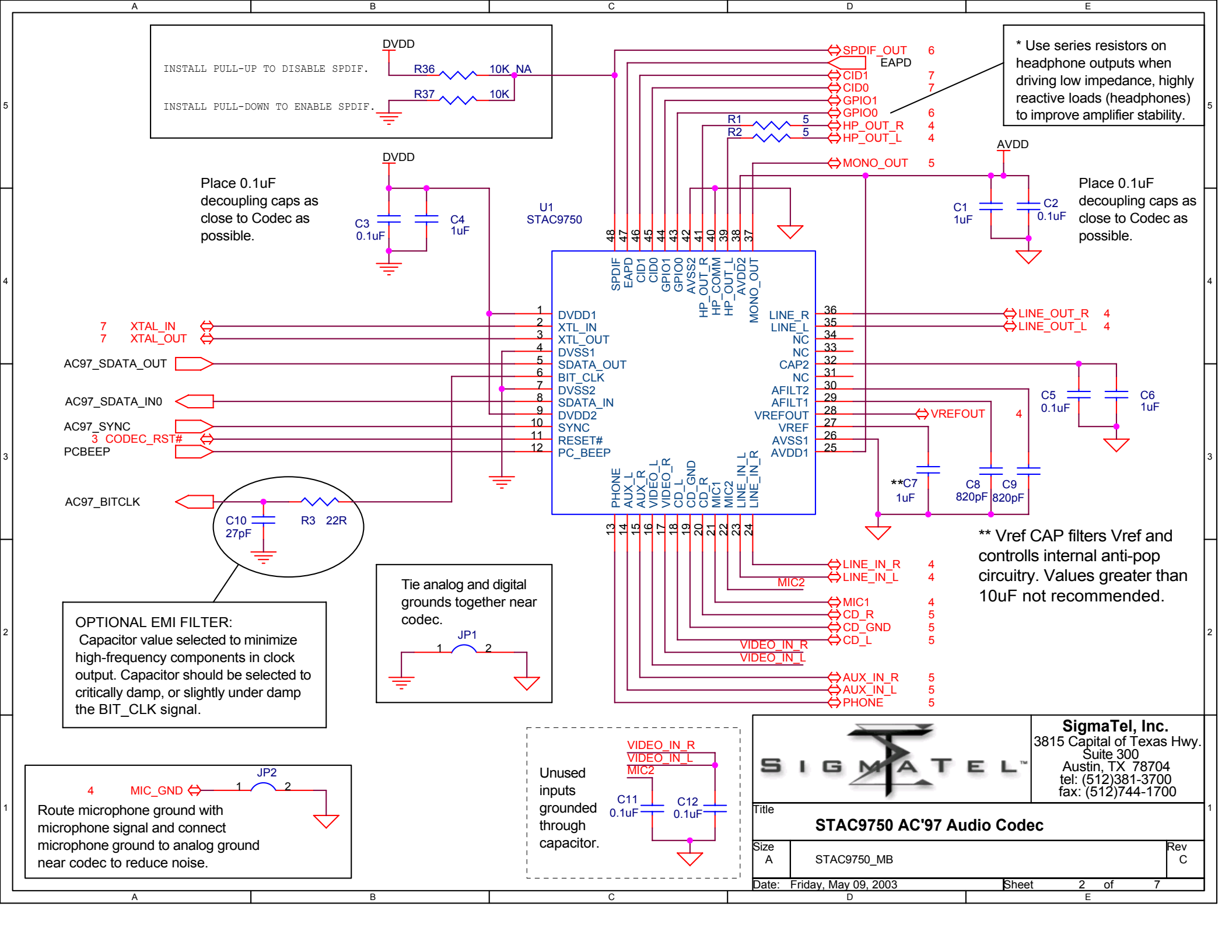
INSTALL PULL-UP TO DISABLE SPDIF.
DVDD
R36
10K_NA
INSTALL PULL-DOWN TO ENABLE SPDIF.
R37
10K
* Use series resistors on headphone outputs when driving low impedance, highly reactive loads (headphones) to improve amplifier stability.
Place 0.1uF decoupling caps as close to Codec as possible.
C3 0.1uF
C4 1uF
U1
STAC9750
SPDIF_OUT 6
EAPD
CID1 7
CID0 7
GPIO1
GPIO0 6
R1 5
R2 5
HP_OUT_R 4
HP_OUT_L 4
MONO_OUT 5
AVDD
C1 1uF
C2 0.1uF
Place 0.1uF decoupling caps as close to Codec as possible.
SPDIF
EAPD
CID1
CID0
GPIO1
GPIO0
AVSS2
HP_OUT_R
HP_COMM
HP_OUT_L
AVDD2
MONO_OUT
48 47 46 45 44 43 42 41 40 39 38 37
1 DVDD1
2 XTL_IN
3 XTL_OUT
4 DVSS1
5 SDATA_OUT
6 BIT_CLK
7 DVSS2
8 SDATA_IN
9 DVDD2
10 SYNC
11 RESET#
12 PC_BEEP
LINE_R 36
LINE_L 35
NC 34
NC 33
CAP2 32
NC 31
AFILT2 30
AFILT1 29
VREFOUT 28
VREF 27
AVSS1 26
AVDD1 25
LINE_OUT_R 4
LINE_OUT_L 4
7 XTAL_IN
7 XTAL_OUT
AC97_SDATA_OUT
AC97_SDATA_IN0
AC97_SYNC
3 CODEC_RST#
PCBEEP
AC97_BITCLK
C10 27pF
R3 22R
C5 0.1uF
C6 1uF
VREFOUT 4
**C7 1uF
C8 820pF
C9 820pF
PHONE
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
13 14 15 16 17 18 19 20 21 22 23 24
** Vref CAP filters Vref and controlls internal anti-pop circuitry. Values greater than 10uF not recommended.
LINE_IN_R 4
LINE_IN_L 4
MIC2
MIC1 4
CD_R 5
CD_GND 5
CD_L 5
VIDEO_IN_R
VIDEO_IN_L
AUX_IN_R 5
AUX_IN_L 5
PHONE 5
OPTIONAL EMI FILTER:
Capacitor value selected to minimize high-frequency components in clock output. Capacitor should be selected to critically damp, or slightly under damp the BIT_CLK signal.
Tie analog and digital grounds together near codec.
JP1
1
2
4 MIC_GND
JP2
1
2
Route microphone ground with microphone signal and connect microphone ground to analog ground near codec to reduce noise.
Unused inputs grounded through capacitor.
VIDEO_IN_R
VIDEO_IN_L
MIC2
C11 0.1uF
C12 0.1uF
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Title
STAC9750 AC'97 Audio Codec
Size A
STAC9750_MB
Rev C
Date: Friday, May 09, 2003
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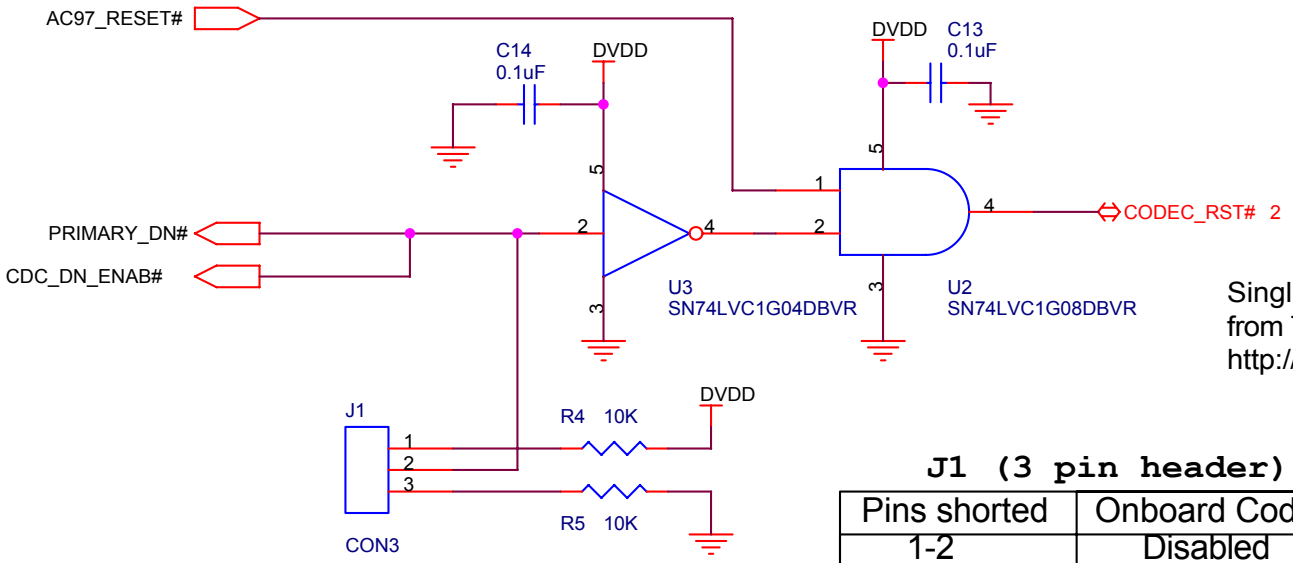
CODEC DISABLE CIRCUIT

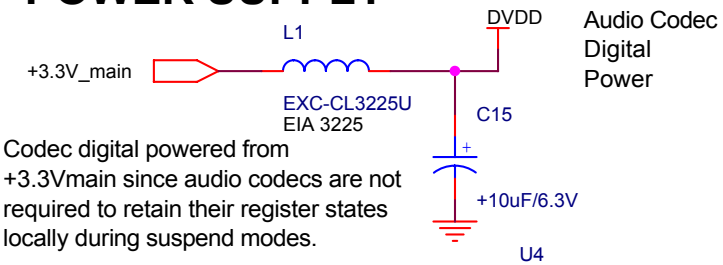


Single Gate devices available from Texas Instruments.
http://www.ti.com/

J1 (3 pin header)

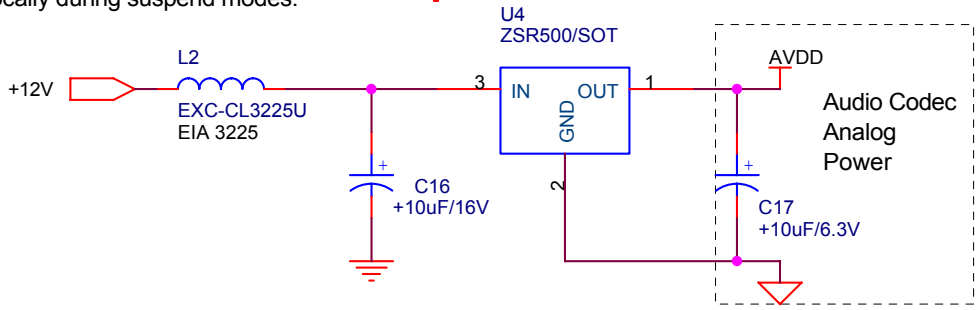
Pins shorted	Onboard Codec
1-2	Disabled
2-3	Enabled

POWER SUPPLY



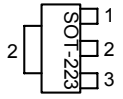
Audio Codec
Digital
Power

Codec digital powered from +3.3Vmain since audio codecs are not required to retain their register states locally during suspend modes.



Audio Codec
Analog
Power

LAYOUT NOTE FOR ZSR500G:



Device requires large copper pad for proper thermal regulation. Please consult Zetex at http://www.zetex.com/

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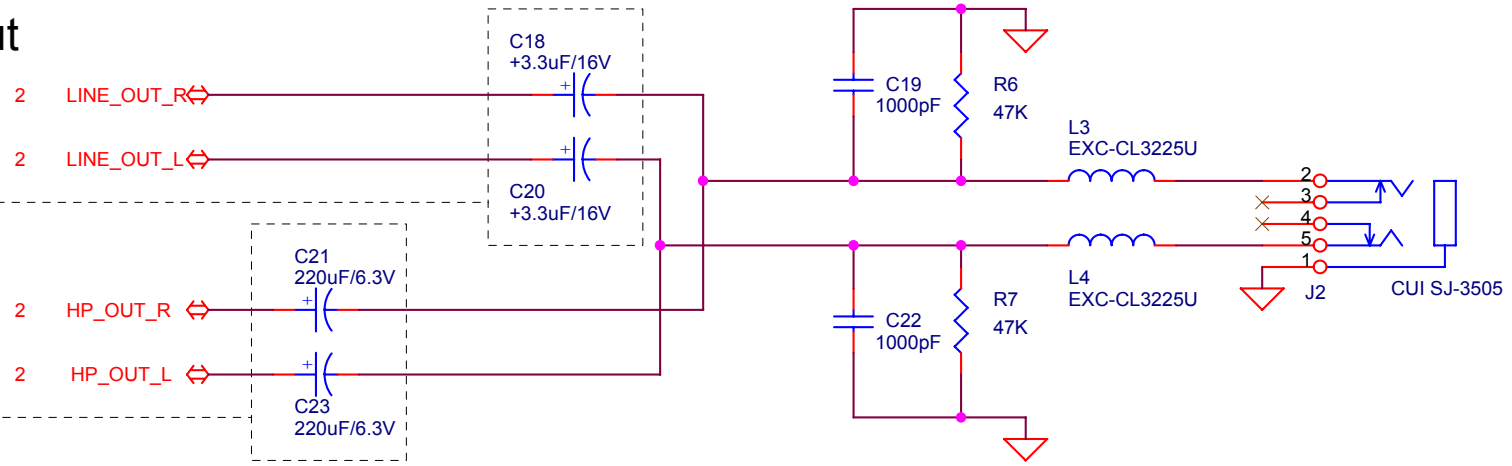
Title
CODEC DISABLE CIRCUITS

Size		Rev
A	STAC9750_MB	A

Date: Friday, May 09, 2003 Sheet 3 of 7

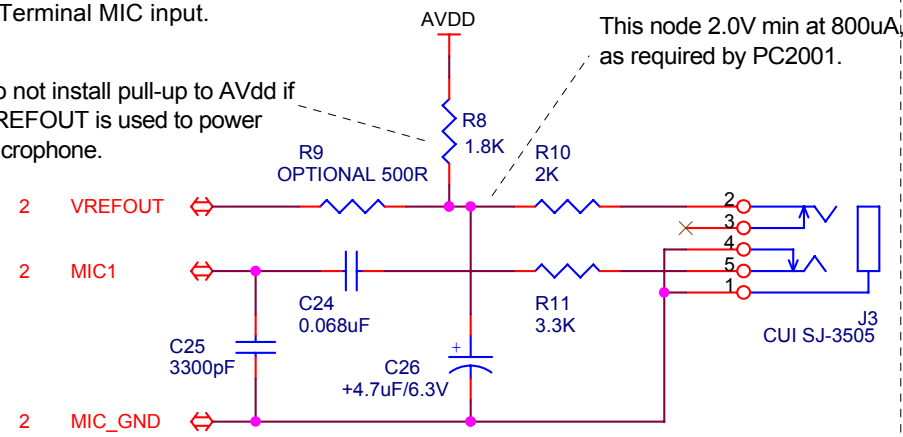
Headphone (Line) Out



*** Note: 220uF ac-coupling capacitors will drive loads of 32 ohms and greater and still meet the bandwidth requirements of PC2001. 3.3uF ac-coupling capacitors will drive loads of 10K ohms and greater and still meet the bandwidth requirements of PC2001.

Microphone Input Circuit

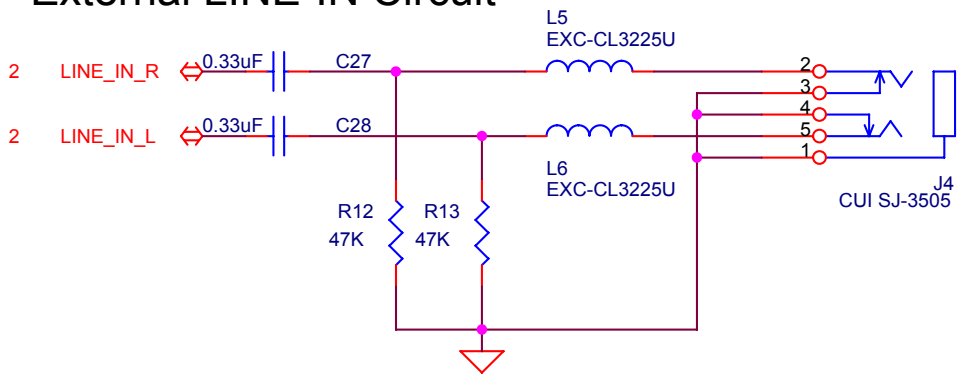
Supports 3-Terminal and 2-Terminal MIC input.



Microphone ground should be routed back to codec along with the main microphone signal trace. Improper microphone grounding can result in audible mouse and CDROM noise. Tie MIC_GND to AGND at a point near the codec.

REAR PANEL

External LINE-IN Circuit



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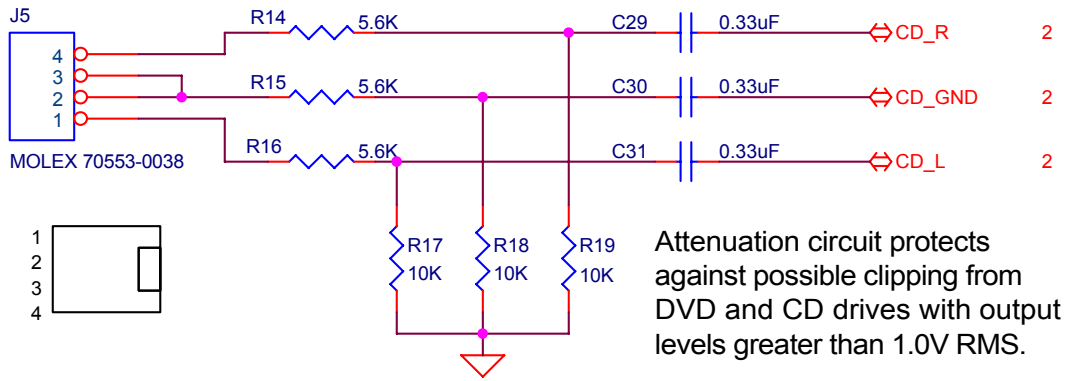
Title: **Rear Panel Jacks**

Size		Rev
A	STAC9750_MB	A

Date: Friday, May 09, 2003 Sheet 4 of 7

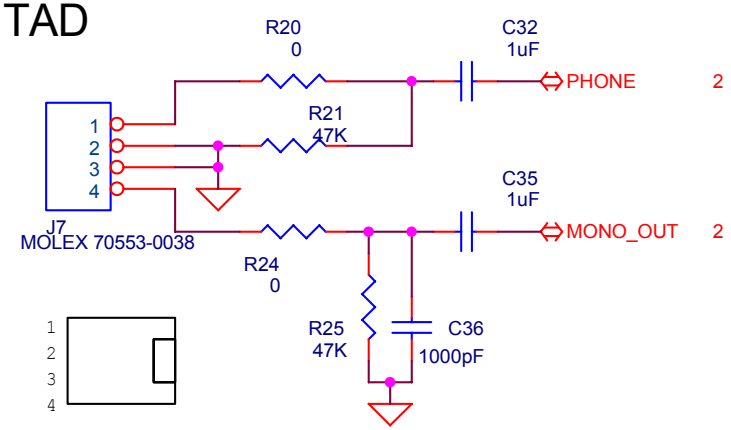
INTERNAL AUDIO JACKS

CDROM Circuit with 4.5dB Attenuation

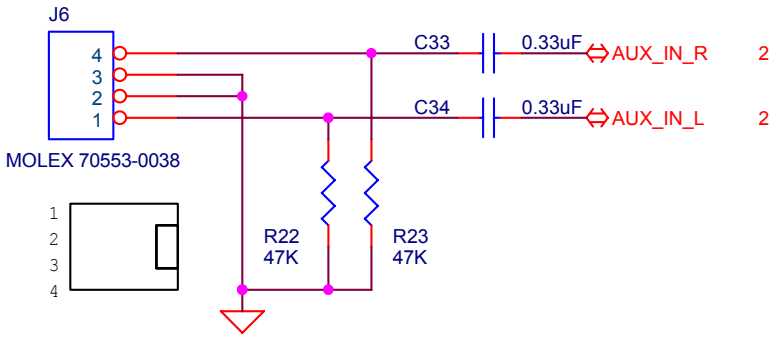


Attenuation circuit protects against possible clipping from DVD and CD drives with output levels greater than 1.0V RMS.

TAD



AUX Input Circuit



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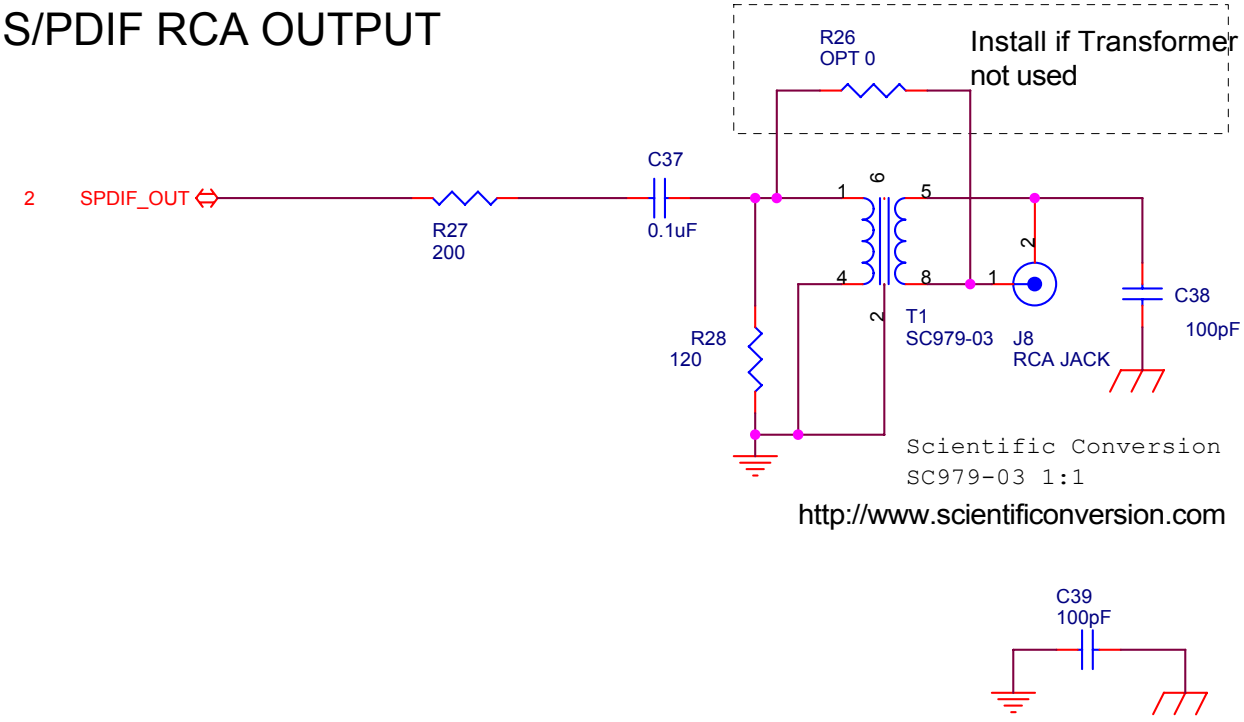
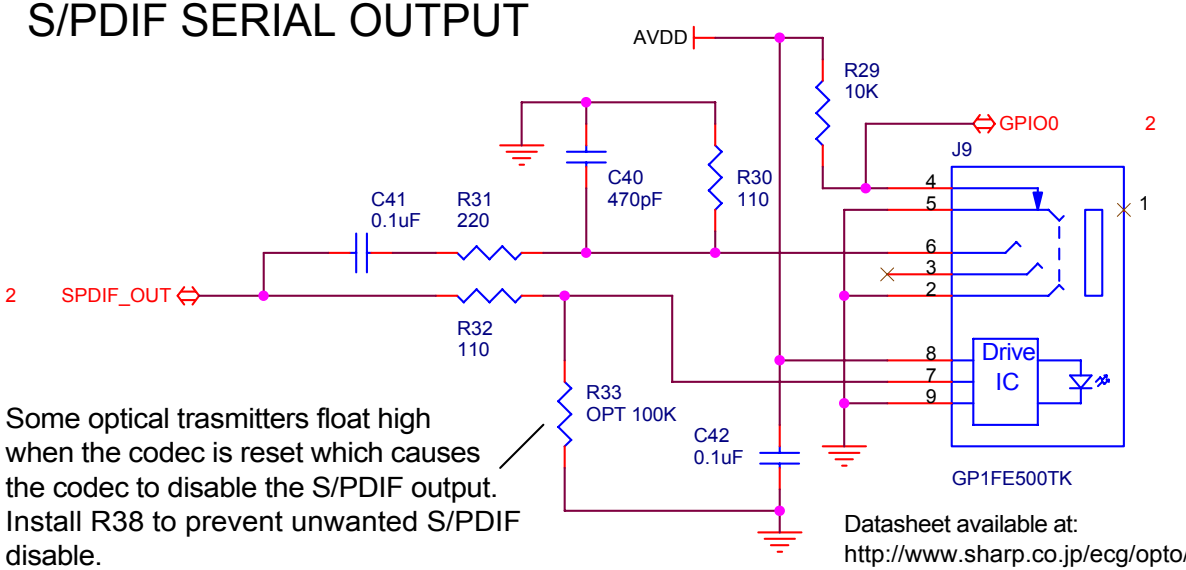
Title	**Analog Audio Jacks**	
Size A	STAC9750_MB	Rev A
Date: Friday, May 09, 2003	Sheet 5 of 7	

S/PDIF RCA OUTPUT



Please do not populate both the 3.5mm and the RCA SPDIF options.

S/PDIF SERIAL OUTPUT



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Title: **S/PDIF Output**

Size		Rev
A	STAC9750_MB	A

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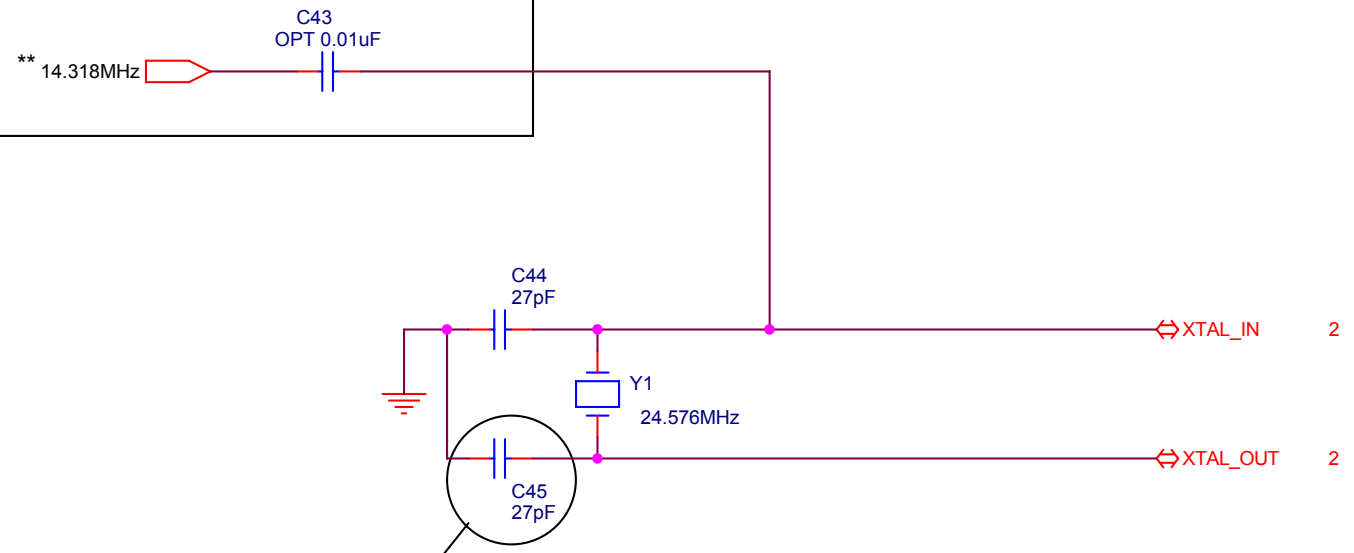
Optional Main Board Clock Source
Do not populate C44 or Y1 when
using an external clock.
Replace C45 with 0 ohm resistor
SEE TABLE BELOW



Motherboard Clock Frequency determines the CID0/CID1 values when external clock is selected (XTAL_OUT must be grounded by replacing C45 with a 0 ohm resistor)

Clock Source	R40 CID1	R39 CID0	C45 XTAL_OUT
**14.318 MHz	open	open	GND
27 MHz	open	1K	GND
48 Mhz	1K	open	GND
24.576 MHz	1K	1K	GND

*STAC9750 CA1 and CA2 revisions differ from this chart.

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Title
Codec Clocking

Size		Rev
A	STAC9750_MB	B

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