STEL-2176

User Manual

STel-MAN-97709

STEL-2176

Digital Mod/Demod ASIC

16/64/256 QAM Receiver with FEC

QPSK/16 QAM Transmitter with FEC

intel

TRADEMARKS

Stanford Telecom® and STEL® are registered trademarks of Stanford Telecommunications, Incorporated.

FOREWORD

The Telecom Component Products Division of Stanford Telecommunications, Inc., is pleased to provide its customers with this copy of the STEL 2176 User Manual.

This User Manual contains product information for the STEL 2176 and is being provided to assist our customers in understanding the advantages to be gained by integrating both the receiver and transmitter functions as an integral portion of their cable modem chip.

Recipients of this User Manual should note that the content contained here-in is subject to change. The content of this User Manual will be updated to reflect the latest technical data, without notice to the recipients of this document.

ERRATA for STEL-2176

Supported Modes of Operation:

Downstream

FEC	16 QAM	64 QAM	256 QAM
Annex A	X	X	
Annex B		X	X
Annex C	X	X	

Upstream

STD	BPSK	QPSK	16 QAM
MCNS		X	X
DAVIC	X	X	

TABLE OF CONTENTS

TABLE OF CONTENTS

PARAGRAPH PAGE

LIST OF FIGURES

LIST OF TABLES

LIST OF TABLES

KEY FEATURES

RECEIVER

- 10-bit A/D on chip
- 16/64/256 QAM demodulation
- Selectable ITU-T (J.83), Annex A/Annex B forward error correction (FEC)
- MCNS, IEEE 802.14 (preliminary), DAVIC/DVB compliant
- Parallel or serial output data with or without gaps
- Viterbi decoder for Annex B
- Selectable Reed-Solomon decoder for Annex A and Annex B
- Programmable De-Interleaver
- Programmable De-Randomizer
- MPEG-2 Framing
- Programmable control registers for maximum flexibility
- FIFO for optional removal of inter-frame gaps
- Automatic frequency control (± 200 kHz)
- Highly integrated receiver functions
- Up to 50 MHz IF input
- Uses inexpensive Crystal in the 25 MHz range
- Adaptive Channel Equalizer (ACE) to compensate for channel distortion
- Selectable Nyquist filter
- Fast acquisition

TRANSMITTER

- Patented (U.S. Patent #5,412,352) Complete BPSK/QPSK/16QAM modulator
- Complete upstream modulator solution—serial data in, RF signal out
- Programmable over a wide range of data rates
- Numerically Controlled Oscillator (NCO) modulator provides fine frequency resolution
- Carrier frequencies programmable from 5 to 65 MHz
- Uses inexpensive crystal in 25 MHz range
- Operates in continuous and burst modes
- Differential Encoder, Programmable Scrambler, and Programmable Reed-Solomon FEC Encoder
- Programmable 64-tap FIR filter for signal shaping before modulation
- 10-bit DAC on chip
- Compatible with DAVIC, IEEE 802.14 (preliminary), Intelsat IESS-308, MCNS Standards
- Supports low data rates for voice applications and high data rates for wideband applications

INTRODUCTION

The STEL-2176 is a complete subscriber-side cable modem chip that integrates both receiver and transmitter functions. It is offered in CMOS .35 micron geometry operating at 3.3 Volts with integrated DAC and ADC. Its programmable register set offers a flexible solution to meet current and evolving standards.

RECEIVER OVERVIEW

A 10-bit A/D converts the analog input signal. The analog input signal may be up to 50 MHz. For MCNS and DAVIC standards 44 MHz and 36 MHz are the two typical IF frequencies used. For 44 MHz the corresponding bandwidth is 6 MHz; for 36 MHz the corresponding bandwidth is 8 MHz. Sampling of the input may be set for 25 MHz for the 6 MHz bandwidth or 29 MHz for the 8 MHz bandwidth.

The downstream receiver offers 16/64/256 QAM demodulation for Annex A, associated with DAVIC, or Annex B, associated with MCNS. It also offers a variety of choices for the data and clock outputs: frames with or without gaps and parallel or serial data.

The incoming signal is sampled. The timing recovery circuit determines the epoch of each symbol. Automatic frequency and gain control circuitry correct the frequency and amplitude of the signal, and a Digital Down Converter (DDC) brings the alias band associated with sampling down to zero. A Nyquist filter eliminates inter-symbol interference, and an Adaptive Channel Equalizer (ACE) corrects for channel distortion while fine tuning the signal. A demapper transforms the modulated signal back into symbols and a De-Interleaver puts the data bits back into the original order, while Trellis and Reed-Solomon decoders handle error correction.

For Annex A, a Reed-Solomon decoder decodes and corrects every 204 bytes in 188 bytes. For Annex B, there is a Viterbi decoder and a 128, 122 (code word length, information) 7-bit Reed-Solomon decoder. A de-randomizer is used to unscramble the data stream.

Format of the receiver output is MPEG-2 frames.

TRANSMITTER OVERVIEW

The transmitter is highly integrated and flexible. It receives serial data, randomizes the data, performs Forward Error Correction (FEC) and differential encoding, maps the data to a constellation before modulation, and outputs an analog RF signal.

It includes a 10-bit DAC and is capable of operating at data rates up to 20 Mbps in QPSK mode and 40 Mbps in 16QAM mode.

The transmitter uses a digital FIR filter to optimally shape the spectrum of the modulating data prior to modulation. Signal level scaling is provided after the FIR filter to allow maximum arithmetic dynamic range.

The transmitter side offers QPSK and 16QAM modulation with frequencies from 5 to 65 MHz. It can operate in continuous or burst mode. And it can operate with very short gaps between bursts less than four symbols.

All digital interfaces support 3.3 volt and 5 volt logic.

MECHANICAL SPECIFICATIONS

208-PIN SQFP PACKAGE

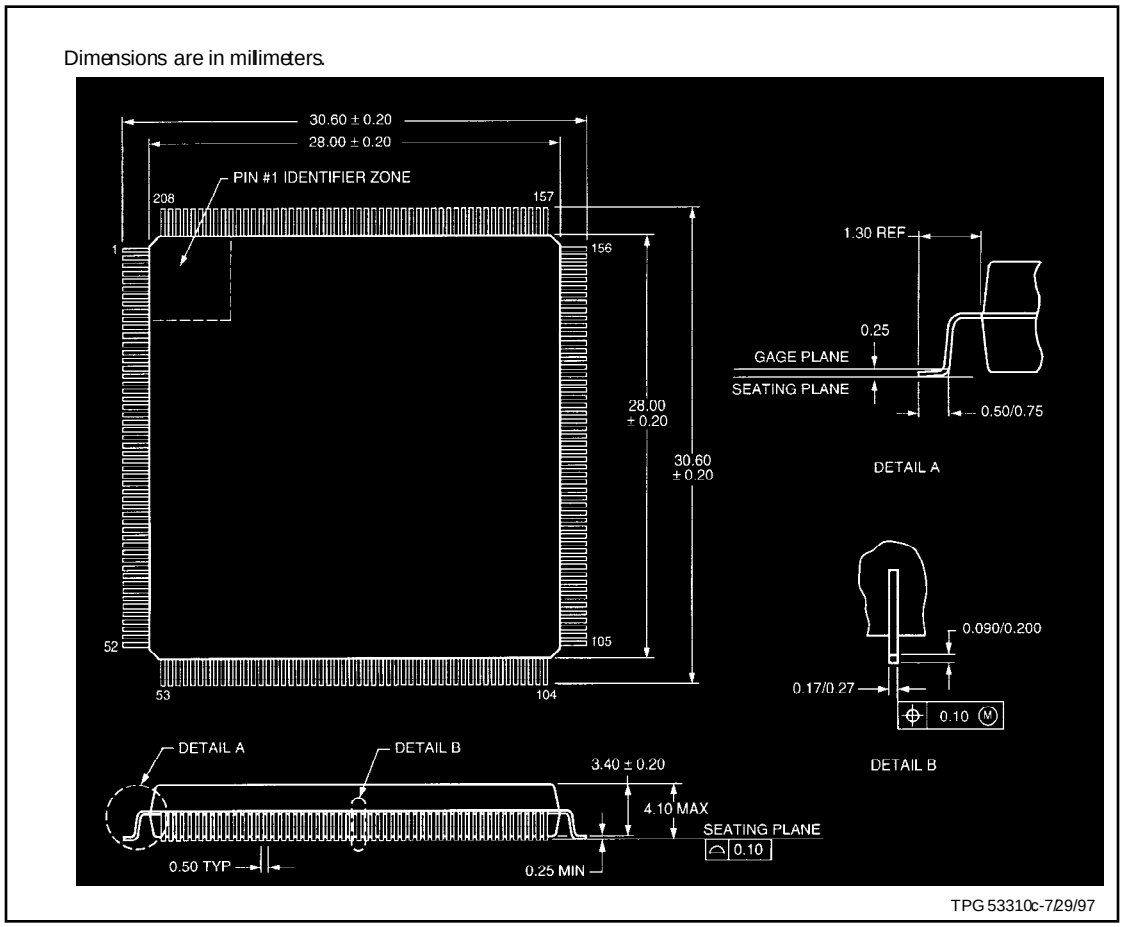


Table 1. STEL-2176 Pin Assignments

Pin No.	Pin Name	Pin Type	Pin Description
1	VSS	Ground	
2	VDD	Power	Dedicated to crystal oscillator at pins 3 & 4
3	RXOSCIN	Input	Receiver oscillator input
4	RXOSCOUT	Output	Receiver oscillator output
5	VSS	Ground	Dedicated to crystal oscillator at pins 3 & 4
6	VDD	Power	Dedicated to digital section of receive clock multiplier
7	VDDA	Power (Analog)	Dedicated to analog section of receive clock multiplier
8	RXMULTEN	Input	Enable receive clock multiplier
9	VSSA	Ground (Analog)	Dedicated to receive clock multiplier
10	VSS	Ground	Dedicated to receive clock multiplier
11	RXMULTCLK	Output	Receive clock multiplier output; enabled by pin 58
12	VDD	Power	
13	ADCDATASEL[2]	Input	ADC/DAC bypass mode select; 111=normal operation
14	ADCDATASEL[1]	Input	ADC/DAC bypass mode select; 110=bypass ADC
15	ADCDATASEL[0]	Input	ADC/DAC bypass mode select; 101=bypass DAC
16	VSS	Ground	
17	ADDATA[9]	Bi-directional	Bypass/test ADC/DAC

Pin No.	Pin Name	Pin Type	Pin Description
18	ADDATA[8]	Bi-directional	Bypass/test ADC/DAC
19	ADDATA[7]	Bi-directional	Bypass/test ADC/DAC
20	ADDATA[6]	Bi-directional	Bypass/test ADC/DAC
21	ADDATA[5]	Bi-directional	Bypass/test ADC/DAC
22	VDD	Power	
23	ADDATA[4]	Bi-directional	Bypass/test ADC/DAC
24	ADDATA[3]	Bi-directional	Bypass/test ADC/DAC
25	ADDATA[2]	Bi-directional	Bypass/test ADC/DAC
26	ADDATA[1]	Bi-directional	Bypass/test ADC/DAC
27	ADDATA[0]	Bi-directional	Bypass/test ADC/DAC
28	VSS	Ground	
29	RXAGCOUTB	Output	AGC output B
30	RXAGCOUTA	Output	AGC output A
31	VDD5	Power	3.3V or 5V for AGC pins 29 & 30
32	V3OP	Input	Must set high if pin 31 is 3.3V or low if pin 31 is 5V
33	VSS	Ground	
34	IC		Internal connection - leave open
35	SO	Output	SPI data out
36	VDD	Power	
37	SI	Input	SPI data in
38	SCK	Input	SPI clock
39	VSS	Ground	
40	ADDR[7]	Input	Control/Status register parallel address bus
41	ADDR[6]	Input	Control/Status register parallel address bus
42	ADDR[5]	Input	Control/Status register parallel address bus
43	ADDR[4]	Input	Control/Status register parallel address bus
44	VDD	Power	
45	ADDR[3]	Input	Control/Status register parallel address bus
46	ADDR[2]	Input	Control/Status register parallel address bus
47	ADDR[1]	Input	Control/Status register parallel address bus
48	ADDR[0]	Input	Control/Status register parallel address bus
49	VSS	Ground	
50	INTSEL[1]	Input	Serial/parallel inter. sel.: 00=parallel, 01=SPI (serial)
51	INTSEL[0]	Input	Serial/parallel interface select: 10=reserved, 11=res.
52	VDD	Power	
53	VSS	Ground	
54	$\overline{CS}$	Input	Control/Status register chip select (active low)
55	$\overline{WRB}$	Input	Control/Status register read/write (low=write)
56	$\overline{DSB}$	Input	Control/Status register data strobe signal (active low)
57	VDD	Power	
58	ENCLKOUT	Input	Enables output pins 11 & 102
59	VSS	Ground	
60	DATA[7]	Bi-directional	Control/Status register parallel data in/out
61	DATA[6]	Bi-directional	Control/Status register parallel data in/out
62	DATA[5]	Bi-directional	Control/Status register parallel data in/out
63	DATA[4]	Bi-directional	Control/Status register parallel data in/out
64	VDD	Power	
65	DATA[3]	Bi-directional	Control/Status register parallel data in/out
66	DATA[2]	Bi-directional	Control/Status register parallel data in/out
67	DATA[1]	Bi-directional	Control/Status register parallel data in/out
68	DATA[0]	Bi-directional	Control/Status register parallel data in/out
69	VSS	Ground	
70	RXRESCLK	Output	FEC test clock output (8 times RX symbol rate)
71	VDD	Power	
72	RXTSTDOUT[9]	Output	Test mux output
73	RXTSTDOUT[8]	Output	Test mux output
74	RXTSTDOUT[7]	Output	Test mux output
75	RXTSTDOUT[6]	Output	Test mux output

Pin No.	Pin Name	Pin Type	Pin Description
76	VSS	Ground	
77	RXTSTDOUT[5]	Output	Test mux output
78	RXTSTDOUT[4]	Output	Test mux output
79	RXTSTDOUT[3]	Output	Test mux output
80	RXTSTDOUT[2]	Output	Test mux output
81	VDD	Power	
82	RXTSTDOUT[1]	Output	Test mux output
83	RXTSTDOUT[0]	Output	Test mux output
84	RXTSTCLK	Output	Test mux output clock
85	VSS	Ground	
86	VDD	Power	Dedicated to digital portion of DAC
87	VDDA	Power (analog)	Dedicated to analog portion of DAC
88	DACOUTP	Analog output	Output of DAC. Terminate in 37.5 ohms to ground (See Figure 2)
89	DACOUTN	Analog output	Comp. output of DAC. Terminate in 37.5 ohms to ground (See Figure 2)
90	VSSA	Power (analog)	Dedicated to analog portion of DAC
91	VSS	Ground	Dedicated to digital portion of DAC
92	VDD	Power	Dedicated to crystal oscillator at pins 93 & 94
93	TXOSCIN	Input	TX oscillator input
94	TXOSCOUT	Output	TX oscillator output
95	VSS	Ground	Dedicated to crystal oscillator at pins 93 & 94
96	VDD	Power	Dedicated to digital section of transmit clock PLL
97	VDDA	Power (analog)	Dedicated to analog section of transmit clock PLL
98	TXPLLEN	Input	Enable transmit clock PLL
99	VSSA	Ground (analog)	Dedicated to analog section of transmit clock PLL
100	TXBYPCLK	Input	High speed transmit bypass clock
101	VDD	Power	Dedicated to digital section of transmit clock PLL
102	TXPLLCLK	Output	Transmit clock PLL output; enabled by pin 58
103	VSS	Ground	Dedicated to digital section of transmit clock PLL
104	VDD	Power	
105	VSS	Ground	
106	$\overline{\text{TXRSTB}}$	Input	Transmit reset (active low)
107	VDD	Power	
108	TXTSDATA	Input	Transmit data input
109	TXDATAENI	Input	Transmit data enable input
110	TXTCLK	Input	Transmit tclk
111	VSS	Ground	
112	TXFCWSEL[1]	Input	Transmit frequency control word (FCW) select
113	TXFCWSEL[0]	Input	Transmit frequency control word (FCW) select
114	VDD	Power	
115	TXCLKEN	Input	Transmit clock enable
116	TXDIFFEN	Input	Transmit differential encoder enable
117	TXRDSLEN	Input	Transmit Reed-Solomon enable
118	TXSCRMEN	Input	Transmit scrambler enable
119	VSS	Ground	
120	TXCKSUM	Output	Transmit Reed-Solomon check sum
121	TXACLK	Output	Transmit auxiliary clock output
122	TXDATAENO	Output	Transmit data enable output
123	VDD	Power	
124	TXBITCLK	Output	Transmit bit clock
125	TXSYMPLS	Output	Transmit symbol pulse output
126	TXNCOLD	Input	Transmit NCO load
127	VDD5	Power	Input buffer bias. Set to 3.3V or 5V dep. on max. input V. voltage.
128	RXRSTB	Input	Receiver reset (active low)
129	VSS	Ground	
130	RXPDATAOUT[7]	Output	Receive parallel output data
131	RXPDATAOUT[6]	Output	Receive parallel output data
132	RXPDATAOUT[5]	Output	Receive parallel output data

Pin No.	Pin Name	Pin Type	Pin Description
133	RXPDATAOUT[4]	Output	Receive parallel output data
134	VDD	Power	
135	RXPDATAOUT[3]	Output	Receive parallel output data
136	RXPDATAOUT[2]	Output	Receive parallel output data
137	RXPDATAOUT[1]	Output	Receive parallel output data
138	RXPDATAOUT[0]	Output	Rec. par. output data or serial data if in serial mode
139	VSS	Ground	
140	RXOUTCLK	Output	Receive output data clock
141	VDD	Power	
142	RXACQFLAG	Output	Receive demod. acquisition flag
143	RXACQFAIL	Output	Receive demod. acquisition failure flag
144	RXDECDFLG	Output	Receive FEC decodable flag
145	FRAMESYNC	Output	Receive output frame sync flag
146	VSS	Ground	
147	SRAMADDR[15]	Output	De-Interleaver optional external SRAM address
148	SRAMADDR[14]	Output	De-Interleaver optional external SRAM address
149	SRAMADDR[13]	Output	De-Interleaver optional external SRAM address
150	SRAMADDR[12]	Output	De-Interleaver optional external SRAM address
151	VDD	Power	
152	SRAMADDR[11]	Output	De-Interleaver optional external SRAM address
153	SRAMADDR[10]	Output	De-Interleaver optional external SRAM address
154	SRAMADDR[9]	Output	De-Interleaver optional external SRAM address
155	SRAMADDR[8]	Output	De-Interleaver optional external SRAM address
156	VSS	Ground	
157	VDD	Power	
158	VSS	Ground	
159	SRAMADDR[7]	Output	De-Interleaver optional external SRAM address
160	SRAMADDR[6]	Output	De-Interleaver optional external SRAM address
161	SRAMADDR[5]	Output	De-Interleaver optional external SRAM address
162	SRAMADDR[4]	Output	De-Interleaver optional external SRAM address
163	VDD	Power	
164	SRAMADDR[3]	Output	De-Interleaver optional external SRAM address
165	SRAMADDR[2]	Output	De-Interleaver optional external SRAM address
166	SRAMADDR[1]	Output	De-Interleaver optional external SRAM address
167	SRAMADDR[0]	Output	De-Interleaver optional external SRAM address
168	VSS	Ground	
169	SRAMDATA[7]	Bi-Directional	De-Interleaver optional external SRAM data bus
170	SRAMDATA[6]	Bi-Directional	De-Interleaver optional external SRAM data bus
171	SRAMDATA[5]	Bi-Directional	De-Interleaver optional external SRAM data bus
172	SRAMDATA[4]	Bi-Directional	De-Interleaver optional external SRAM data bus
173	VDD	Power	
174	SRAMDATA[3]	Bi-Directional	De-Interleaver optional external SRAM data bus
175	SRAMDATA[2]	Bi-Directional	De-Interleaver optional external SRAM data bus
176	SRAMDATA[1]	Bi-Directional	De-Interleaver optional external SRAM data bus
177	SRAMDATA[0]	Bi-Directional	De-Interleaver optional external SRAM data bus
178	VSS	Ground	
179	SRAMWEB	Output	De-Interleaver SRAM write enable (active low)
180	SRAMCSB	Output	De-Interleaver SRAM chip select (active low)
181	SRAMOEB	Output	De-Interleaver SRAM output enable (active low)
182	VDD	Power	
183	RXIENBLE	Input	FEC test input I clock
184	RXQENBLE	Input	FEC test input Q clock
185	VSS	Ground	
186	RXBYPCLK	Bi-directional	Receiver bypass clock input; output reserved
187	VDD	Power	
188	VSSA	Ground (analog)	Dedicated to analog section of ADC (See Figure 1)
189	VDDA	Power (analog)	Dedicated to analog section of ADC (See Figure 1)
190	VCMA	Analog output	From ADC (See Figure 1)
191	VDD	Power	Dedicated to digital section of ADC (See Figure 1)

Pin No.	Pin Name	Pin Type	Pin Description
192	VREFN	Analog output	From ADC(See Figure 1)
193	VSSA	Ground (analog)	Dedicated to analog section of ADC(See Figure 1)
194	VSS	Ground	Dedicated to digital section of ADC (See Figure 1)
195	VDDA	Power (analog)	Dedicated to analog section of ADC (See Figure 1)
196	VDDA	Power (analog)	Dedicated to analog section of ADC(See Figure 1)
197	ADCINP	Analog input	ADC input(See Figure 1)
198	ADCINN	Analog input	Complementary ADC input(See Figure 1)
199	VSSA	Ground (analog)	Dedicated to analog section of ADC (See Figure 1)
200	VSSA	Ground (analog)	Dedicated to analog section of ADC(See Figure 1)
201	VDD	Power	Dedicated to digital section of ADC(See Figure 1)
202	VDDA	Power (analog)	Dedicated to analog section of ADC(See Figure 1)
203	VREFP	Analog output	From ADC(See Figure 1)
204	VSS	Ground	Dedicated to digital section of ADC(See Figure 1)
205	VCMB	Analog output	From ADC(See Figure 1)
206	VSSA	Ground (analog)	Dedicated to analog section of ADC(See Figure 1)
207	VDDA	Power (analog)	Dedicated to analog section of ADC(See Figure 1)
208	VDD	Power	

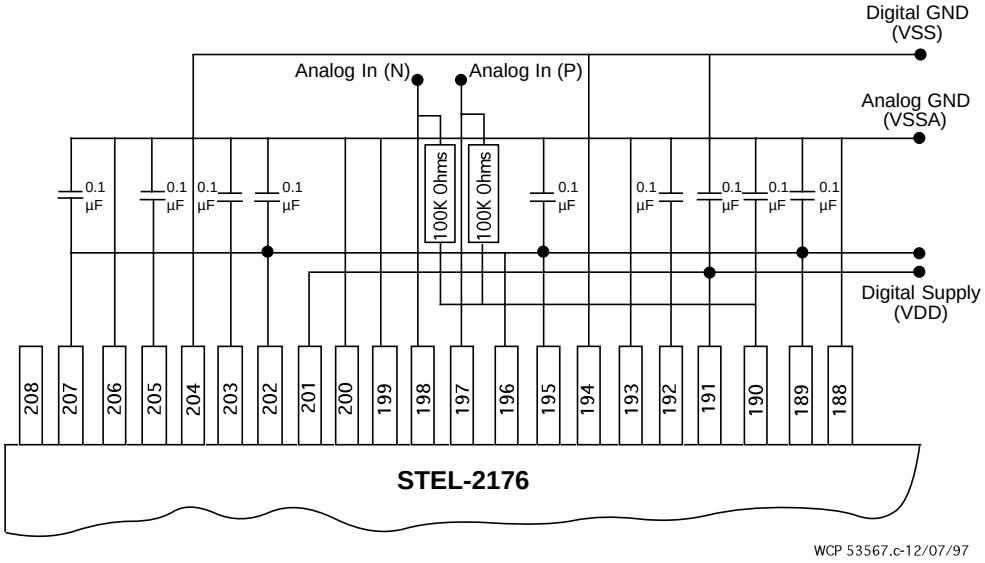


Figure 1. Reference A/D Wiring

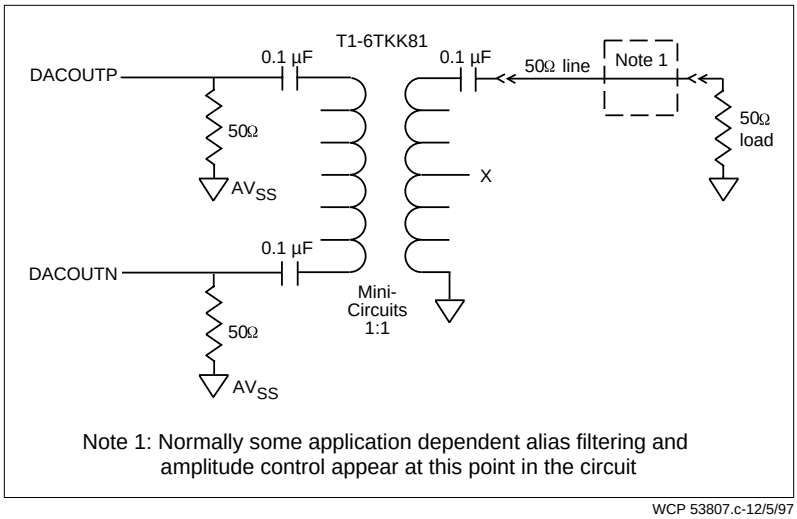


Figure 2. Example Output Load Schematic

ELECTRICAL SPECIFICATIONS

The STEL-2176 electrical characteristics are provided by Table 2 through Table 4.

WARNING

Stresses greater than those shown in Table 2 may cause permanent damage to the STEL-2176. Exposure to these conditions for extended periods may also affect the STEL-2176 reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Range	Units [Note 1]
T_{stg}	Storage Temperature	–40 to +125	°C
V_{DDmax}	Supply voltage on VDD	–0.3 to +4.6	volts
A_{VDDmax}	Supply voltage on AVDD	–0.3 to +4.6	volts
$5V_{DDmax}$	Supply voltage on 5VDD	–0.3 to +7.0	volts [Note 2]
AV_{SS}	Analog supply return for AVDD	± 10% of VDD	volts
$V_{I(max)}$	Input voltage	–0.3 to 5VDD+0.3	volts
I_i	DC input current	± 30	mA
$P_{Diss\ (max)}$	Power dissipation	1500	mW

Note:

All voltages are referenced to V_{SS}.

$5V_{DD}$ must be greater than or equal to V_{SS}. This rule can be violated for a maximum of 100 msec during power up.

Table 3. Recommended Operating Conditions

Symbol	Parameter	Range	Units [Note 1]
AV_{DD}	Supply Voltage	+3.3 ± 10%	Volts
$5V_{DD}$	Supply Voltage	+5.0 ± 10%	Volts [Note 2]
V_{DD}	Supply Voltage	+3.3 ± 10%	Volts
C_{LOAD}	DAC Load Capacitance	≤ 20	pF
R_{LOAD}	DAC Load Resistance	≤ 30K	ohms
	Recommended DAC Load	37.5	ohms
V_{LOAD}	DAC Output Voltage	≤ 1.25	Volts
T_a	Operating Temperature (Ambient)	–40 to +85	°C [Note 3]

Note:

1. All voltages with respect to V_{SS} and assume $AV_{ss} = V_{ss}$
2. If interface logic is to be driven by V_{DD} then connect the $5V_{DD}$ pin to the V_{DD} supply and set pin 32 to correct value.
3. Duty Cycle Derating is required from +70° to +85° C.

Table 4. ADC Performance Specifications

Parameter	Min	Nom	Max	Units
Sampling Frequency			50	MHz
Resolution		10		bits
Input Differential Signal Range	-0.75		+0.75	Volts
Analog Input Bandwidth	60			MHz
Signal to Distortion Ratio 10 MHz signal over 25 MHz BW	54			dB
Input Common Mode	1.4	1.5	1.6	Volts

Table 5. DC Characteristics

(V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, T_a = -40° to 85° C)

Symbol	Parameter	Min.	Nom.	Max.	Units	Conditions
I_{VDDQ}	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{VDD}	Supply Current, Operational, V_{DD}		1.9		mA/MHz	
$I5V_{DD}$	Supply Current, Operational, $5V_{DD}$		0.2		mA	
IAV_{DD}	Supply Current, Operational, AV_{DD}		12.0		mA	
VIH_{CLK}	Clock High Level Input Voltage	2.0			volts	**CLK**, Logic '1'
VIL_{CLK}	Clock Low Level Input Voltage			0.8	volts	**CLK**, Logic '0'
V_{IH}	High Level Input Voltage	2.0			volts	Other inputs, Logic '1'
V_{IL}	Low Level Input Voltage			0.8	volts	Other inputs, Logic '0'
I_{IH}	High Level Input Current			10	µA	$V_{IN} = 5V_{DD}$
I_{IL}	Low Level Input Current			–10	µA	$V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	3.0	VDD	volts	I_O = –2.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +2.0 mA
I_{OS}	Output Short Circuit Current		40		mA	$V_{OUT} = V_{DD}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4	10	pF	All outputs
I_{OFS}	Output Full Scale DAC Current	16	19	22	mA	Single output
V_O	DAC Compliance Voltage (Differential)		±0.96		Volts	Based on 50 ohms load resistance to ground.
R_O	DAC Output Resistance[1]		N/A			
C_O	DAC Output Capacitance		4	8	pF	

NOTES:
1. Current source to ground output.

RECEIVER

OVERVIEW

The STEL-2176 is a complete subscriber-side cable modem ASIC which integrates both the downstream receiver and upstream transmitter functions. The receiver includes a high performance 10-bit Analog-to-Digital Converter (ADC) with a direct Intermediate Frequency (IF) interface. The receiver also includes a QAM demodulator and both ITU-T (J.83) Annex A and Annex B Forward Error Correction (FEC). The upstream transmitter includes a BPSK/QPSK/16QAM modulator with highly flexible FEC and scrambling, and a 10-bit low spurious digital to analog converter (DAC) for direct synthesis of an upstream 5 to 65 MHz signal. Both the receiver and transmitter are highly flexible and programmable; the STEL-2176 Digital Mod/Demod ASIC offers a solution to meet current and evolving standards.

The input to the STEL-2176 receiver is an analog IF signal of up to 50 MHz. Typically, the IF signal has 44 MHz center frequency with a 6 MHz bandwidth for NTSC based systems, or a 36 MHz center frequency with an 8 MHz bandwidth for PAL based systems. In typical applications, the input signal is sampled by the ADC at approximately 25 MHz for the 44 MHz IF, or at approximately 29 MHz for the 36 MHz IF

This type of sub-sampling technique works by intentionally undersampling the carrier frequency so that aliased signal appears at a lower frequency. The sampling rate is still high enough to capture all of the modulation bandwidth without distortion. In the case of a 44 MHz IF and a 25 MHz clock, the resulting digital signal is centered at 6 MHz. In the case of a 36 MHz IF and 29 MHz clock, the resulting digital signal is centered at 7 MHz. For more information on sub-sampling techniques, please see Stanford Telecom Application Note A-117.

The digital samples from the ADC are downconverted to baseband I and Q signals in the Digital Down Converter (DDC) block. Since the RF tuner sections of a cable modem may have large frequency errors, an Automatic Frequency Control (AFC) block is used in the STEL-2176 for coarse tuning of the DDC. This allows rapid acquisition of the input signal even with frequency errors of ±200 kHz. Fine tuning of the DDC is done using a carrier Phase-Lock Loop (PLL).

An Automatic Gain Control (AGC) function provides two output signals to adjust the RF and IF analog gain stages of circuitry external to the STEL-2176, so that the ADC input is in the optimal range. The two outputs can be programmed to create a sequential AGC system which maximizes RF gain for improved receiver noise figure. The two AGC outputs and the external gain adjust blocks work together to maximize ADC performance, but when large adjacent channels are present, the power of the desired signal may change. A second digital AGC tracks and adjusts the level of the desired signal after the adjacent channel energy is removed by filtering.

Following the DDC, a square root raised cosine Nyquist filter eliminates adjacent channel signals, and performs matched filtering to eliminate intersymbol interference. The filter excess bandwidth or alpha is programmable from 0.12 to 0.20. The Timing Recovery block finds the exact location in the center of each symbol using a special low-jitter discriminator. These values are fed to the Adaptive Channel Equalizer.

An Adaptive Channel Equalizer (ACE) compensates for any multipath distortion on the input signal introduced in the channel. The equalizer uses one sample per symbol (T spaced taps). The output of the equalizer is baseband I and Q signals with carrier frequency and phase errors, symbol timing errors, gain errors, and multipath effects removed.

The Demapper takes the baseband I and Q signals representing the QAM symbols, and translates each symbol back into a series of binary values based on one of the selectable constellation maps.

Following the Demapper is the Forward Error Correction (FEC) system. This programmable system supports both the ITU-T (J.83) Annex A (see page 14) and Annex B (see page 16) standards. In general, both FEC systems employ Reed Solomon Decoders, Frame Sync circuits that determine the FEC code block boundaries, and a De-Interleaver. Interleaving is used in the FEC standards to improve performance when the channel contains bursty noise. Since the transmitter Interleaver spreads the data over a large time, when the receiver performs the matched operation to the Interleaver in order to bring the data back into the correct time sequence, any burst errors appear to be spread out in time. This helps makes these errors

correctable by the FEC. The STEL-2176 internal memory can support all MCNS Interleaver configurations. For deeper interleaving, a direct interface to external memory is provided.

The output of the receiver is typically arranged as MPEG-2 frames, although the MPEG-2 framing can be by-passed for ATM applications. The output can be 8-bit parallel with a byte clock or serial with a bit clock. The data can be output in a smooth fashion without inter-frame gaps or with the pauses in output data caused by the FEC system passed through to the output (see Receiver Timing discussion).

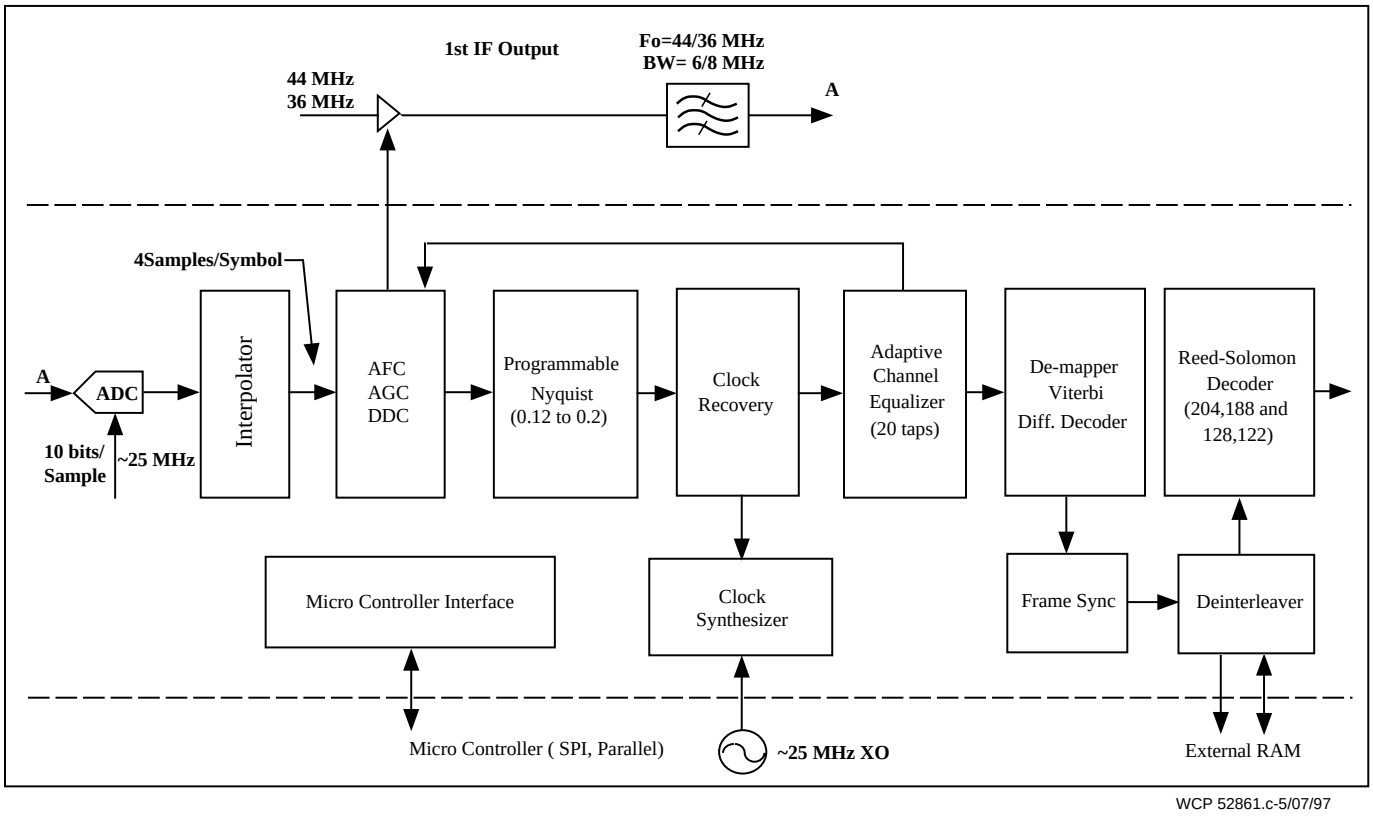


Figure 3. STEL-2176 Receiver Block Diagram

FUNCTIONAL BLOCKS

ADC

The ADC uses differential analog signal inputs ADCINP and ADCINN. Differential coupling to the ADC is important to prevent common mode noise from the digital sections of the ASIC from coupling into the input. The recommended input signal level is ± 0.75V. The input is sampled by the ADC, and the samples are converted into 10-bit digital values. The sampling rate is typically 25 MHz for an input of 44 MHz ± 3 MHz with a symbol rate of about 5 MHz (i.e., the MCNS standard) or 29 MHz for an input of 36 MHz ± 4 MHz with a symbol rate of about 7 MHz (i.e., the DAVIC and DVB standards). The sampling rate is controlled the choice of crystal connected between RXOSCIN and RXOSCOUT or by the clock frequency applied to RXOSCIN. The sample rate must be slightly more than 4 samples per symbol. The sample clock generated by the crystal/receive clock oscillator or applied to RXOSCIN must be a low phase noise signal. For this reason, dedicated power and ground connections for the receive oscillator and input buffer are adjacent to the RXOSCIN and RXOSCOUT pins.

Microcontroller Interface

The microcontroller interface provides access to the internal programmable Universal, Downstream (Receive), and Upstream (Transmit) registers (see page 20) via a parallel or a SPI interface. The interface used is selected by the interface select lines (INTSEL[1-0]).

The parallel interface consists of an 8-bit address bus (ADDR[7-0]), an 8-bit bi-directional data bus (DATA[7-0]), and the control signals chip select (CS), read/write (WRB), and data strobe (DSB).

The SPI interface consists of a serial input (SI), serial output (SO), and a serial clock (SCK).

Master Receive Clock Generator

The STEL-2176 uses a master clock (MCLK) to control the receive timing functions. MCLK can be generated in either of three ways as shown in Figure 4.

A receive bypass clock can be applied to the RXBYPCLK input and selected to drive CLK. The RXMULTEN should be held high to select the RXBYPCLK input.

An external clock can be applied to the RXOSCIN input or a crystal can be connected across the RXOSCIN and RXOSCOUT inputs. The oscillator circuit outputs a 20-50 MHz signal to a frequency multiplier PLL, which upconverts the signal to a 100-150 MHz clock. When the bypass clock is not used, RXMULTEN is driven high to select the output of the frequency multiplier to drive the MCLK signal. The frequency multiplier output frequency is controlled by the formula:

$$MCLK = OscillatorOutput * \frac{N}{M}$$

where:

- The Oscillator signal (RXOSCIN and RXOSCOUT) is four times the signal symbol rate.
- The value of M and N should be selected so MCLK is four times the value of the Oscillator signal.
- N is the value stored in RxFsynN (bits 6-0 of Bank 0 Register $F7_H$), and M is the value stored in RxFsynM (bits 6-0 of Bank 0 Register $F6_H$).
- The recommended values for DAVIC, DVB, and IEEE 802.14 are Oscillator Frequency = 29 MHz, M = 2, and N = 8. The recommended values for MCNS are Oscillator Frequency = 25 MHz, M = 2, and N = 8.

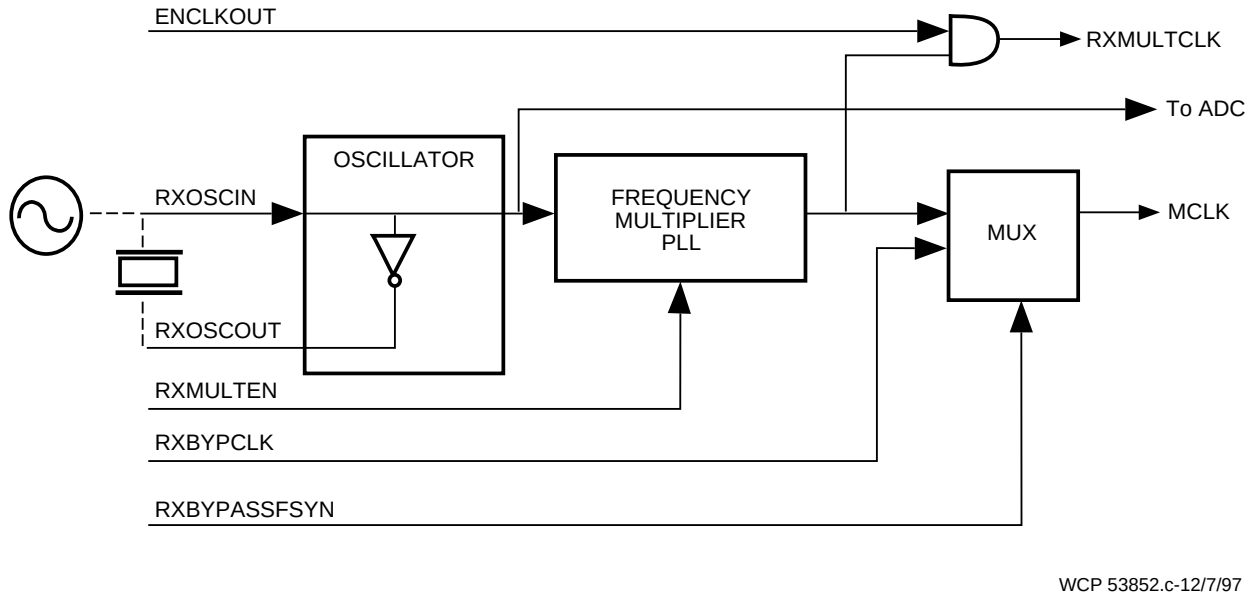


Figure 4. Master Receive Clock Generator

QAM Demodulator Blocks

The following diagram shows the major QAM circuit blocks.

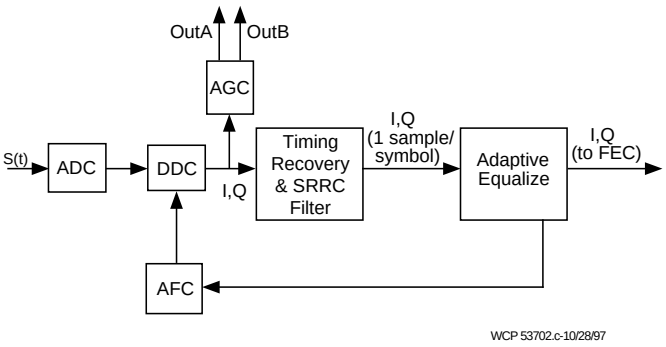


Figure 5. QAM Demodulator Blocks

Digital Down Converter (DDC)

The digital samples from the ADC are mixed down to baseband I and Q signals in the Digital Down Converter (DDC) block. The input analog signal is sub-sampled at the rate set by the receive crystal oscillator or a clock applied directly to the RXOSCIN input. The resultant sub-sampled input signal's spectrum is aliased to a lower frequency. In typical cases, with a 44 MHz _ 3 MHz input and a 25 MHz sample rate, the digital signal appears to the input of the DDC as a 6 MHz _ 3 MHz signal. For a 36 MHz _ 4 MHz input and a 29 MHz sample rate, the digital signal appears to the input of the DDC as a 7 MHz _ 4 MHz signal. Other input frequencies and sample rates are also possible. The digital signal is down converted to baseband I and Q by mixing with cos $2\pi f_c t$ and sin $2\pi f_c t$ where f_c is the center frequency of the digital signal.

The Digital Down Converter contains a numerically controlled oscillator (NCO) with cosine and sine outputs, a pair of mixers, and an image filter. The frequency f_c is a combination of a starting value that is set using DeltaTheta_in [13:0] (bits 7-2 of Bank 0 Register 10_H and Bank 0 Register 11_H) and any frequency error terms computed by the Automatic Frequency Control block. The value for DeltaTheta_in [13:0] is given by:

DeltaTheta_in [13:0] = f_c / ADC sample rate _214

For f_c = 6 MHz and ADC sample rate = 25 MHz, DeltaTheta_in [13:0] = $0F5C_H$

For f_c = 7 MHz and ADC sample rate = 29 MHz, DeltaTheta_in [13:0] = $0F73_H$

The complex NCO drives a pair of multipliers which serve as mixers. The products of the ADC samples and the sine and cosine outputs of the NCO produce the desired baseband I and Q signals plus undesired higher frequency image terms. These higher frequency terms are removed by an image filter.

Automatic Frequency control (AFC)

The STEL-2176 can accommodate up to ±200 kHz uncertainty in the carrier frequency. The carrier frequency recovery is divided into two steps. The first step is a coarse frequency estimation during initial signal acquisition. This estimation is performed by the AFC section. The estimated carrier frequency offset is calculated by the AFC and fed to the DDC NCO.

AGC

The AGC takes the output from the Image Filter in the DDC and estimates the power of the signal. The AGC discriminator compares the estimate to one or two different thresholds that can be set via the registers values AGC_ThresholdA (Bank 0 Register 14_H) and AGC_ThresholdB (Bank 0 Register 15_H). Thresholds should be set to optimize ADC performance. The range of the AGC`s power thresholds is 0 to 128 (2^{8-1}). For 256-QAM, the value ranges from about 75 to 100 (default is 96), depending on the desired A/D clipping level. The trade off for selecting the value weighs occasional ADC clipping with a large input versus loss of signal fidelity with a small input. The power of the input signal depends upon adjacent channel interference, AM hum, burst noise, etc.

The AGC generates two 1-bit outputs OUTA and OUTB that indicate whether that the input analog signal is too high or too low. The OUTA and OUTB signals should be smoothed using low pass filters. ***These filters can each be a series resistor of ___ ohms and a shunt capacitor of ___ _ F.*** OUTA and OUTB can be set to have a logic high voltage of either 3.3V or 5V. For 3.3V operation, connect the power source's +3.3V output to pins 31 and 32 and its return to V_{SS}. For 5V operation, connect the power source's +5V output to pin 31 and its return to pin 32 and V_{SS}.

The polarity of OUTA and OUTB may be controlled with AGC_InvertOutputA (bit 0 of Bank 0 Register 12_H) and AGC_InvertOutputB (bit 1 of Bank 0 Register 12H). For variable gain stages where a higher control voltage at the input to the filter produces higher gain, set the AGC_InvertOutput bit to 0. For variable gain stages

where a higher control voltage at the input to the filter produces lower gain, set the AGC_InvertOutput bit to 1.

The two outputs can be programmed to create a sequential AGC system which maximizes RF gain for improved receiver noise figure. This is accomplished by setting AGC_ThresholdA (Bank 0 Register 14_H) and AGC_ThresholdB (Bank 0 Register 15_H) to slightly different values. The threshold which is set to a lower value will cause its associated output to command increase gain first. This output is typically connected to the RF variable gain stages so that the best receiver noise figure is achieved.

Timing Recovery and Nyquist Filter

The sampled signal (> 4 times the symbol rate in I and Q format) is fed to this block to:

- Eliminate inter-symbol interference (ISI) by filtering it with a square route raised cosine filter (SRRC) of a selectable excess bandwidth (a) for 12%<= a<=20%.
- Recover the exact symbol rate, within 100 ppm of the nominal value.
- Resample and transmit one composite sample (I and Q for each symbol) to the equalizer. These samples are taken at the epoch of each symbol.

Adaptive Channel Equalizer

The output of the Timing Recovery block is fed to the Adaptive Equalizer at a rate of one complex sample/symbol. The Adaptive Equalizer will:

1. Compensate for channel distortion including:
   a. Multipath
   b. AM hum
   c. FM hum
   d. Phase noise
2. Fine tune to the carrier frequency and phase offset.
3. Set the acquisition flag "true", after the equalizer successfully locks on to the signal.
4. Write to ErrPwr (Block 0 Register 44_H) the estimated output SNR.

The adaptive equalizer control registers are Block 1 Registers 21_H to 24_H.

FEC Decoder Blocks

The purpose of the FEC subsystem is to improve the bit error rate performance of the data link. The arrangement of the FEC blocks in the receiver is in reverse order from the transmitter. The STEL-2176 FEC subsystem can decode signals which are generated in conformance with either the ITU-T (J.83) Annex A or Annex B FEC standards.

There are two different though similar set of blocks used for ITU-T (J.83) Annex A (Figure 6) and Annex B (Figure 13).

The STEL-2176 supports the MPEG-2 standard. MPEG-2 uses 188 byte packets with a sync byte and three header bytes containing service identification, scrambling, and control information. The 184 bytes of data follows the sync and header bytes. Normally this header information flows through to the receiver output, but with ITU-T (J.83) Annex B there is an option of bypassing the MPEG-2 outer layer of processing.

Annex A FEC

The ITU-T (J.83) Annex A FEC subsystem consists of the following blocks:

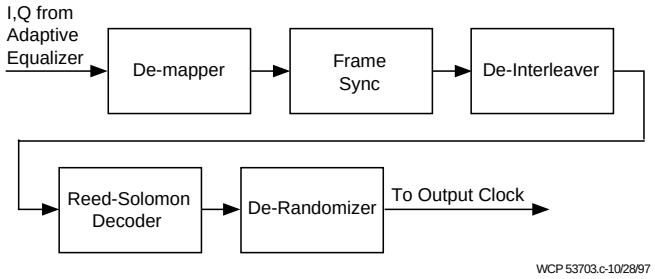


Figure 6. ITU-T (J.83) Annex A FEC Subsystem

Demapper

This block maps the Adaptive Channel Equalizer I and Q outputs for each symbol into 4, 6, or 8 bits for 16, 64, or 256 QAM respectively. The mapping tables are as follows:

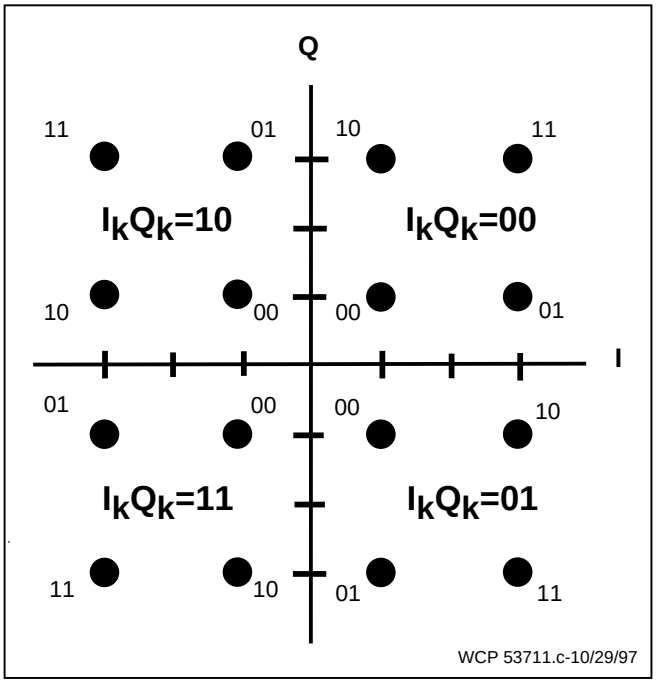


Figure 7. 16 QAM Constellation

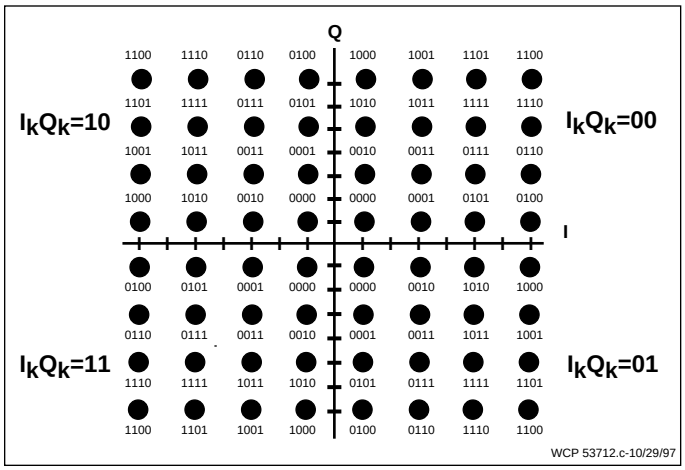


Figure 8. 64 QAM Constellation

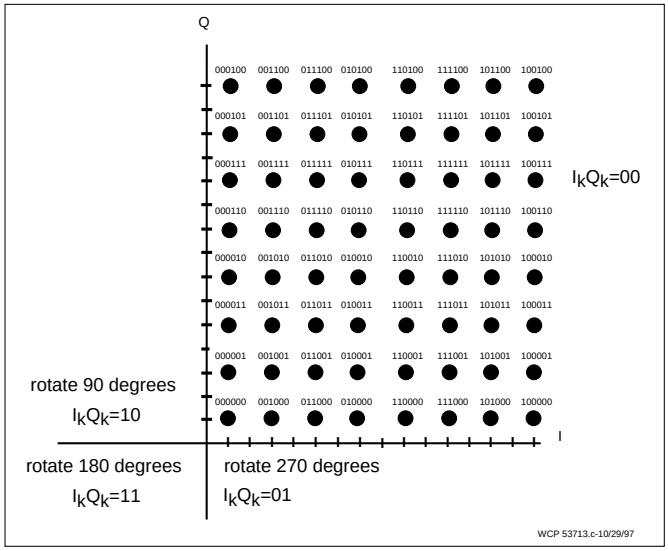


Figure 9. 256 QAM Constellation (DAVIC)

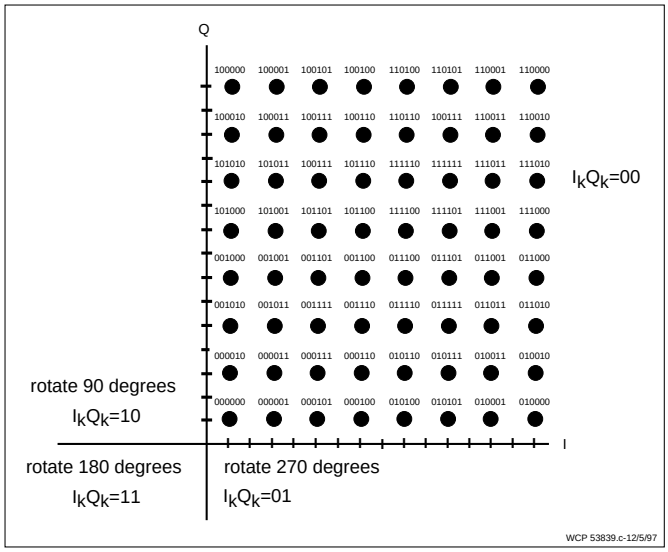


Figure 10. 256 QAM Constellation (DVB/IEEE 802.14)

Two bits are the same for each modulation type, and are identified as I_KQ_K. The remaining bits are identified as $[b_{q-1} \ldots b_{o]}$, where q = 2, 4, and 6 for 16, 64 or 256 QAM.

I_KQ_K are processed by the differential decoder before being fed to the frame sync block. The remaining bits $[b_{q-1} \ldots b_{o]}$ are fed directly to the frame sync.

Differential Decoder

Two bits (I_KQ_K) of each symbol are differentially decoded according to the equation:

$$b_{q+1} = A_k = (I_k \oplus I_{k-1}) \oplus (I_{k-1} \oplus Q_{k-1}) \bullet (1 \oplus I_k \oplus Q_k)$$

$$b_q = B_k = (Q_k \oplus Q_{k-1}) \oplus (I_{k-1} \oplus Q_{k-1}) \bullet (1 \oplus I_k \oplus Q_k)$$

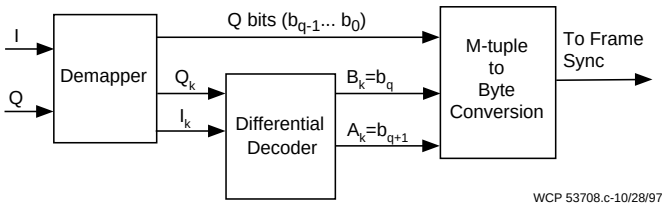


Figure 11. Demapper

Frame Sync

The frame sync receives symbols from the mapper. Each symbol represents 4, 6 or 8 bits for 16 QAM, 64 QAM, and 256 QAM respectively. These bits are collected into bytes. For 16 QAM, every two symbols are converted into one byte. For 64 QAM, every 4 symbols to are converted into 3 bytes, and for 256 QAM each symbol gives one byte..

Once bytes are formed, the frame sync block looks for a sequence of fixed byte values separated by 203 bytes of data.

47_H (203 bytes) $B8_H$ (203 bytes) 47_H (203 bytes) 47_H (203 bytes) $47_H \ldots 47_H \ldots 47_H \ldots . 47_H \ldots 47_H \ldots 47_H \ldots B8_H \ldots$

When the frame sync finds this pattern HIT (Block 1 Register 55_H) times, the frame sync block declares "acquisition" and starts feeding the bytes to the De-Interleaver. The frame sync stays in the "acquisition" state until it misses this pattern MISS (Block 1 Register 56_H) times.

De-Interleaver

This block is a convolutional De-Interleaver, as shown:

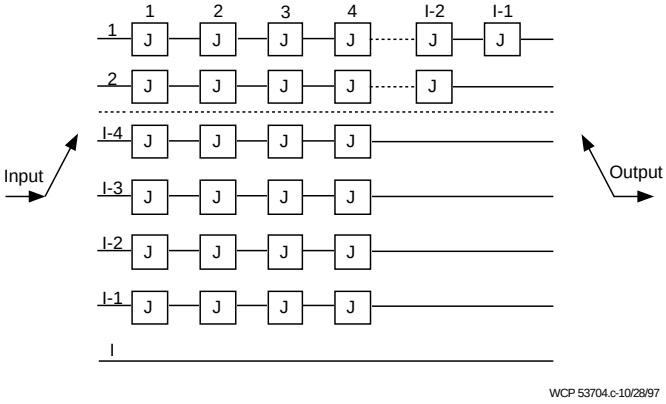


Figure 12. De-Interleaver

I and J are programmable (Block 1 Registers 47_H and 48_H).

A total memory of J _ (I-1) _ I/2 is required. The STEL-2176 has 8K internal memory. Up to 64K memory can be added externally without any additional logic, as shown.

Reed-Solomon Decoder

This function decodes Reed-Solomon blocks. Each code block is 204 bytes long and contains 188 bytes of data followed by 16 bytes of checksum. The code blocks are assumed to be coded according to ITU-T (J.83) Annex A FEC shortened R-S algorithm.

If the decoder fails to decode a code block, the decoder sets the undecodable flag "true" for this block. This flag propagates to the STEL-2176 output as RXDECDFLG.

In addition, the number of errors in each decodable block accumulates in Error_cnt[15:0] (Block 1 Registers 72_H and 73_H). This register can be reset by writing a 1 to CLR_ERR (bit 0 of Block 1 Register 74_H).

De-Randomizer

The de-randomizer is exactly the same as the randomizer described by the ITU-T (J.83) Annex A standard.

Output Clock Block

The function of the output clock block is to evenly distribute the output receive data of the STEL-2176 and to eliminate gaps caused by the FEC subsystem. The output of the Reed-Solomon decoder is 188 bytes of data for every 204 input bytes. Therefore, there is a gap of 16 bytes where the checksum information is removed.

The STEL-2176 output can send the received data in bytes on an 8-bit wide buss, or in bits on a single line as shown in Downstream Output Timing Diagrams (Figure 19 through Figure 21). Selecting between "bytewise" versus "bitwise" can be done by setting Serial Mode (bit 0 of Bank 1 Register 69_H) to 1.

ANNEX B

The ITU-T (J.83) Annex B FEC subsystem consists of the following blocks:

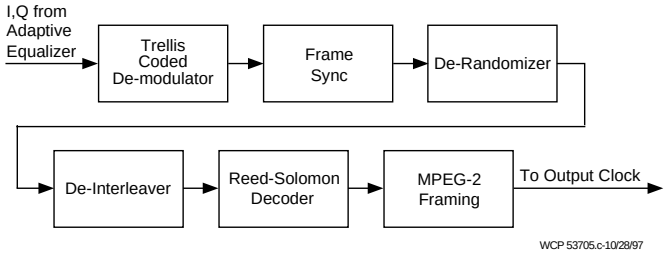


Figure 13. ITU-T (J.83) Annex B FEC Subsystem

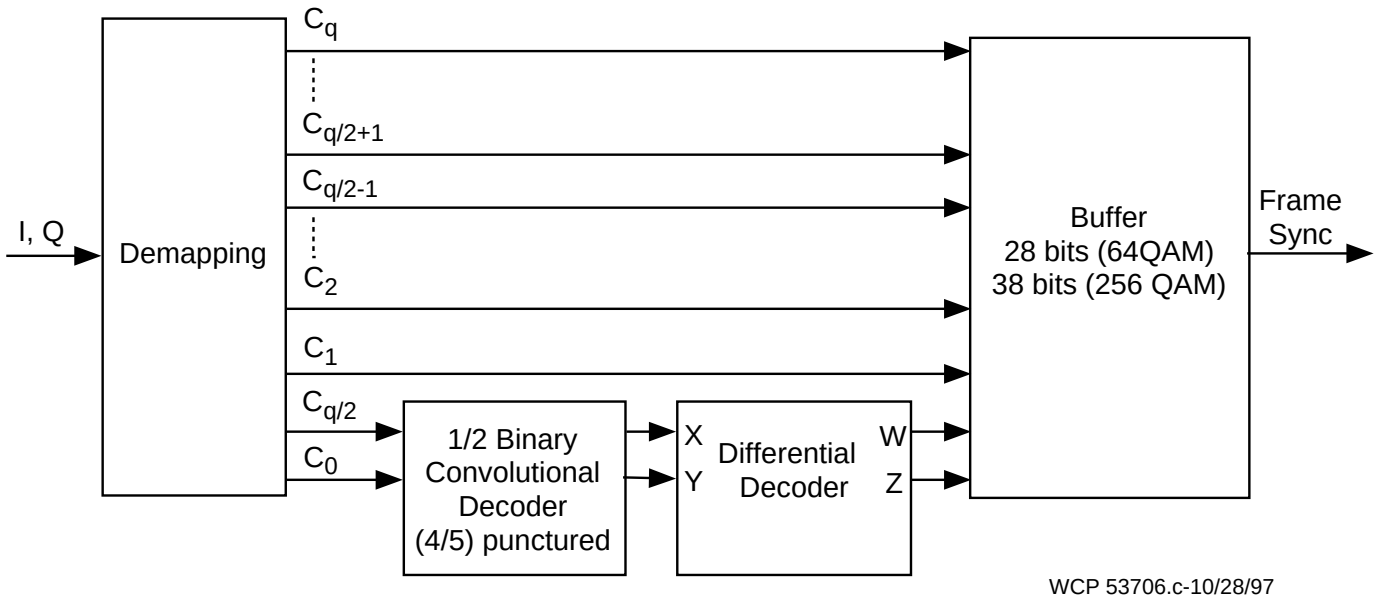


Figure 14. Trellis Coded Demodulator

The demapping block maps the Adaptive Channel Equalizer I and Q outputs for each symbol into 4, 6, or 8 bits for 16, 64, or 256 QAM respectively. The mapping tables are as follows:

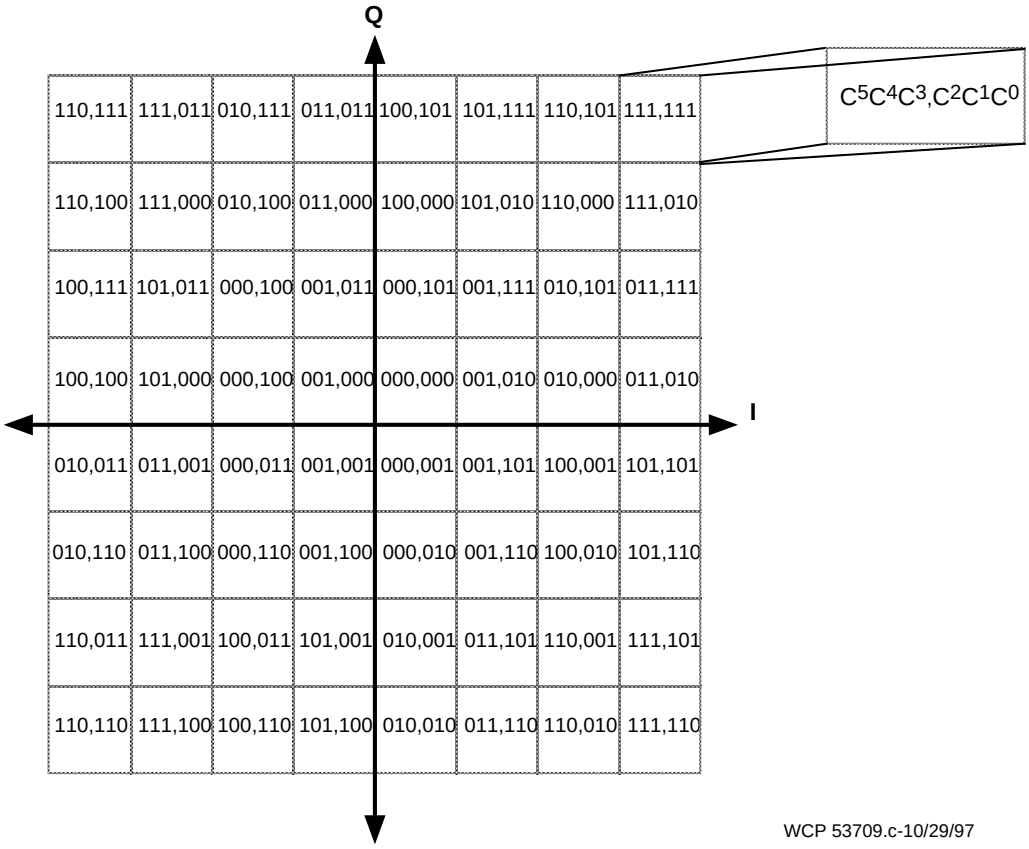


Figure 15. 64 QAM Mapping

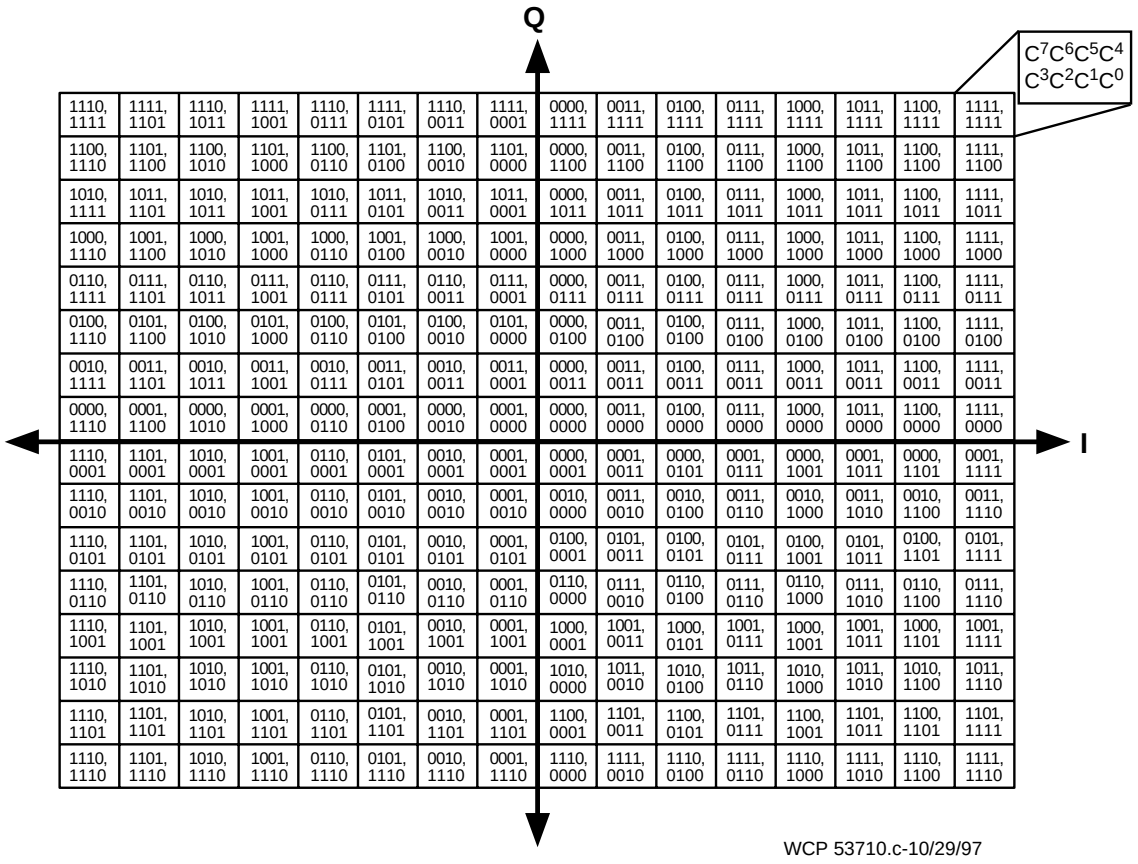


Figure 16. 256 QAM Mapping

The de-mapper generates "q" bits for each symbol where q = 6 for 64 QAM and q = 8 for 256 QAM. Two bits (b_o and $b_{q/2}$) are processed by the binary convolutional decoder and the differential decoder. The remaining bits are passed directly to the output buffer.

Viterbi Decoder

The binary convolutional decoder is a 1:2 Viterbi decoder (4/5 punctured). For every 5 consecutive input b_o or $b_q/2$ bits, the Viterbi decoder produces only 4 output bits. With this type of punctured code there are 5 possibilities for synchronization. The synchronization can occur automatically, or under manual control using the programmable registers. Setting VitFeedBackEn (bit 4 of Bank 0 Register $F4_H$) to 1 selects the automatic mode, while setting it to 0 selects the manual mode. In the manual mode, the decoder starts at any point in the puncturing sequence. To skip to the next state, write 1 to VitFeedBack (bit 7 of Bank 0, Register FC_H).

Differential Decoder

The two bit streams coming out of the Viterbi decoder are fed into the differential decoder. The differential decoder uses the following formula to produce its output:

$$W_k = (X_k \oplus X_{k-1}) \bullet (1 \oplus X_{k-1} \oplus Y_{k-1}) \oplus (Y_k \oplus Y_{k-1}) \bullet (X_{k-1} \oplus Y_{k-1})$$

$$Z_k = (X_k \oplus Y_{k-1}) \oplus (Y_k \oplus Y_{k-1})$$

Buffer

The trellis coded demodulator buffer converts groups of 5 symbols into a bitstream (28 bits for 64 QAM, or 38 bits for 256 QAM) following Annex B convention.

Frame Sync

This block receives data from the buffer. The frame sync looks for Annex B frame sync patterns which are different for 64 QAM and 256 QAM. Also, the separation distance between successive patterns is different (60 R-S code words for 64 QAM and 88 R-S code words for 256 QAM).

When the frame sync finds this pattern HIT (Bank 1 Register 55_H) times, the frame sync block declares "acquisition" and starts further processing of the data.

The frame sync stays in the "acquisition" state until it misses this pattern MISS (Bank 1 Register 56_H) times.

When in the "acquisition" state, the frame sync patterns are deleted, except the 4 bits identifying the interleaving parameters. These can be used by the De-Interleaver to automatically select the De-Interleaving parameters.

The remaining data, that is all bits between frame syncs, are formed in 7-table bits symbols and passed to the de-randomizer.

Derandomizer

The Derandomizer uses a linear feedback shift register as shown below. It works in GF (128). The delay elements are initialized at the beginning of each frame to $7F_H$, $7F_H$ and $7F_H$.

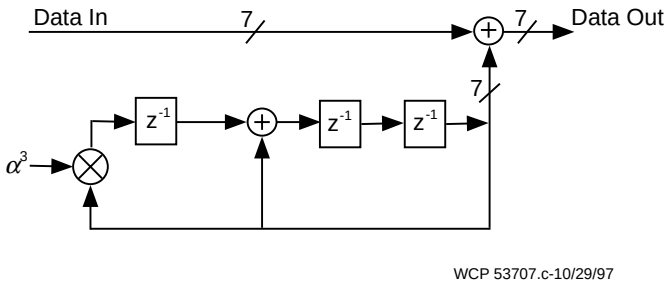


Figure 17. Derandomizer

De-Interleaver

This block is a convolutional De-Interleaver, as shown:

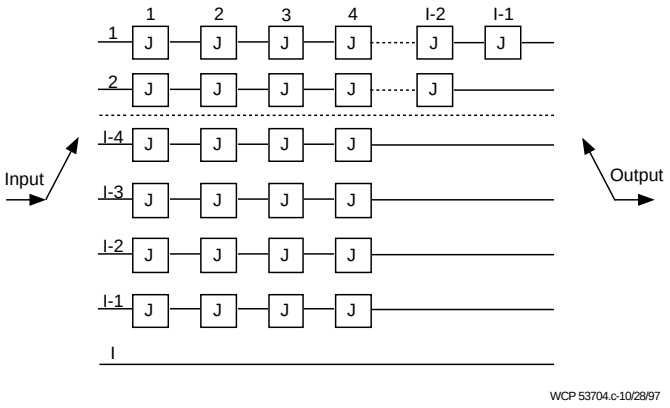


Figure 18. De-Interleaver

I and J (Bank 1 Registers 47_H and 48_H) are programmable, however in Level II, the I and J values are determined by the 4-bit pattern of the frame sync.

A total memory of J _ (I-1) _ I/2 is required. The STEL-2176 has 8K internal memory. Up to 64K memory can be added externally without any additional logic, as shown.

Reed-Solomon Decoder

This function decodes Reed-Solomon blocks. Each code block is 128 (7 bits symbols) long and contains 122 (7 bits symbols) of data followed by 6 (7 bits symbols) of checksum. The code blocks are assumed to be coded according to ITU-T (J.83) Annex B FEC R-S algorithm.

If the decoder fails to decode a code block, the decoder sets the undecodable flag "true" for this block. This flag propagates to the STEL-2176 RXDECDFLG output.

In addition, the number of errors in each decodable block accumulates in Error_cnt[15:0] (Bank 1 Registers 72_H and 73_H). This register can be reset by writing a 1 to CLR_ERR (bit 0 of Bank 1 Register 74_H).

MPEG Framing

The R-S decoder's output is serialized and fed through the ITU-T (J.83) Annex B MPEG-2 syndrome converter. The output of the syndrome generator is monitored for the pattern of 47_H separated by 1496 bits. When "n" (n is a programmable number) successive occurrences of this pattern are found, MPEG-2 frame sync is declared. MPEG-2 packets are framed by converting every 8 bits into one byte.

After declaring successful MPEG-2 frame sync, the absence of a valid code word at the expected location is indicated as a packet error.

MPEG-2 framing can be bypassed if so selected. In this case, the output of the R-S decoder will be reformed into bytes starting at the beginning of each frame.

Output Clock Block

The output clock block functionally the same as the Annex A output clock block. However, the gaps between data bytes occur due to eliminating the R-S checksum symbols, the frame sync information, and the bits that were added to support Viterbi decoding.

RECEIVE AND UNIVERSAL REGISTER DESCRIPTIONS

PROGRAMMING THE 2176 RECEIVE FUNCTIONS

The STEL-2176 has a combination of universal, receive and transmit registers. The registers are arranged as three banks of registers (Bank 0, Bank 1, and Bank 2). The Bank 0 registers are divided into Group 1 and Group 2 registers. The Bank 1 and 2 registers form separate groups (Groups 3 and 4 respectively). The Bank 0 and 1 registers (Groups 1, 2, and 3) are described by the following paragraphs. The Bank 2 registers (Group 4) are described in the Transmitter section (see page 54).

The Bank/Group address, shown below, must be written to register location FF_H to access the respective bank of registers. Register location FF_H can be accessed from each register bank/group. The registers can be accessed using the Microcontroller Interface's parallel or serial interface (see page 11).

REGISTER DESCRIPTIONS

Bank 0 - Universal Registers (Group 1)

The Universal Registers (Bank 0, Group 1) consist of three sets of registers: Read/Write (see Table 6), Read-only, and Write-only (see Table 7). The Read-only register set (Bank 0 Register F2) is for factory use only and not described by this User Manual.

Bank	Group	Group Name	Bank/Group Address (location FF_H)
0	1	Universal Registers (Group 1)	00_H
0	2	QAM Demodulator Registers Universal Registers (Group 2)	00_H
1	3	Downstream FEC Registers	01_H
2	4	Upstream, or transmitter, Registers	02_H

Table 6. Read/Write Register Set

Address	7	6	5	4	3	2	1	0
$F1_H$	Not Used				FECTestMode (Bypass QAM)	Factory Use Only Program to 0_H		
$F4_H$	Not Used		BypassMPE Gframe (write only)	VitFeedBackEn	Factory Defined Value - 0_H			
$F5_H$	Not Used				Factory Defined Value - 2_H		RxBypassFsyn	TxBypassFsyn
$F6_H$	Not Used	RxFsynM						
$F7_H$	Not Used	RxFsynN						
$F8_H$	Not Used	TxFsynM						
$F9_H$	Not Used	TxFsynN						
FA_H	Not Used							
FB_H	Not Used			Factory Use Only				
FD_H	QAMAcquisitionMaxTries							
FE_H	Not Used			QAMEnable	QAMType		FEC Type	

Table 7. Write Only Registers:

Address	7	6	5	4	3	2	1	0
$F3_H$	Not Used						Reset_OutputFIFO	Factory Defined Value - 0_H
FC_H	VitFeedBack	Factory Defined Value - 0_H		LoadRxM	LoadRxN	LoadTxM	LoadTxN	QAM Start

Bank 0, Group 1 Register Data Field Descriptions

BypassMPEGframe	This data field is a write only register. Setting it to 1 will bypass MPEG framing.
Factory Use Only	This data field is used by the factory and must be programmed to the value indicated above.
FEC Type	Used to select the type of FEC encoding: 00 ♉ Annex A 01 ♉ Annex B 10 ♉ STel use only
FECTestMode	For test purposes, the QAM can be bypassed by setting the value to 1. Data is then fed directly to the FEC.
LoadRxM	Setting the value to 1 loads the value of RxFsynM into the Receiver frequency synthesizer.
LoadRxN	Setting the value to 1 loads the value of RxFsynN into the Receiver frequency synthesizer.
LoadTxM	Setting the value to 1 loads the value of TxFsynM into the Transmitter frequency synthesizer.
LoadTxN	Setting the value to 1 loads the value of TxFsynN into the Transmitter frequency synthesizer.
QAM Start	Setting the value to 1 starts the QAM acquisition.
QAMAcquisitionMaxTries	The programmed value determines the number of acquisition tries the QAM makes before it declares an acquisition failure. The acquisition process will be restarted.
QAMEnable	QAMEnable must be set to 1 to enable the QAM circuitry, before programming QAM Start.
QAMType	Used to select 16, 64, or 256 QAM 00 ♉ 16 QAM 01 ♉ 64 QAM 10 ♉ 256 QAM
Reset_OutputFIFO	Setting the value to 1 resets the FIFO of the output clock in case of overflow.
RxBypassFsyn	Setting value to 1 bypasses the frequency synthesizer in the Master Receive Clock Generator.
RxFsynM	Value controls the Receiver Frequency Synthesizer output.
RxFsynN	Value controls the Receiver Frequency Synthesizer output.
TxBypassFsyn	Setting value to 1 bypasses the frequency synthesizer in the Master Transmit Clock Generator.
TxFsynM	Value controls the Transmitter Frequency Synthesizer output.
TxFsynN	Value controls the Transmitter Frequency Synthesizer output.
VitFeedBack	When use of Viterbi Decoder feedback is enabled, setting the value to 1 forces the Frame Sync circuit to begin shifting by one symbol and testing for the start of the symbol group. Once the search is externally initiated the value should be returned to 0.
VitFeedBackEn	Setting the value to 1 enables the use of Viterbi Decoder feedback for using the VitFeedBack register to force the Frame Sync circuit to search for the start of the symbol group.

Bank 0 - QAM Demodulator Registers Universal Registers (Group 2)

The QAM Demodulator Registers Universal Registers are divided into 6 sub-groups of registers. Each sub-group has two sets of registers: a Read/Write set which is used for control purposes, and a Read-only set for monitoring purposes. The sub-groups are:

Sub-Group	Name	Read/Write Register Addresses	Read-only Register Addresses
A	Control, address range	00_H to $0E_H$	40_H to 45_H
B	DDC, Nyquist, AGC, and AFC address range	$0F_H$ to $1B_H$	46_H to 52_H
C	Timing, address range	$1C_H$ to 20_H	53_H to $5B_H$
D	FFE, address range	21_H to 24_H	$5C_H$ to $5F_H$ and $6B_H$ to $9A_H$
E	FBE, address range	25_H to 26_H	$9B_H$ to $B2_H$
F	PLL, address range	27_H to $3F_H$	60_H to $6A_H$

Bank 0, Group 2, Sub-Group 'A' - Control Address Range Registers

Table 8. Group 2, Sub-Group 'A' Read/Write Registers

Address	7	6	5	4	3	2	1	0
00_H	QAM_Enable	QAM_SoftResetEnable	Pwrlvl_correctEn	Decimate_GainSel	Factory Defined Value - A_H			
01_H	Factory Defined Value - 19_H							
02_H	Factory Defined Value - 44_H							
03_H	Factory Defined Value - 19_H							
04_H	CMA1_Ksym							
05_H	AFC1_Ksym							
06_H	CMA2_Ksym							
07_H	AFC2_Ksym							
08_H	Factory Defined Value - 64_H							
09_H	Factory Defined Value - 00_H							
$0A_H$	Factory Defined Value - 00_H							
$0B_H$	Factory Defined Value - 64_H							
$0C_H$	Factory Defined Value - 40_H = 16 QAM, 53_H = 64 QAM, or 87_H = 256 QAM							
$0D_H$	Factory Defined Value - 33_H = 16 QAM, 37_H = 64 QAM, or 54_H = 256 QAM							
$0E_H$	Factory Defined Value - $5F_H$ = 16 QAM, 76_H = 64 QAM, or $A4_H$ = 256 QAM							

Table 9. Sub-Group 'A' Read-Only Registers

Address	7	6	5	4	3	2	1	0
40_H	SymbolCnt[1:0]		AcquisitionLock	AcquisitionFail	State			
41_H	SymbolCnt[9:2]							
42_H	SymbolKCnt							
43_H	AcquireCnt							
44_H	ErrPwr							
45_H	JitPwr							

Bank 0, Group 2, Sub-Group 'A' Register Data Field Descriptions

AcquireCnt	The value indicates the number of times the STEL-2176 has attempted to acquire the signal.
AcquisitionFail	The value is set to 1 when an acquisition failure is declared due to excessive error power; the STEL-2176 is also returned to the idle mode.
AcquisitionLock	The value is set to 1 when acquisition lock is detected.
Decimate_GainSel	If GainSel is low (the default), the Nyquist filter output (10 bits plus 1 fractional bit) is multiplied by a factor of 1.25 (+2 dB power); if GainSel is high, the scale factor is 1.5 (+3.5 dB power).
ErrPwr	Provides an indication of the SNR. The conversion between ErrPwr and the SNR can be determined from Table 10 (intermediate values can be found by interpolation).
Factory Defined Value	The specified value must be written to the data field. In a few cases, several values are provided for selecting a specific mode and one of the specified values must be written to the data field.
JitPwr	
Pwrlvl_correctEn	Enables the power level adjuster to correct for deviations in the signal power due to adjacent channel interference.
QAM_Enable	
QAM_SoftResetEnable	The value is set to 1 to enable soft reset of the QAM.
State	
SymbolCnt[9:0]	
SymbolKCnt	

Table 10. SNR to ErrPwr Conversion

	ErrPwr		
SNR(dB)	**256 QAM**	**64 QAM**	**16 QAM**
34	18		
33	23		
32	28		
31	36		
30	44		
29	55		
28	69		
27	84	23	
26	100	28	
25	118	35	
24	135	44	
23	151	55	
22	164	68	
21	176	83	20
20	185	101	26
19		118	33
18		137	41
17		155	51
16		171	64
15		185	78
14		198	95
13			113
12			131
11			148
10			163
9			174
8			184

Bank 0, Group 2, Sub-Group 'B' - DDC, Nyquist, AGC, and AFC Address Range Registers

Table 11. Group 2, Sub-Group 'B' Read/Write Registers

Address	7	6	5	4	3	2	1	0
$0F_H$	Factory Defined Value - 34_H						UpdateEn	Correct_ addsub
10_H	DeltaTheta_in[5:0]						CorrectEn	Update_ addsub
11_H	DeltaTheta_in[13:6]							
12_H	AGC_GainSel				Nyquist_AlphaSel		AGC_InvertOutputB	AGC_Invert OutputA
13_H	Factory Defined Value - 00_H							
14_H	AGC_ThresholdA							
15_H	AGC_ThresholdB							
16_H	Factory Defined Value - 22_H = 16 QAM, $2B_H$ = 64 QAM, or 35_H = 256 QAM							
17_H	Factory Defined Value - 26_H 16 QAM, 37_H 64 QAM, or $3C_H$ 256 QAM							
18_H	Factory Defined Value - 52_H = Signal BW ~5MHz or $3B_H$ = Signal BW ~7MHz							
19_H	AFC_Cntr_stop1							
$1A_H$	AFC_Cntr_stop2							
$1B_H$	WARNING: SHOULD NOT BE PROGRAMMED BY THE USER							

Table 12. Group 2, Sub-Group 'B' Read-Only Registers

Address	7	6	5	4	3	2	1	0
46_H	Factory Use Only							
47_H	Factory Use Only							
48_H	DDC_DeltaTheta[3:0]							
49_H	DDC_DeltaTheta[11:4]							
$4A_H$	Factory Use Only						DDC_DeltaTheta [13:12]	
$4B_H$	Factory Use Only							
$4C_H$	Factory Use Only							
$4D_H$	Factory Use Only							
$4E_H$	Factory Use Only							
$4F_H$	AGC_PowerEstimate[7:0]							
50_H	Factory Use Only						AGC_PowerEstimate[9:8]	
51_H	Factory Use Only							
52_H	Factory Use Only							

Bank 0, Group 2, Sub-Group 'B' Register Data Field Descriptions

AFC_Cntr_stop1[7:0]	Set the upper limit for the first frequency offset estimate.
AFC_Cntr_stop2[7:0]	Set the upper limit for the second frequency offset estimate.
AGC_GainSel[3:0]	Sets the gain of the AGC. The effective gain is $1/(2^{GainSel})$. GainSel defaults to 2, and will normally range from 2 to 8.
AGC_InvertOutputA	InvertOutputA is a checkbutton that inverts the polarity of the AGC's output bits (default is off). When InvertOutput is off, then a low AGC output bit means that the current power estimate is greater than the corresponding Threshold.
AGC_InvertOutputB	InvertOutputB is a checkbutton that inverts the polarity of the AGC's output bits (default is off). When InvertOutput is off, then a low AGC output bit means that the current power estimate is greater than the corresponding Threshold.
AGC_PowerEstimate[9:0]	
AGC_ThresholdA[7:0]	There are two gain amplifiers. ThresholdA sets the AGC`s power threshold (0 to 2^8-1) of one amplifier. For 256-QAM, the value ranges from about 75 to 100 (default is 96), depending on the desired A/D clipping level.
AGC_ThresholdB[7:0]	There are two gain amplifiers. ThresholdB sets the AGC`s power threshold (0 to 2^8-1) of one amplifier. For 256-QAM, the value ranges from about 75 to 100 (default is 96), depending on the desired A/D clipping level.
Correct_addsub Update_addsub	Correct_addsub should always be the opposite of Update_addsub. Update_addsub controls which way the NCO rotates, thereby selecting either the positive or negative passband sidelobe. This allows spectrum inversion. The hardware default value is 1, which selects the positive sidelobe (spectrum inversion off).
CorrectEn	CorrectEn should be set to 1. When set to 0, the DDC ignores the AFC's frequency correction.
DDC_DeltaTheta	
DeltaTheta_in[13:0]	DeltaTheta_in[13:0] sets the initial phase increment of the NCO, thereby specifying the carrier frequency, f_c. DeltaTheta_in should be initialized depending on the carrier and the sampling frequencies: DeltaTheta_in = round ($f_c/f_s * 2^{14}$), where f_s is the sample clock frequency. Note that f_s will be 25 to 30 MHz and f_c will be 6 MHz or 7 MHz. E.g., for $f_c = 6$ and $f_s = 25$, DeltaTheta_in = $6/25 * 2^{14} = 3932$ fc = (DeltaTheta_in/2^{14}) * f_s,
Factory Defined Value	The specified value must be written to the data field. In a few cases, several values are provided for selecting a specific mode and one of the specified values must be written to the data field.
Factory Use Only	This data field is used by the factory and its function is not related to the STEL-2176 receive and transmit characteristics.
Nyquist_AlphaSel[1:0]	Selects the excess BW of the Nyquist matched filter: 00 -> 12% 01 -> 15% 10 -> 18% 11 -> not valid
UpdateEn	Should be set to 1. When set to 0, the DDC's NCO is frozen.
WARNING: SHOULD NOT BE PROGRAMMED BY THE USER	This data field is used by the factory and the programmed value will affect the STEL-2176 receive and transmit characteristics. The factory programmed value should not be changed by the user. If inadvertently changed, the receiver must be reset.

Bank 0, Group 2, Sub-Group 'C' - Timing Address Range Register

Table 13. Group 2, Sub-Group 'C' Read/Write Registers

Address	7	6	5	4	3	2	1	0
$1C_H$	Factory Defined Value - 14_H							
$1D_H$	Ratio_in[5:2]				Factory Defined Value - 3_H			
$1E_H$	Ratio_in[13:6]							
$1F_H$	Ratio_in[21:14]							
20_H	Factory Defined Value - 42_H							

Table 14. Group 2, Sub-Group 'C' Read-Only Registers

Address	7	6	5	4	3	2	1	0
53_H	Factory Use Only							
54_H	Factory Use Only							
55_H	Factory Use Only							
56_H	Ratio_out[1:0]		Factory Use Only					
57_H	Ratio_out[9:2]							
58_H	Ratio_out[17:10]							
59_H	Factory Use Only				Ratio_out[21:18]			
$5A_H$	Pwrlvl_PowerEstimate[6:0]							Factory Use Only
$5B_H$	Factory Use Only				Pwrlvl_powerEstimate[10:7]			

Bank 0, Group 2, Sub-Group 'C' Register Data Field Descriptions

Factory Defined Value — The specified value must be written to the data field. In a few cases, several values are provided for selecting a specific mode and one of the specified values must be written to the data field.

Factory Use Only — This data field is used by the factory and its function is not related to the STEL-2176 receive and transmit characteristics.

Pwrlvl_powerEstimate[10:0]

Ratio_in[21:2]

Ratio_out[21:0]

Bank 0, Group 2, Sub-Group 'D' - FFE Address Range Registers

Table 15. Group 2, Sub-Group 'D' Read/Write Registers

Address	7	6	5	4	3	2	1	0
21_H	Factory Defined Value - 2_H = 16 QAM, 0_H = 64 QAM, or 3_H = 256 QAM		DDenable	UpdateEn	CenterTapAddr			
22_H	Factory Defined Value - $1A_H$ =16 QAM, $1D_H$ = 64 QAM, or $1D_H$ = 256 QAM							
23_H	ShiftSel_W3[1:0]		ShiftSel_W2[2:0]			ShiftSel_W1[2:0]		Factory Defined Value - 0_H
24_H	Factory Defined Value - 0_H	ShiftSel_W5[2:0]			ShiftSel_W4[2:0]			ShiftSel_W3[2]

Table 16. Group 2, Sub-Group 'D' Read-Only Registers

Address	7	6	5	4	3	2	1	0
$5C_H$	Factory Use Only							
$5D_H$	Factory Use Only							
$5E_H$	Factory Use Only							
$5F_H$	Factory Use Only							
$6B_H$	WI0[7:0]							
$6C_H$	WI0[15:8]							
$6D_H$	WQ0[7:0]							
$6E_H$	WQ0[15:8]							
$6F_H$	WI1[7:0]							
70_H	WI1[15:8]							
71_H	WQ1[7:0]							
72_H	WQ1[15:8]							
73_H	WI2[7:0]							
74_H	WI2[15:8]							
75_H	WQ2[7:0]							
76_H	WQ2[15:8]							
77_H	WI3[7:0]							
78_H	WI3[15:8]							
79_H	WQ3[7:0]							
$7A_H$	WQ3[15:8]							
$7B_H$	WI4[7:0]							
$7C_H$	WI4[15:8]							
$7D_H$	WQ4[7:0]							
$7E_H$	WQ4[15:8]							
$7F_H$	WI5[7:0]							
80_H	WI5[15:8]							
81_H	WQ5[7:0]							
82_H	WQ5[15:8]							
83_H	WI6[7:0]							
84_H	WI6[15:8]							
85_H	WQ6[7:0]							
86_H	WQ6[15:8]							
87_H	WI7[7:0]							
88_H	WI7[15:8]							
89_H	WQ7[7:0]							
$8A_H$	WQ7[15:8]							
$8B_H$	WI8[7:0]							
$8C_H$	WI8[15:8]							
$8D_H$	WQ8[7:0]							
$8E_H$	WQ8[15:8]							
$8F_H$	WI9[7:0]							
90_H	WI9[15:8]							
91_H	WQ9[7:0]							
92_H	WQ9[15:8]							
93_H	WI10[7:0]							
94_H	WI10[15:8]							
95_H	WQ10[7:0]							
96_H	WQ10[15:8]							
97_H	WI11[7:0]							
98_H	WI11[15:8]							
99_H	WQ11[7:0]							
$9A_H$	WQ11[15:8]							

Bank 0, Group 2, Sub-Group 'D' Register Data Field Descriptions

CenterTapAddr	Defines which the taps address that will be set as the "center-tap". There are 12 taps in the FFE that can be designated as the center-tap (0 to 11).
DDenable	Allows the FFE to switch to “decision-directed” (DD) mode; otherwise the FFE will remain in its "blind" equalization mode, aka CMA (constant modulus algorithm) mode.
Factory Defined Value	The specified value must be written to the data field. In a few cases, several values are provided for selecting a specific mode and one of the specified values must be written to the data field.
Factory Use Only	This data field is used by the factory and its function is not related to the STEL-2176 receive and transmit characteristics.
ShiftSel_W1[2:0]	The setting specifies the step size of the FFE, the nominal value is 2.
ShiftSel_W2[2:0]	The setting specifies the step size of the FFE, the nominal value is 2.
ShiftSel_W3[2:0]	The setting specifies the step size of the FFE, the nominal value is 2.
ShiftSel_W4[2:0]	The setting specifies the step size of the FFE, the nominal value is 2.
ShiftSel_W5[2:0]	ShiftSel_W5[2:0] sets the step size when the PLL is acquiring.
UpdateEn	Enables update of the feedforward equalizer (FFE).
WI0[15:0] to WI11[15:0]	Current in-phase feedforward equalizer coefficients.
WQ0[15:0] to WO11[15:0]	Current quadratic feedforward equalizer coefficients.

Bank 0, Group 2, Sub-Group 'E' - FBE Address Range Registers

Table 17. Group 2, Sub-Group 'E' Read/Write Registers

Address	7	6	5	4	3	2	1	0
25_H	Factory Defined Value - 7_H			Update_En	Factory Defined Value - 1_H		ShiftSel_W_DD[1:0]	
26_H	Factory Defined Value - $7F_H$							

Table 18. Group 2, Sub-Group 'E' Read-Only Registers

Address	7	6	5	4	3	2	1	0
$9B_H$	WI0[7:0]							
$9C_H$	WQ0[3:0]				WI0[11:8]			
$9D_H$	WQ0[[11:4]							
$9E_H$	WI1[7:0]							
$9F_H$	WQ1[3:0]				WI1[11:8]			
$A0_H$	WQ1[[11:4]							
$A1_H$	WI2[7:0]							
$A2_H$	WQ2[3:0]				WI2[11:8]			
$A3_H$	WQ2[[11:4]							
$A4_H$	WI3[7:0]							
$A5_H$	WQ3[3:0]				WI3[11:8]			
$A6_H$	WQ3[[11:4]							
$A7_H$	WI4[7:0]							

$A8_H$	WQ4[3:0]	WI4[11:8]
$A9_H$	WQ4[[11:4]	
AA_H	WI5[7:0]	
AB_H	WQ5[3:0]	WI5[11:8]
AC_H	WQ5[[11:4]	

Bank 0, Group 2, Sub-Group 'E' Register Data Field Descriptions

Factory Defined Value	The specified value must be written to the data field. In a few cases, several values are provided for selecting a specific mode and one of the specified values must be written to the data field.
ShiftSel_W_DD	Sets the step size for the FBE when the system initially switches the equalizers to DD mode.
Update_En	Enables update of the feedback equalizer (FBE).
WI0[11:0] to WI5[[11:0]	Current in-phase feedback equalizer coefficients.
WQ0[11:0] to WQ5[[11:0]	Current quadratic feedback equalizer coefficients.

Bank 0, Group 2, Sub-Group 'F' - PLL Address Range Registers

Table 19. Group 2, Sub-Group 'F' Read/Write Registers

Address	7	6	5	4	3	2	1	0
27_H	Factory Defined Value - 64_H							
28_H	Factory Defined Value - $2A_H$							
29_H	Factory Defined Value - $F4_H$							
$2A_H$	Factory Defined Value - $D6_H$							
$2B_H$	Factory Defined Value - 64_H							
$2C_H$	Factory Defined Value - $2A_H$							
$2D_H$	Factory Defined Value - $F4_H$							
$2E_H$	Factory Defined Value - $D6_H$							
$2F_H$	Factory Defined Value - 64_H							
30_H	Factory Defined Value - $2A_H$							
31_H	Factory Defined Value - $F4_H$							
32_H	Factory Defined Value - $D6_H$							
33_H	Factory Defined Value - $3F_H$							
34_H	FBE_ShiftSel_W_Lock		FFE_ShiftSel_W_Lock			FFE_ShiftSel_W_DD		
35_H	Factory Defined Value - 80_H							
36_H	Factory Defined Value - 00_H							
37_H	Factory Defined Value - $3F_H$							
38_H	Factory Defined Value - 3_H		Factory Defined Value - $1F_H$					UpdateEn
39_H	Factory Defined Value - $1F_H$					Factory Defined Value - 7_H		
$3A_H$	Factory Defined Value - 88_H							
$3B_H$	Factory Defined Value - 14_H							
$3C_H$	Factory Defined Value - 88_H							
$3D_H$	Factory Defined Value - 14_H							
$3E_H$	Factory Defined Value - 88_H							
$3F_H$	Factory Defined Value - 14_H							

Table 20. Group 2, Sub-Group 'F' Read-Only Registers

Address	7	6	5	4	3	2	1	0
60_H to 68_H	Factory Use Only							
69_H	[7:0]							
$6A_H$	DeltaPhase[15:8]							

Bank 0, Group 2, Sub-Group 'F' Register Data Field Descriptions

DeltaPhase[15:0]	Specifies the initial value for the PLL's phase increment.
Factory Defined Value	The specified value must be written to the data field. In a few cases, several values are provided for selecting a specific mode and one of the specified values must be written to the data field.
Factory Use Only	This data field is used by the factory and its function is not related to the STEL-2176 receive and transmit characteristics.
FBE_ShiftSel_W_Lock[1:0]	Sets the step size of the FBE when the system has "locked" (steady-state operation).
FFE_ShiftSel_W_DD[2:0]	Sets the step size of the FFE when the system initially switches the equalizers to DD mode
FFE_ShiftSel_W_Lock[2:0]	Sets the step size of the FFE when the system has "locked" (steady-state operation).
UpdateEn	UpdateEn should be high; if UpdateEn is low, the PLL is disabled.

Bank 1 - FEC Registers (Group 3)

The QAM Demodulator Registers Universal Registers are divided into 7 sub-groups of registers. Each sub-group can have a Read/Write set of registers which are used for control purposes, a Read-only set which are used for monitoring purposes, or a combination of both types of registers. The sub-groups are:

Sub-Group	Name	Read/Write Register Addresses	Read-only Register Addresses
A	Viterbi and De-Mapper	00_H	Not Used
B	De-Randomizer	Not Used	41_H
C	De-Interleaver	45_H to 48_H	43_H to 44_H and 49_H to $4A_H$
D	MPEG Frame Sync	$4B_H$ to $4E_H$	$4F_H$ to 52_H
E	Frame Sync	53_H to 57_H	58_H to 65_H
F	Output Clk	66_H to $6A_H$	Not Used
G	Reed-Solomon Decoder	70_H ,71_H, and 74_H	72_H to 73_H

Bank 1, Group 3, Sub-Group 'A' - Viterbi and De-Mapper Registers

Table 21. Group 3, Sub-Group 'A' Read/Write Registers

Address	7	6	5	4	3	2	1	0
00_H	DVB & IEEE 802.14 map						Factory Defined Value - 3_H	

Bank 1, Group 3, Sub-Group 'A' Register Data Field Descriptions

DVB & IEEE 802.14 map — Set the value to 1 to select 256 QAM DVB & IEEE 802.14 demapper, 0 selects the DAVIC 256 QAM demapper.

Factory Defined Value — The specified value must be written to the data field. In a few cases, several values are provided for selecting a specific mode and one of the specified values must be written to the data field.

Bank 1, Group 3, Sub-Group 'B' - De-Randomizer Registers

Table 22. Group 3, Sub-Group 'B' Read-Only Registers

Address	7	6	5	4	3	2	1	0
41_H	Not Used	DataOut[6:0]						

Bank 1, Group 3, Sub-Group 'B' Register Data Field Descriptions

DataOut

Bank 1, Group 3, Sub-Group 'C' - De-Interleaver Registers

Table 23. Group 3, Sub-Group 'C' Read/Write Registers

Address	7	6	5	4	3	2	1	0
45_H	Not used						ShadowMode	Level2
46_H	Not used							TestMode
47_H	I_test							
48_H	Not used			J_test				

Table 24. Group 3, Sub-Group 'C' Read-Only Registers

Address	7	6	5	4	3	2	1	0
43_H	I_test							
44_H	J_test							
49_H	SRAM_addr[15:8]							
$4A_H$	SRAM_addr[7:0]							

Bank 1, Group 3, Sub-Group 'C' Register Data Field Descriptions

I_test (Read/Write)	The I value used during test mode.
I_test (Read-Only)	Read register that permits looking at I value when the interleaver is running during test.
J_test (Read/Write)	The J value used during test mode.
J_test (Read-Only)	Read register that permits looking at J value when the interleaver is running during test.
Level2	There are two distinct operating modes of interleaving for Annex B. If Level2 is 1, the depth of interleaving is variable and depends on a control word from Frame Sync. If Level2 is 0 (level 1), interleaving is always 128 X 1; the control word does not matter.
ShadowMode	There is 8 Kbytes of internal memory for the interleaver. In normal operation, the interleaver first fills up its internal memory, then uses external memory. If Shadow mode is 1, internal memory is bypassed.
SRAM_addr[15:0]	The address is used by the interleaver to access the SRAM. For Annex A, 256-QAM requires external SRAM.
TestMode	The Interleaving type is set elsewhere by selecting QAM and Annex type. Setting this register to 1, enables use of the I and J values stored in the I_test and J_test Read/Write registers.

Bank 1, Group 3, Sub-Group 'D' - MPEG FrameSync Registers

Table 25. Group 3, Sub-Group 'D' Read/Write Registers

Address	7	6	5	4	3	2	1	0
$4B_H$	HIT							
$4C_H$	MISS							
$4D_H$	SyncSymbol							
$4E_H$	Not used							OP_ERR

Table 26. Group 3, Sub-Group 'D' Read-Only Registers

Address	7	6	5	4	3	2	1	0
$4F_H$	Factory Use Only							
50_H	Factory Use Only							
51_H	Factory Use Only							
52_H	Factory Use Only							

Bank 1, Group 3, Sub-Group 'D' Register Data Field Descriptions

Factory Use Only	This data field is used by the factory and its function is not related to the STEL-2176 receive and transmit characteristics.
HIT	The number of Syncs that must be detected before data is output.
MISS	The number of misses before the MPEG Frame Sync state machine goes into idle.
OP_ERR	Setting the value to 1 enables flagging of data errors via the checksum in the Frame Sync byte.
SyncSymbol	Used in Annex A only to input an arbitrary MPEG FRAME sync symbol; normally 47_H.

Bank 1, Group 3, Sub-Group 'E' - FrameSync Registers

Table 27. Group 3, Sub-Group 'E' Read/Write Registers

Address	7	6	5	4	3	2	1	0
53_H	ErrorTolerance[5:0]						ErrorTolEn	NoMissMode
54_H	TRACK[7:0]							
55_H	HIT[7:0]							
56_H	MISS[7:0]							
57_H	SyncSymbol[7:0]							

Table 28. Group 3, Sub-Group 'E' Read-Only Registers

Address	7	6	5	4	3	2	1	0
58_H to 65_H	Factory Use Only							

Bank 1, Group 3, Sub-Group 'D' Register Data Field Descriptions

Factory Use Only	This data field is used by the factory and its function is not related to the STEL-2176 receive and transmit characteristics.
NoMissMode	If NoMissMode is 1, then once Frame Sync is acquired the state machine will never go to the idle mode, even if all data is bad.
ErrorTolEn	If ErrorTolEn is 1, then all bits in the Frame Sync sequence must match the expected pattern. This is for Annex B only.
ErrorTolerance	Sets the number of bits that can be wrong in the Frame Sync sequence and have the sequence considered valid.
TRACK	The number of frames the Frame Sync state machine must detect before telling the Viterbi that data should be realigned. This is for Annex B only.
HIT	The number of Syncs that must be detected before data is output.
MISS	The number of misses before the Frame Sync state machine goes into idle.
SyncSymbol	Used in Annex A only to input an arbitrary FRAME sync symbol; normally 47_H.

Bank 1, Group 3, Sub-Group 'F' - OutputClk Registers

Table 29. Group 3, Sub-Group 'F' Read/Write Registers

Address	7	6	5	4	3	2	1	0
66_H	Nominal_value[7:0]							
67_H	Nominal_Value[15:8]							
68_H					Nominal_Value[19:16]			
69_H	Not Used					ByPass Mode	LSB_First	Serial Mode
$6A_H$	Not Used				Scale[3:0]			

Bank 1, Group 3, Sub-Group 'F' Register Data Field Descriptions

ByPass Mode — Setting to 0, enables output clock block to eliminate gaps between MPEG frames.

LSB_First — set

Nominal_Value[19:0] — The 20-bit value is programmed according to the Annex and QAM type, as shown below. It controls how fast the output clock is operating by setting the ratio of the high speed clock to the output clock.

	Annex A	Annex B	STEL Use Only
16-QAM			
64-QAM			
256-QAM			

Scale — Controls the amount of jitter in the output clock. If Scale is set to low, acquisition of the input data will be slower (i.e., locking onto it will take longer) but the clock will be smoother.

Serial Mode — If Serial Mode is 1, the data is serial.

Bank 1, Group 3, Sub-Group 'G' - Reed-Solomon Decoder Registers

Table 30. Group 3, Sub-Group 'G' Read/Write Registers

Address	7	6	5	4	3	2	1	0
70_H	Factory Defined Value - CC_H = Annex A:, 80_H = Annex B:							
71_H	Not Used			OutputDataRate				
74_H	Not Used							CLR_ERR

Table 31. Group 3, Sub-Group 'G' Read-Only Registers

Address	7	6	5	4	3	2	1	0
72_H	Error_cnt[7:0]							
73_H	Error_cnt[15:8]							

Bank 1, Group 3, Sub-Group 'G' Register Data Field Descriptions

Factory Defined Value — The specified value must be written to the data field. In a few cases, several values are provided for selecting a specific mode and one of the specified values must be written to the data field.

CLR_ERR — Clears the Error_cnt register

Error_cnt[15:0] — Error_cnt[7:0] is byte 0 of the number of errors found in a block and Error_cnt[15:8] is byte 1 of the number of errors found in a block.

OutputDataRate — The value to be written to the OutputDataRate data field is dependent on the value of Register FE_H[3:0].

When Register FE_H[3:0] is:	**OutputDataRate[4:0] should be set to:**
0_H	10_H
1_H	Not Valid
2_H	10_H
4_H	$0A_H$
5_H	08_H
6_H	$0A_H$
8_H	08_H
9_H	07_H
A_H	Not Valid

TIMING

The basic input to the receiver is an analog input; basic outputs consist of data (serial or parallel), an output clock and a frame sync. These outputs are shown in the four timing diagrams that follow.

There are four output modes depending on whether there are gaps between frames and depending on whether the data output is parallel (8 bit) or serial.

The addition of the Read-Solomon checksum creates gaps in the transmission of the MPEG-2 frame. But the STEL-2176 provides the option of spreading the gap over a frame so there appears to be no gap. For gap or no-gap mode, data may be parallel or serial.

The four modes are as follows:

NO GAP, PARALLEL MODE

Here Frame-Sync/ indicates the first byte of an MPEG-2 frame, and Output Clock is approximately 50% of the byte period. There are 188 bytes in a frame with one byte per symbol.

NO GAP, SERIAL MODE

This is similar to the above. Here the frame length is 8 X 188 bits, and the Output Clock is for a bit period rather than a byte period.

GAPS, PARALLEL MODE

In this mode there are two differences:

The Output Clock is now approximately 8 nanoseconds.

The Output Clock goes for 188 bytes, then the data and clock stop until Frame-Sync/ is asserted again.

GAPS, SERIAL MODE

This mode is the same as above, but here the bytes are serialized. There are 8 X 188 clocks and 8 X 188 bits per Frame-Sync/.

DOWNSTREAM OUTPUT TIMING (SERIAL DATA OUTPUT)

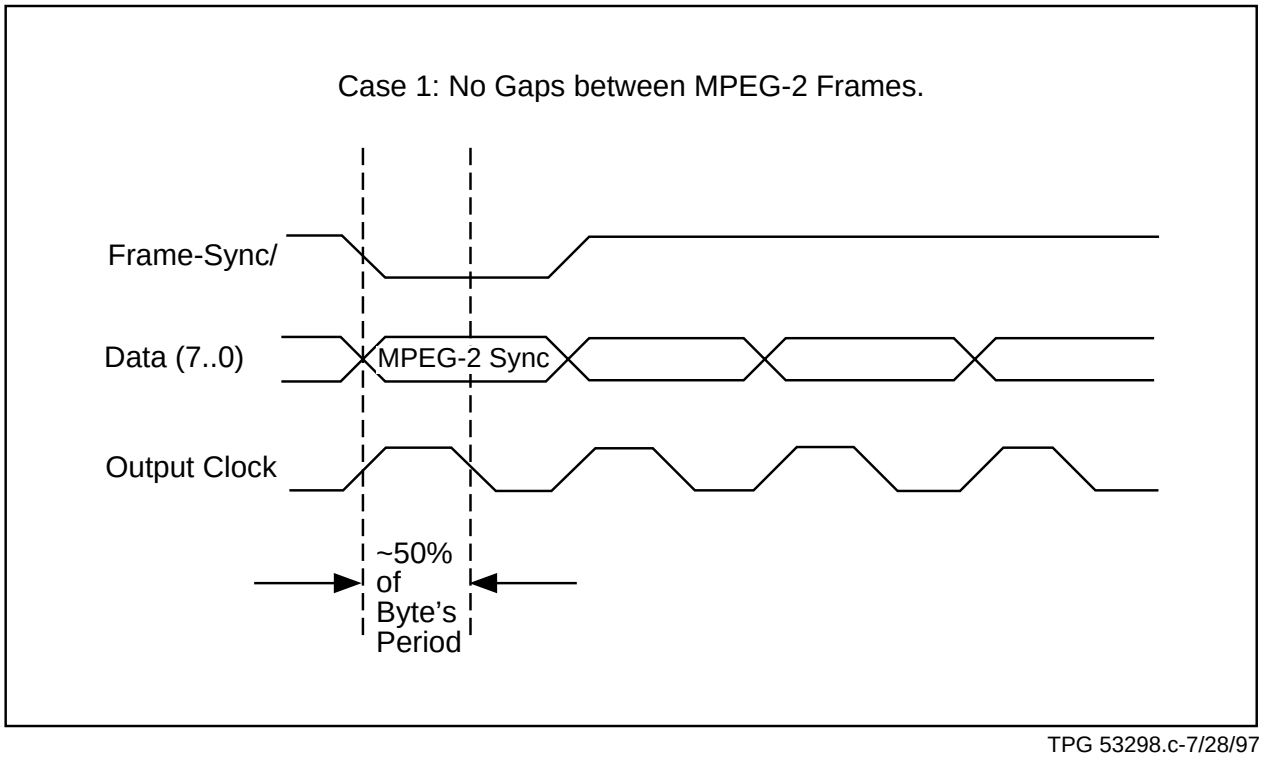


Figure 19.

DOWNSTREAM OUTPUT TIMING (SERIAL OUTPUT)

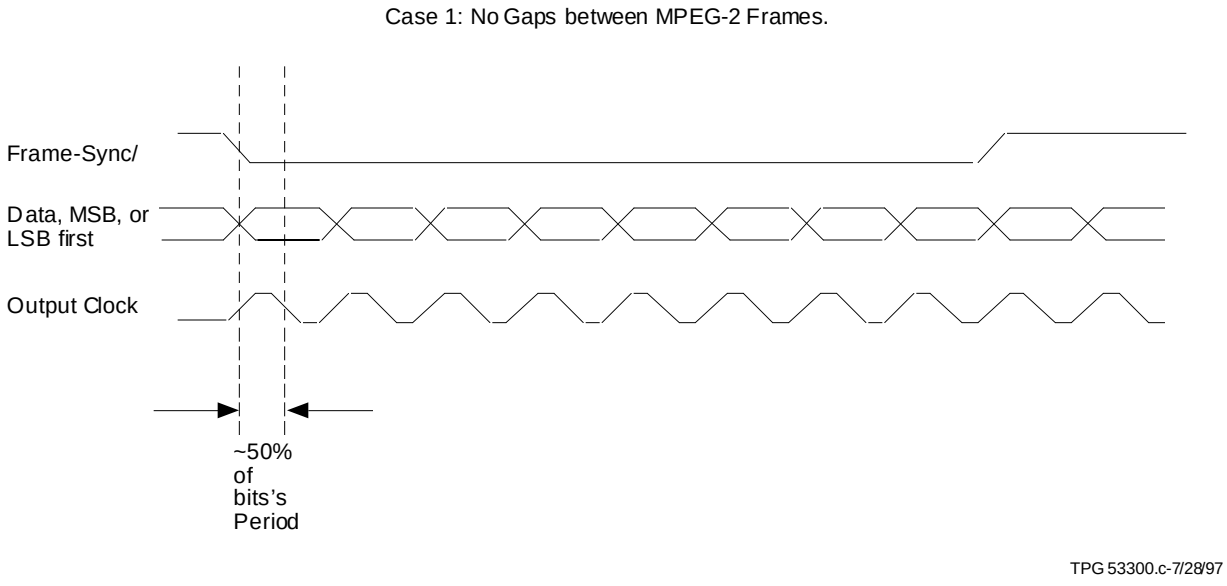
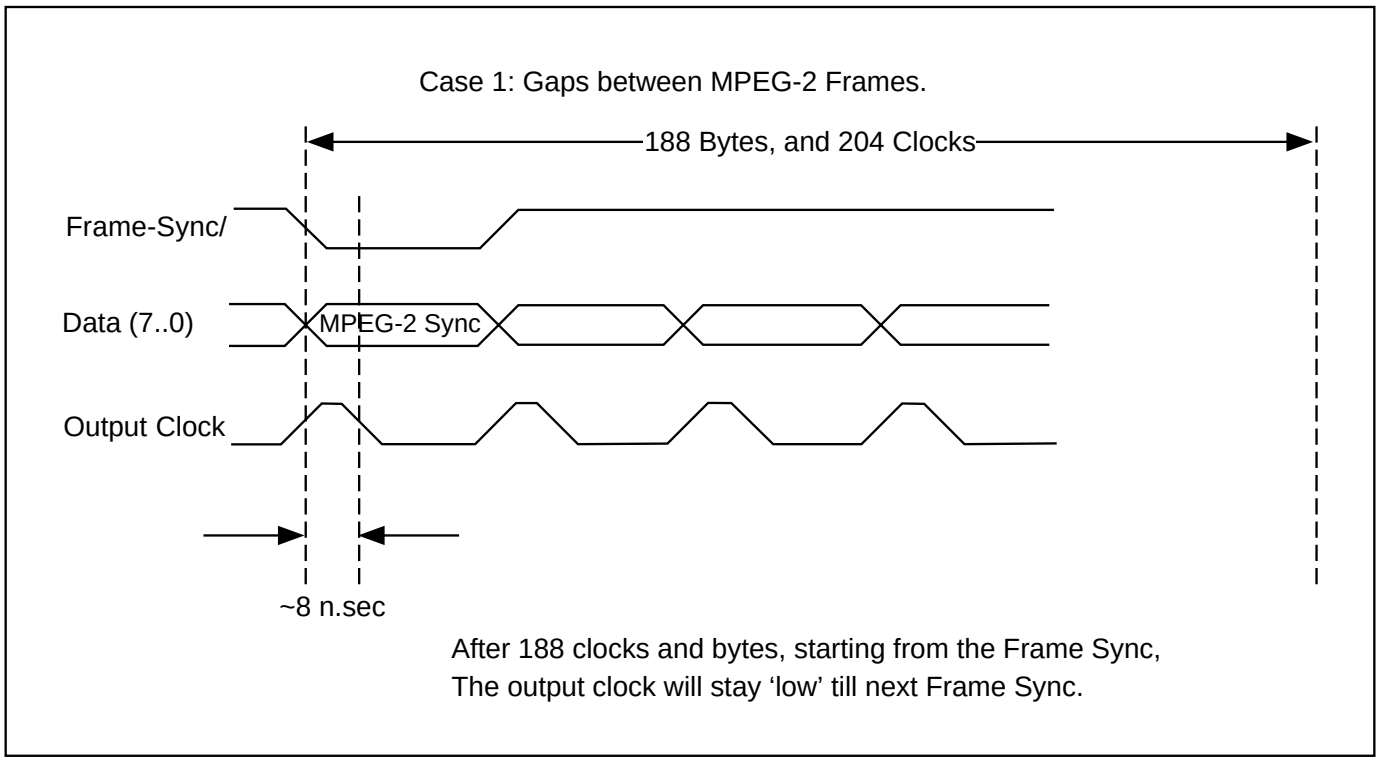


Figure 20.

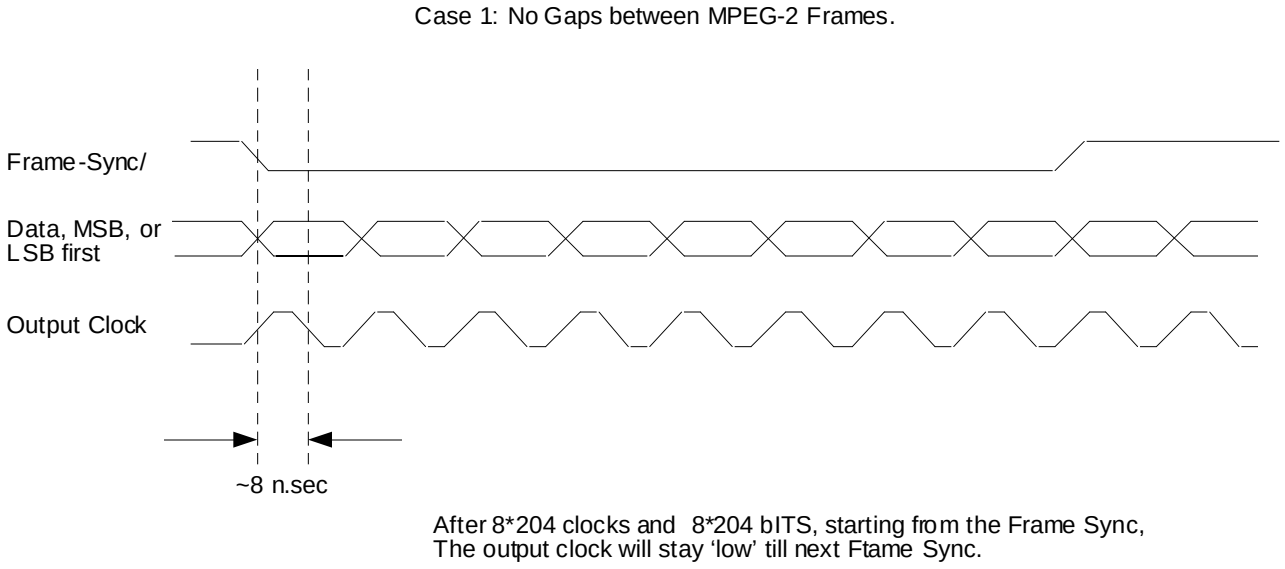
DOWNSTREAM OUTPUT TIMING (PARALLEL DATA OUTPUT)



TPG 53299.c-7/28/97

Figure 21.

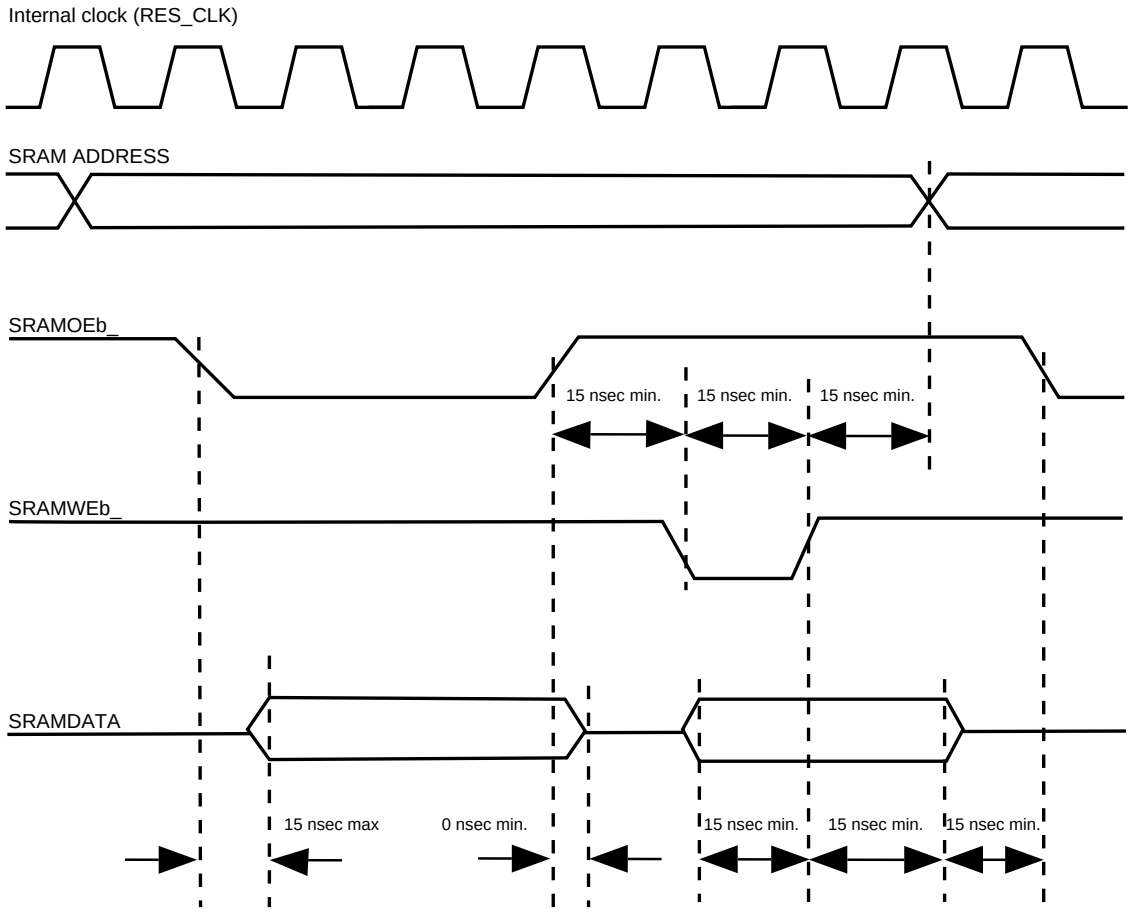
DOWNSTREAM OUTPUT TIMING (SERIAL DATA OUTPUT)



TPG 53297.c-7/28/97

Figure 22.

DE-INTERLEAVER EXTERNAL SRAM TIMING



WCP 53888.C-12/6/97

Figure 23.

TRANSMITTER

INTRODUCTION

The STEL-2176[1] contains a highly integrated, maximally flexible, burst transmitter targeted to the cable modem market. It receives serial data, randomizes the data, performs FEC and differential encoding, maps the data to a constellation before modulation, and outputs an analog RF signal.

The STEL-2176 is the latest in a series of modulator chips that comprise the STEL-1103 through STEL-1109 modulators. Several key components (e.g., a 64-bit FIR and a clock multiplier) have been incorporated in the STEL-2176 and the enhancements have resulted in significant improvements to the chip's performance.

The STEL-2176 is capable of operating at data rates of up to 10 Mbps in BPSK mode, 20 Mbps in QPSK mode, and 40 Mbps in 16QAM mode. It operates at clock frequencies of up to 165 MHz, which allows its internal, 10-bit Digital-to-Analog Converter (DAC) to generate RF carrier frequencies of 5 to 65 MHz.

The STEL-2176 also uses digital FIR filtering to optimally shape the spectrum of the modulating data prior to modulation. This optimizes the spectrum of the modulated signal, and minimizes the analog filtering required after the modulator. The filters are designed to have a symmetrical (mirror image) polynomial transfer function, thereby making the phase response of the filter linear. This also eliminates the inter-symbol interference that results from group delay distortion. In this way, it is possible to change the carrier frequency over a wide frequency range without having to change filters, thus providing the ability to operate a single system in many channels.

The STEL-2176 can operate with very short gaps between transmitted bursts to increase the efficiency of Time Division Multiple Access (TDMA) systems. The STEL-2176 operates properly even when the interburst gap is less than four (4) symbols (half the length of the FIR filter response). In this case the postcursor of the previous burst overlaps and is superimposed on the precursor of the following burst.

Signal level scaling is provided after the FIR filter to allow the STEL-2176's maximum arithmetic dynamic range to be utilized. Signal levels can be changed over a wide range depending on how the device is programmed.

In addition, the STEL-2176 is designed to operate from a 3.3 Vdc power supply and the chip can be interfaced with logic that operates at 5 Vdc.

FUNCTIONAL BLOCK DIAGRAM DESCRIPTIONS

The STEL-2176 is comprised of the Data Path (see page 39) and Control Unit (see page 52) sections shown in Figure 24. The Data Path is comprised of a Bit Sync Block, Bit Encoder Block (i.e., the Scrambler, Reed-Solomon Encoder, and two Multiplexers shown in **Figure 25**), Symbol Mapper Block (i.e., the Bit Mapper, Differential Encoder, and Symbol Mapper are shown in Figure 28), two channels (one for I and one for Q), a Combiner, and a 10-bit DAC. Each channel consists of a Nyquist Filter, Interpolation Filter, and Modulator. The Control Unit is comprised of a Bus Interface Unit (BIU), Clock Generator, and NCO.

Table 32 summarizes the main features of the circuits described by the remaining paragraphs of this section.

DATA PATH DESCRIPTION

Bit SYNC Block

The Bit Sync Block has two functions: latching input data, and synchronizing the STEL-2176 TXBITCLK and symbol counters to the user data.

[1] The STEL-2176 utilizes advanced signal processing techniques which are covered by U.S. Patent Number 5,412,352.

Table 32. Transmit Features

Feature	Characteristic
Carrier frequency:	5 to 65 MHz (maximum of approximately 40% of master clock)
Symbol rate:	From Master clock divided by 16 down to Master clock divided by 16384 (in steps of 4) yielding a maximum symbol rate of 10 Msps with a 160 MHz clock.
FIR filter tap coefficients:	64 programmable taps (10 bits each), symmetric response
Modulation:	BPSK, QPSK, or 16QAM
16QAM constellation:	Eight selectable bit-to-symbol mappings Five selectable symbol-to-constellation mappings
I and Q modulator signs / Spectral Inversion	Signs of I and Q plus the mapping to Sine and Cosine carriers is programmable.
Reed-Solomon Encoder:	Selectable on/off Two selectable generator polynomials Block length shortened any amount Error correction capability T = 1 to 10
Scrambler:	Selectable on/off Self-synchronizing or frame synchronized (sidestream) Location before or after RS Encoder Programmable generator polynomial Programmable length up to 2^{24} - 1 Programmable initial seed
Differential Encoder:	Selectable on/off

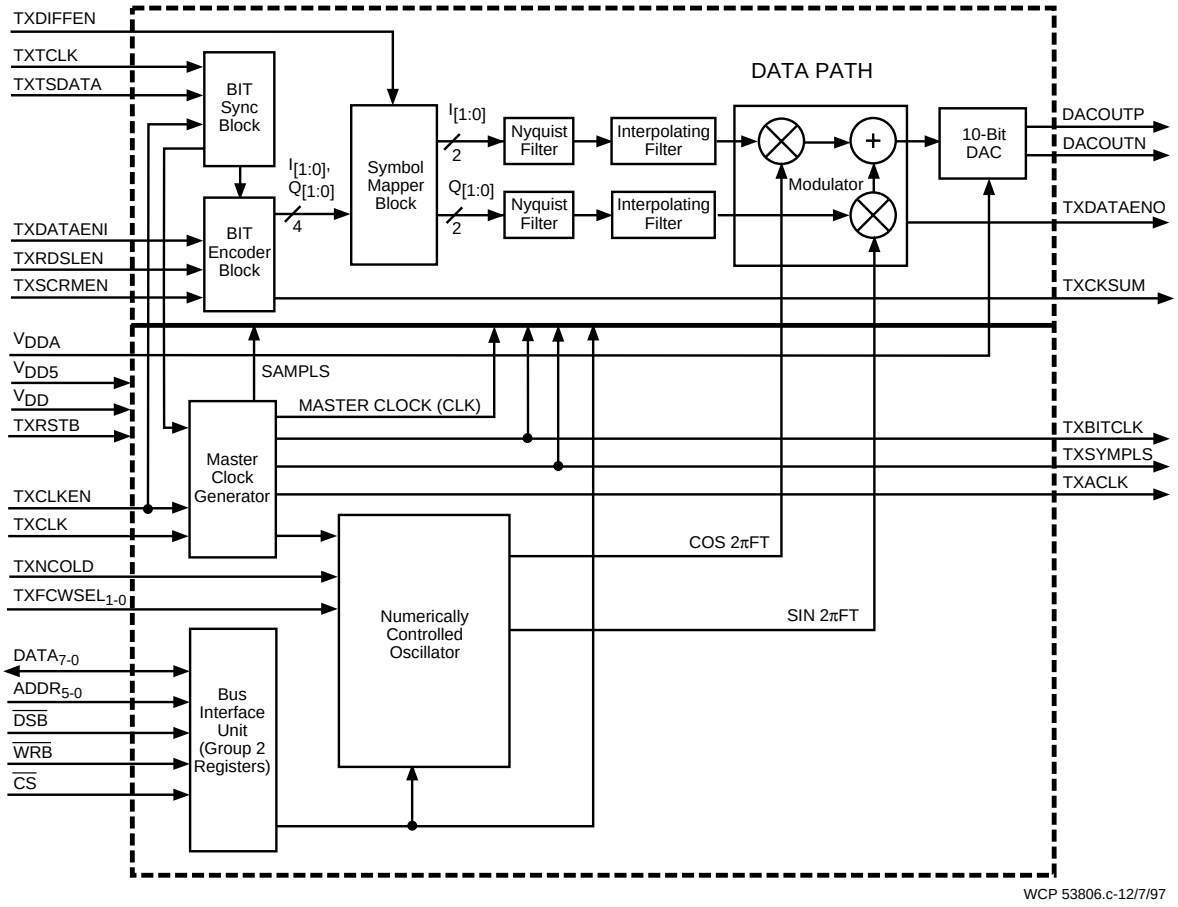


Figure 24. STEL-2176 Transmitter Block Diagram

Table 33. Data Latching Options

Data Source	Latched By	Register 2C Bit 7	Register 2D Bits 1,0	Mode Name
TXTSDATA	TXBITCLK	0	X,0	Master Mode
TXTSDATA	TXTCLK	1	X,0	Slave Mode
PN Code 10, 3	TXBITCLK	0	0,1	Test Mode
PN Code 23, 18	TXBITCLK	0	1,1	Test Mode

Latching Input Data

Latching of input data is accomplished in one of three modes:

- Externally supplied TXTSDATA is latched by the internal TXBITCLK (Master mode).
- Externally supplied TXTSDATA is latched by an externally provided TXTCLK (Slave mode).
- Internally generated PN code data is latched by the internal TXBITCLK (Test mode).

See Table 33 for register settings to implement each mode.

TXBITCLK latches data on its falling edge. TXTCLK latches data on its rising edge.

Whenever the TXCLKEN input is low, the TXBITCLK output will stop. There is also an auxiliary continuous clock (TXACLK) output which is discussed later in the clock generator section. The TXACLK output is primarily for use in master mode where users may need a clock to run control circuits during the time between bursts.

When using slave mode, the data that is latched by the rising edge of TXTCLK is re-latched internally by the next falling edge of TXBITCLK which re-synchronizes the data to the internal master clock.

Synchronizing TXBITCLK / TXSYMPLS

The synchronization circuit aligns the STEL-2176 TXBITCLK and its TXSYMPLS counter circuits to the beginning of the first user data symbol. The circuit has two parts, an arming circuit and a trigger circuit. Once armed, the first rising edge on the TXTCLK input will activate (trigger) the synchronization process.

The circuit can be armed in two ways; taking TXCLKEN from low to high, or toggling Block 2 Register $2E_H$ bit 0 from low to high to low again. In a normal burst mode application, the circuit is automatically re-armed between bursts because TXCLKEN goes low. For applications that will not allow TXCLKEN to cycle low between bursts, some system level precautions should be observed to maintain synchronization of user data to the STEL-2176 TXBITCLK.

Once triggered, the sync circuit re-starts the TXBITCLK and TXSYMPLS counters. The TXBITCLK output starts high, and TXSYMPLS resets to the start of a symbol. There is a delay equal to about three cycles of the master clock from the rising edge of the TXTCLK input before this re-start occurs. During this brief delay period, the TXBITCLK and TXSYMPLS counters are still free running and may or may not have transitions.

In master mode, the rising edge of TXTCLK normally marks the transition of the first user data bit (which will be latched in by the next falling edge of TXBITCLK). In slave mode, the first user data bit must already be valid at this first rising edge of TXTCLK.

Bit Encoder Block

The Bit Encoder Block consists of a Scrambler, a Reed-Solomon Encoder, and data path controls (multiplexers), as shown in **Figure 25**.

Data Path Control (Multiplexers)

The STEL-2176 provides a great deal of flexibility and control over the routing of data through or around the encoding functions. With appropriate register selections, data can be routed around (bypass) both encoders, through either one and around the other, through the scrambler then the RS Encoder, or through the RS Encoder and then the scrambler. Control over the bypassing can be set for software control or external

(user) input signal control. Generally, if an encoding function will be left either on or off continuously, then software control is appropriate. If the function must be turned on and off dynamically (typically in order to send the preamble 'in the clear' i.e. unencoded), then external (user) input control is required. If the Reed-Solomon encoder will not be used at all, then a separate

bypass option can be activated to remove an 8-bit delay register from the data path that is required if the possibility of turning on the encoder exists. Each of the external (user) input control pins (if enabled) turns on the encoding function when high and bypasses the function when low.

The TXDATAENI input signal determines whether or not data will advance (shift through) the encoding blocks. The presence of a high on the TXDATAENI input when the TXBITCLK output goes low allows the circuits to advance data through them. The TXDATAENI signal is delayed internally to allow the rising edge of TXDATAENI to coincide with the first rising edge of TXTCLK.

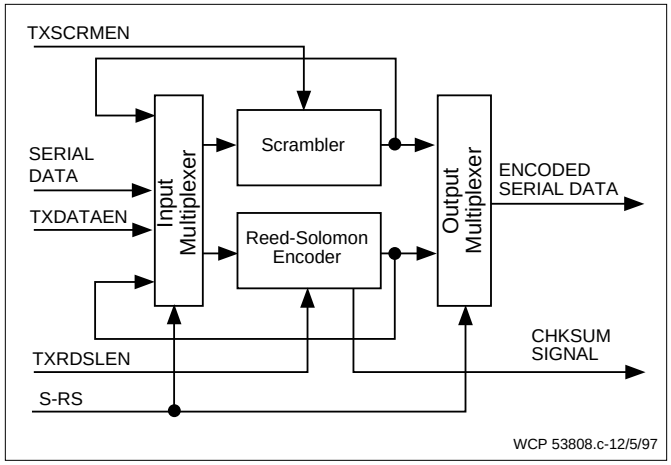


Figure 25. Bit Encoder Functional Diagram

See Table 34 for a summary of register settings required to achieve the various data path possibilities.

Table 34. BIT Encoding Data Path Options

Data Path	Register 36 Bits 6,5	Register 38 Bits 7-2
Data stopped (continuously)	X,X	01 XX XX
Data path on (continuously)	X,X	11 XX XX
Data path enabled by pin 109	X,X	X0 XX XX
Scrambler off (continuously)	X,X	XX XX 01
Scrambler on (continuously)	X,X	XX XX 11
Scrambler enabled by pin 118	X,X	XX XX X0
RS Encode off (continuously)	1,X	XX 01 XX
RS Encode on (continuously)	1,X	XX 11 XX
RS Encode enabled by pin 117	1,X	XX X0 XX
Scrambler then RS Encoder	1,1	XX XX XX
RS Encoder then Scrambler	1,0	XX XX XX
Bypass RS Encoder	0,X	XX XX XX

Scrambler

The scrambler can be used to randomize the serial data in order to avoid a strong spectral component that might otherwise arise from the occurrence of repeating patterns in the input data. The Scrambler (Figure 26) uses a Pseudo-Random (PN) generator to generate a PN code pattern. All 24 registers are presettable and any combination of the registers can be connected (tapped) to form any polynomial of up to 24 bits. The scrambler may be either frame synchronized or self synchronized. Table 35 shows the registers involved.

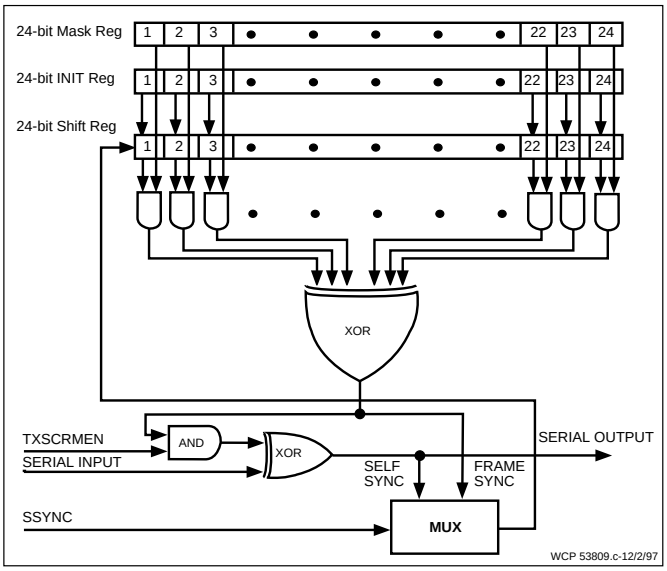


Figure 26. Scrambler Block Diagram

The value in the INIT registers is loaded into the scrambler shift registers whenever the scrambler is at disabled. The scrambler will scramble data one bit a time at each falling edge of TXBITCLK that occurs while both the scrambler and TXDATAENI are active (enabled). Internal delays on the TXSCRMEN control signal input allow for a rising edge to occur coincident with the rising edge of TXBITCLK that precedes the latching of the first data bit to be scrambled.

The Mask, Init, and SSync fields can be programmed for different scrambler configurations. For example, the DAVIC Scrambler configuration shown in Figure 27 can be implemented by programming the Mask, Init, and SSync fields with the values indicated by Table 36.

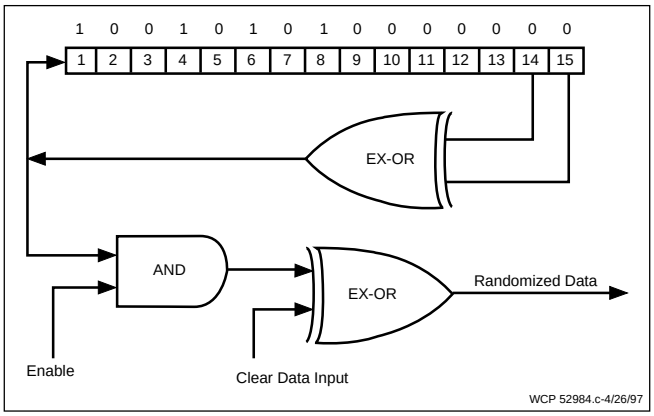


Figure 27. DAVIC Scrambler

Table 35. Scrambler Parameters

Parameter	Characteristic	Block 2 Register Setting		
Generator Polynomial (Mask Reg)	$p(x) = c_{24}x^{24} + c_{23}x^{23} + \ldots + c_1x + 1$ where c_i is a binary value (0, 1)	Register 35 Bit 7 to Bit 0 c_{24} to c_{17}	Register 34 Bit 7 to Bit 0 c_{16} to c_9	Register 33 Bit 7 to Bit 0 c_8 to c_1
Seed (INIT Reg)	Any 24-bit binary value, $s_{24\text{-}1}$	Register 32 Bit 7 to Bit 0 s_{24} to s_{17}	Register 31 Bit 7 to Bit 0 s_{16} to s_9	Register 30 Bit 7 to Bit 0 s_8 to s_1
Scrambler Type	Frame synchronized (sidestream)	Register 36 Bit 4 Set to zero		
Scrambler Type	Self-synchronized	Register 36 Bit 4 Set to one		

Table 36. Sample Scramble Register Values

Parameter	Characteristic	Block 2 Register Setting		
Generator Polynomial (Mask Reg)	$p(x) = x^{15} + x^{14} + 1$	Register 35 Bit 7 to Bit 0 0000 0000	Register 34 Bit 7 to Bit 0 0110 0000	Register 33 Bit 7 to Bit 0 0000 0000
Seed (INIT Reg)	$0000A9_H$	Register 32 Bit 7 to Bit 0 0000 0000	Register 31 Bit 7 to Bit 0 0000 0000	Register 30 Bit 7 to Bit 0 1010 1001
Scrambler Type	Frame synchronized (sidestream)	Register 36 Bit 4 Set to zero		

Reed-Solomon Encoder

The STEL-2176 uses a standard Reed-Solomon (RS) Encoder for error correction encoding of the serial data stream. The error correction encoding uses GF (256) and can be programmed for an error correction capability of 1 to 10, a block length of 3 to 255, and one of two primitive polynomials using the data fields listed in Table 37

When TXDATAENI is high and the RS Encoder is enabled, the serial data stream both passes straight through the RS Encoder and also into encoding circuitry. The encoding circuitry computes a checksum that is 2T bytes long for every K bytes of input data. After the last bit of each block of K bytes of input data, the RS Encoder inserts its checksum (2T bytes of data) into the data path. There is no adverse effect to letting TXTCLK or TXTSDATA continue to run during the checksum; the data input will be ignored. TXCKSUM will be asserted high to indicate that the checksum bytes are being inserted into the data stream and will be lowered at the end of the checksum data insertion. The width of the TXCKSUM pulse is 2T bytes.

The STEL-2176 registers include two bits for determining the bit order for *data into* and *checksum out of* the RS Encoder circuitry. Set these to match the Reed-Solomon decoding circuitry along with the other parameters.

.

Table 37. Reed-Solomon Encoder Parameters

Field Name	Block 2 Register	Description
PP	36_H (bit 7)	1-bit field for selecting Primitive Polynomial: $0 \Rightarrow p(x) = x^8 + x^4 + x^3 + x^2 + 1$ $1 \Rightarrow p(x) = x^8 + x^7 + x^2 + x + 1$
T	36_H (bits 3-0)	4-bit field for setting Error Correction Capability. Programmable over the range of 1 to 10.
K	37_H (bits 7-0)	8-bit field for setting User Data Packet Length (K) in bytes. Programmable over the range of 1 to (255 - 2T). [Net block length, N = K + 2T]
LDLSBF	39_H (bit 4)	Determines whether the first bit of the serial input is to be the MSB (bit 4 = 0) or LSB (bit 4 = 1) of the byte applied to the RS Encoder.
TRLSBF	39_H (bit 5)	Determines whether the MSB (bit 5 = 0) or LSB (bit 5 = 1) of the RS Encoder checksum byte is to be the first bit of the serial output data.

Notes:
GF (256).

Code generator polynomial 1 is used when PP=1: $G(x) = \prod_{i=120}^{119+2T} (x - \alpha^i)\Big|_{\alpha = 02H}$

Code generator polynomial 2 is used when PP=0. $G(x) = \prod_{i=0}^{2T-1} (x - \alpha^i)\Big|_{\alpha = 02H}$

Symbol Mapper Block

The Symbol Mapper Block (Figure 28) maps the serial data bits output by the Bit Encoder Block to symbols, differentially encodes the symbols, and (in 16QAM) maps the symbols to one of five constellations. The Symbol Mapper Block functions are modulation dependent. The modulation mode also defines the number of bits per symbol. The Symbol Mapper Block outputs 2 bits for each symbol to each of the two Nyquist (FIR) Filters.

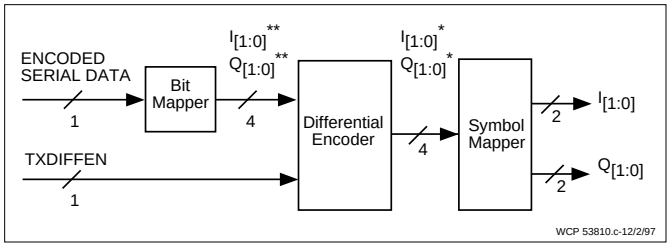


Figure 28. Mapping Block Functional Diagram

Bit Mapper

The Bit Mapper receives serial data and maps the serial data bits to output symbol bits (I_1^{**}, I_0^{**}, Q_1^{**}, and Q_0^{**}). There are four output bits per symbol even in BPSK and QPSK modes. In BPSK, all bits are set equal to each other. In QPSK, each input symbol bit drives a pair of output bits. The four symbol bits are routed to the Differential Encoder in parallel.

For BPSK modulation, each bit (symbol = b_0) of the input serial data stream is mapped directly to I_1^{**}, Q_1^{**}, I_0^{**}, and Q_0^{**} (i.e., $I_1^{**} = I_0^{**} = Q_1^{**} = Q_0^{**} = b_0$). Thus, bit mapping has no affect on the respective value of the symbol's four bits, as shown in Table 38.

For QPSK modulation, each pair of bits (a dibit) forms a symbol (b_0 b_1). The QPSK dibit is mapped so that $I_1^{**} = I_0^{**}$ and $Q_1^{**} = Q_0^{**}$, as shown in Table 38.

For 16QAM, every four bits (a nibble) forms a symbol ($b_0b_1b_2b_3$). The 16QAM nibble is mapped to I_1^{**}, Q_1^{**}, I_0^{**}, and Q_0^{**}, as shown in Table 38.

Table 38. Bit Mapping Options

Mode	Bit-To-Symbol Mapping				Bit Mapping	Mod Mode
	b_0	b_1	b_2	b_3	Register 2D bits 6-4	Register 2C bits 3,2
BPSK	I_1^{**} Q_1^{**} I_0^{**} Q_0^{**}	N/A	N/A	N/A	XXX	1X
QPSK	I_1^{**} I_0^{**}	Q_1^{**} Q_0^{**}	N/A	N/A	XX0	00
QPSK	Q_1^{**} Q_0^{**}	I_1^{**} I_0^{**}	N/A	N/A	XX1	00
16QAM	I_1^{**}	I_0^{**}	Q_1^{**}	Q_0^{**}	000	01
16QAM	Q_1^{**}	Q_0^{**}	I_1^{**}	I_0^{**}	001	01
16QAM	I_0^{**}	I_1^{**}	Q_0^{**}	Q_1^{**}	010	01
16QAM	Q_0^{**}	Q_1^{**}	I_0^{**}	I_1^{**}	011	01
16QAM	I_1^{**}	Q_1^{**}	I_0^{**}	Q_0^{**}	100	01
16QAM	Q_1^{**}	I_1^{**}	Q_0^{**}	I_0^{**}	101	01
16QAM	I_0^{**}	Q_0^{**}	I_1^{**}	Q_1^{**}	110	01
16QAM	Q_0^{**}	I_0^{**}	Q_1^{**}	I_1^{**}	111	01
Note: b_0 is the first serial data bit to arrive at the Bit Mapper						

Differential Encoder

The Differential Encoder encodes the bits (i.e., I_1^{**}, I_0^{**}, Q_1^{**}, and Q_0^{**}) of each symbol received from the Bit Mapper to determine the output bit values (i.e., I_1^{*}, Q_1^{*}, I_0^{*}, and Q_0^{*}), which are routed to the Symbol Mapper.

The differential encoder can be either enabled or bypassed under the control of either a register bit or a user supplied control signal (TXDIFFEN). The selection between user input pin control or register control is made in another register bit, as shown in Table 39.

Table 39. Differential Encoder Control

Level/Value	Register 38 Bits 1,0
Encoding off (continuously)	0,1
Encoding on (continuously)	1,1
Encoding enabled by pin 116 high - enable the Differential Encoder low - disable the Differential Encoder	X,0

For any modulation mode, if differential encoding is disabled then:

$$I_1^* Q_1^* I_0^* Q_0^* = I_1^{**} I_0^{**} Q_1^{**} Q_0^{**}$$

If differential encoding is enabled, then the results are described below for each modulation type.

BPSK

In BPSK mode, the next output bit is found by XORing the input bit with the current output bit. The result is a 180 degree phase change if the output is high and 0 degrees if the output is low.

QPSK

In QPSK mode, the next output dibit is found by XORing the input dibit with the current output dibit. Table 40 shows the results of the differential encoding performed for QPSK modulation and the resulting phase shift. In the table, $I = I_1 = I_0$ and $Q = Q_1 = Q_0$.

16QAM

In 16QAM mode, the differential encoding algorithm is the same as in QPSK. Only the two MSB's, I_1^{**} and Q_1^{**} are encoded. The output bits I_0^* and Q_0^* are set equal to the inputs bits I_0^{**} and Q_0^{**}.

Table 40. QPSK Differential Encoding and Phase Shift

Current Input (IQ)	Current Output (IQ)	Next Output (IQ)	Phase Shift (degrees)
00	00	00	0
	01	01	-90 (CW)
	10	10	90 (CCW)
	11	11	180
01	00	01	-90 (CW)
	01	11	180
	10	00	0
	11	10	90 (CCW)
10	00	10	90 (CCW)
	01	00	0
	10	11	180
	11	01	90 (CCW)
11	00	11	180
	01	10	90 (CCW)
	10	01	-90 (CW)
	11	00	0

Symbol Mapper

The Symbol Mapper receives I_1^*, Q_1^*, I_0^*, Q_0^* of each symbol. Based on the signal modulation and the symbol mapping selection, the Symbol Mapper block maps the symbol to a constellation data point (I_1,Q_1,I_0,Q_0). The Symbol Mapping field (bits 7-5 of Block 2 Register $2E_H$) will map the four input bits to a new value, as indicated in Table 41.

BPSK and QPSK

For BPSK and QPSK, the settings of the symbol to constellation mapping bits is ignored. The constellations for BPSK (Figure 29) and QPSK (Figure 30) are shown below. I_1Q_1 values are indicated by large, bold font (**00** and **11)** and I_0Q_0 values by the smaller font (00 and 11).

16QAM

For 16QAM modulation, the Symbol Mapper maps each input symbol to one of the 16QAM constellations. The specific constellation is programmed by the Symbol Mapping field (bits 7-5 of Block 2 Register $2E_H$) to select the type of symbol mapping. If the MSB of the Symbol Mapping field is set to 0, the mapping will be bypassed and $I_1Q_1I_0Q_0 = I_1^*Q_1^*I_0^*Q_0^*$. The resulting constellation (Figure 31) is the natural constellation for the STEL-2176.

If the MSB of the Symbol Mapping field is set to 1, bits 6-5 can select any of four possible types of symbol mapping (Gray, DAVIC, Left, or Right), as indicated by Table 41.

Table 42 summarizes the symbol mapping and the resulting constellations are shown in Figure 31 and Figure 32. In these figures, I_1Q_1 are indicated by large, bold font (**00, 01, 10,** and **11)** and I_0Q_0 by the smaller font (00, 01, 10, and 11).

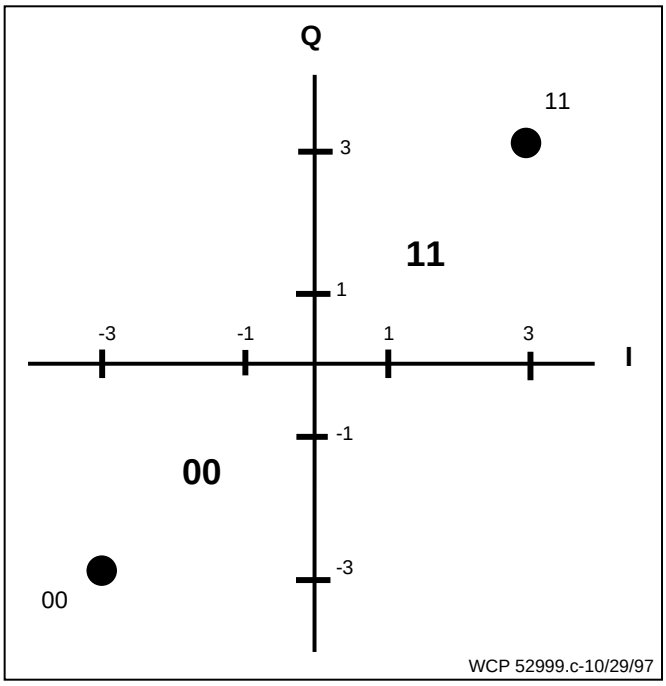


Figure 29. BPSK Constellation

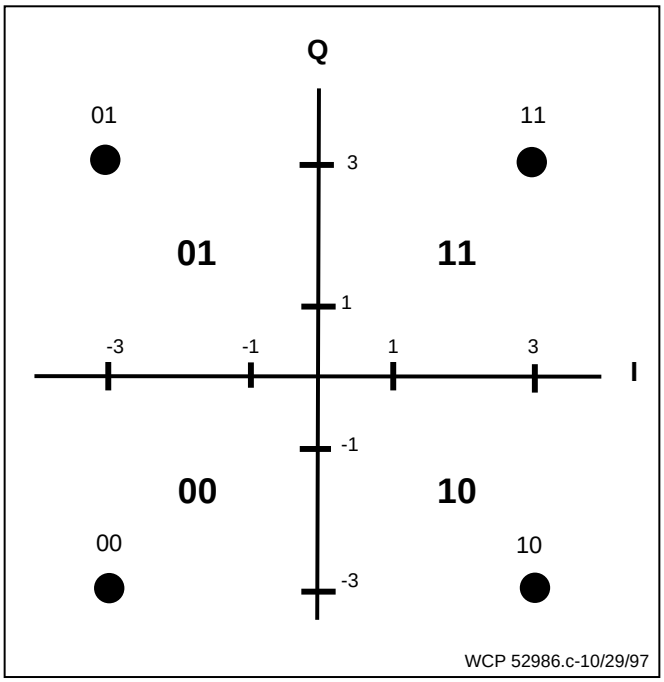


Figure 30. QPSK Constellation

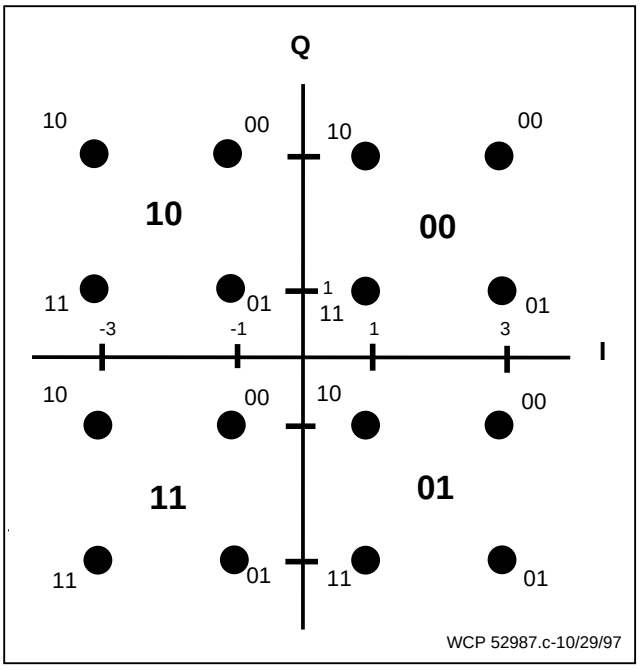


Figure 31. Natural Mapping Constellation

Table 41. Symbol Mapping Selections

Mapping Selection	Register 2E Bits 7-5
Natural	0XX
Gray	100
DAVIC	101
Left	110
Right	111

Table 42. Symbol Mapping

Input Code					Output Code
Natural Mapping (Bypass) $I_1^* Q_1^* I_0^* Q_0^*$	Gray $I_1^* Q_1^* I_0^* Q_0^*$	DAVIC $I_1^* Q_1^* I_0^* Q_0^*$	Left $I_1^* Q_1^* I_0^* Q_0^*$	Right $I_1^* Q_1^* I_0^* Q_0^*$	$I_1 Q_1 I_0 Q_0$
0000	0011	0011	0011	0011	0000
0001	0010	0001	0010	0001	0001
0010	0001	0010	0001	0010	0010
0011	0000	0000	0000	0000	0011
0100	0110	0110	0101	1010	0100
0101	0111	0111	0111	1011	0101
0110	0100	0100	0100	1000	0110
0111	0101	0101	0110	1001	0111
1000	1001	1001	1010	0101	1000
1001	1000	1000	1000	0100	1001
1010	1011	1011	1011	0111	1010
1011	1010	1010	1001	0110	1011
1100	1100	1100	1100	1100	1100
1101	1101	1110	1101	1110	1101
1110	1110	1101	1110	1101	1110
1111	1111	1111	1111	1111	1111

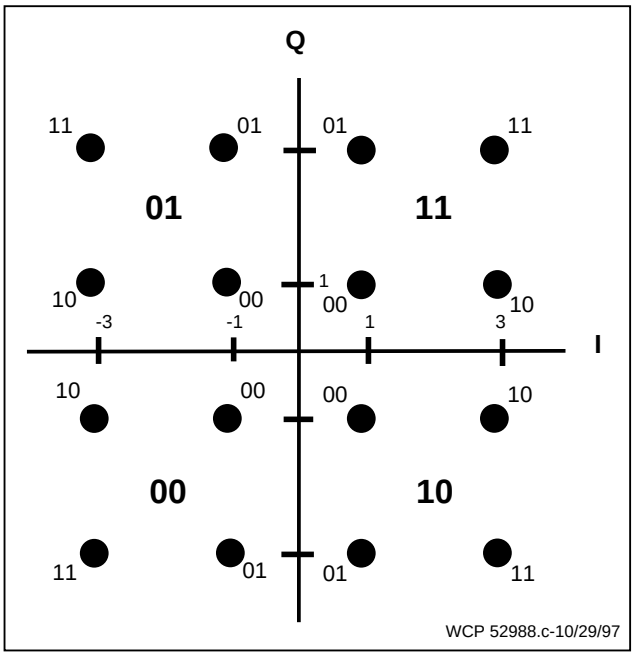


Figure 32. Gray Coded Constellation

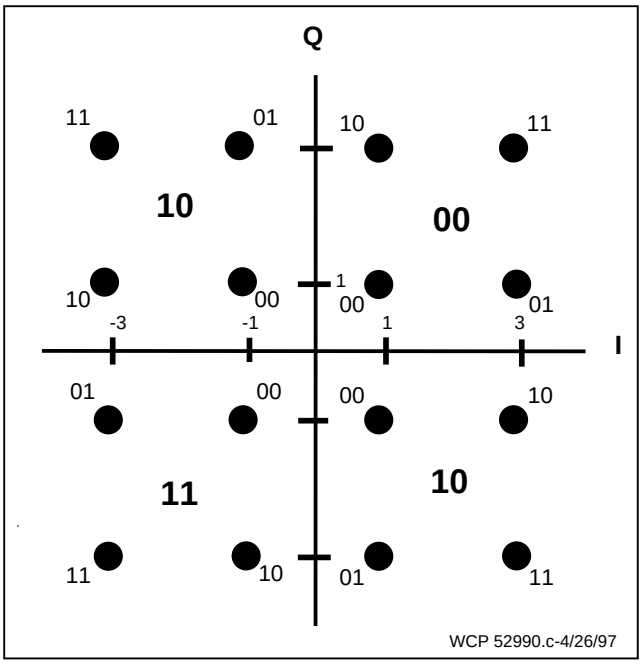


Figure 34. DAVIC Coded Constellation

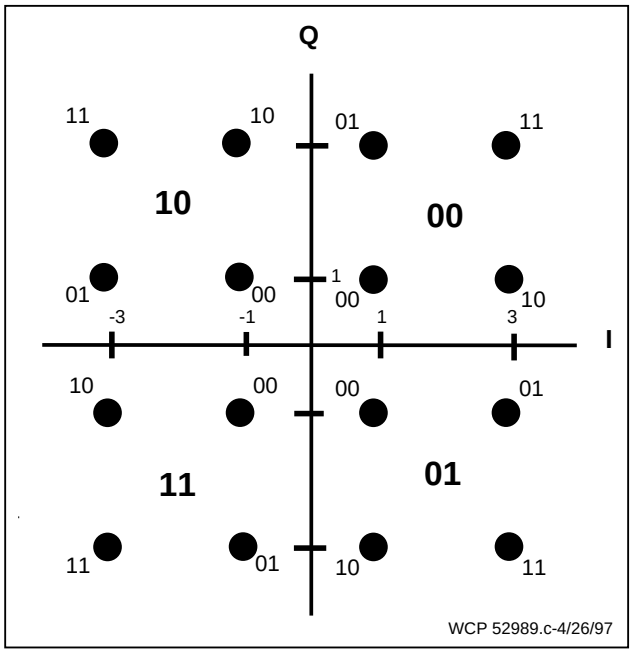


Figure 33. Left Coded Constellation

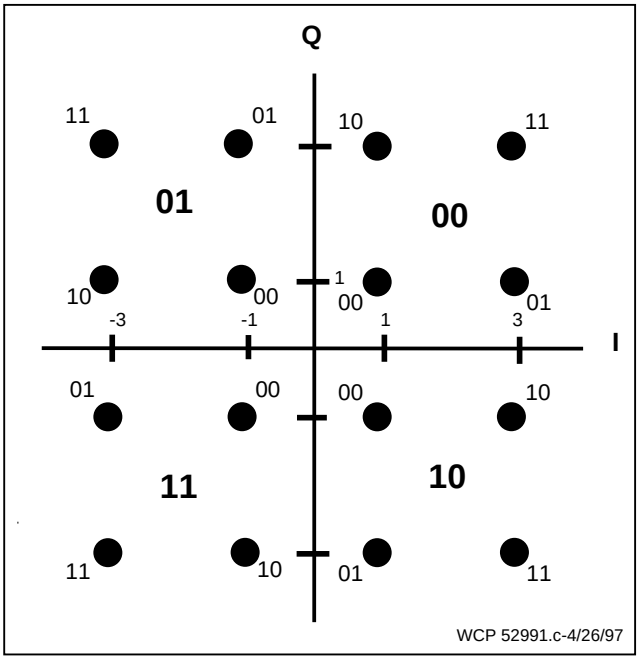


Figure 35. Right Coded Constellation

Nyquist FIR Filter

The finite impulse response (FIR) filters are used to shape each transmitted symbol pulse by filtering the pulse to minimize the sidelobes of its spectrum. The Symbol Mapper Block outputs the I_1I_0 data to a pair of I-channel FIR filters and the Q_1Q_0 data to a pair of Q-channel FIR filters. Figure 36 shows the filter block diagram for a channel pair (I or Q). The FIR filter can be bypassed altogether or, in BPSK or QPSK modes, individual channels can be turned on and off which changes the effective filter gain. Table 43 shows the various FIR configuration options.

Table 43. FIR Filter Configuration Options

Mode	Gain	Register 2E Bits 4-1	Register 2C Bit 1
No FIR Filter	N/A	XXXX	1
16QAM	Unity	1010	0
BPSK/QPSK	Unity	0000	0
BPSK/QPSK	x2	1111	0
BPSK/QPSK	x3	1010	0

Each of the 32-tap, linear phase, FIR filters use 16 ten-bit, coefficients, which are completely programmable for any symmetrical (mirror image) polynomial. The FIR filter coefficients are stored in addresses 09_H - 28_H, using two addresses for each 10-bit coefficient as shown in Table 50. The coefficients are stored as Two's Complement numbers in the range -512 to +511 (200_H to $1FF_H$). The filter is always constrained to have symmetrical coefficients, resulting in a linear phase response. This allows each coefficient to be stored once for two taps, as shown in Table 44.

Interpolating Filter

The Interpolating Filter, shown in Figure 37, is a configurable, three-stage, interpolating filter. The filter increases the STEL-2176's sampling rate (to permit the wide range of RF carrier frequencies possible) by interpolating between the FIR filter steps at the master clock frequency. This smoothes the digital representation of the signal which removes spurious signals from the spectrum

The interpolation filter contains accumulators. As the interpolation ratio grows larger, the number of accumulations per period of time increases. If the interpolation ratio becomes too large, the accumulator

Table 44. FIR Filter Coefficient Storage

MSB (Bits 9-8)	LSB (Bits 7-0)	Filter Taps
$0A_H$	09_H	Taps 16 and 47
$0C_H$	$0B_H$	Taps 17 and 46
$0E_H$	$0D_H$	Taps 18 and 45
10_H	$0F_H$	Taps 19 and 44
…	…	…
…	…	…
26_H	25_H	Taps 30 and 33
28_H	27_H	Taps 31 and 32
$3B_H$	$3A_H$	Taps 0 and 63
$3D_H$	$3C_H$	Taps 1 and 62
…	…	…
…	…	…
56_H	55_H	Taps 13 and 50
58_H	57_H	Taps 14 and 49
$5A_H$	59_H	Taps 15 and 48

Note: For MSB storage, only bits 1-0 are used.

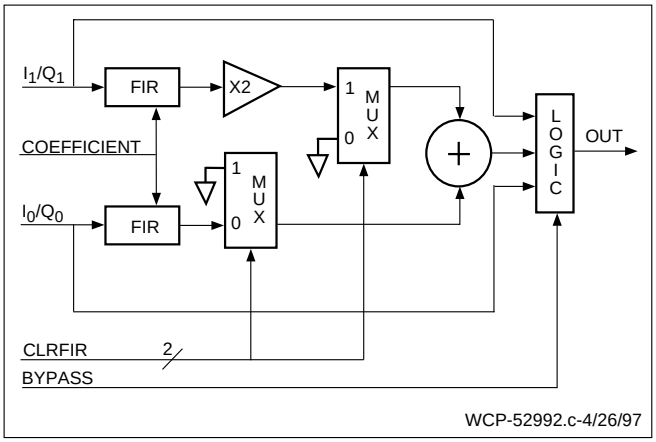


Figure 36. Nyquist FIR Filter

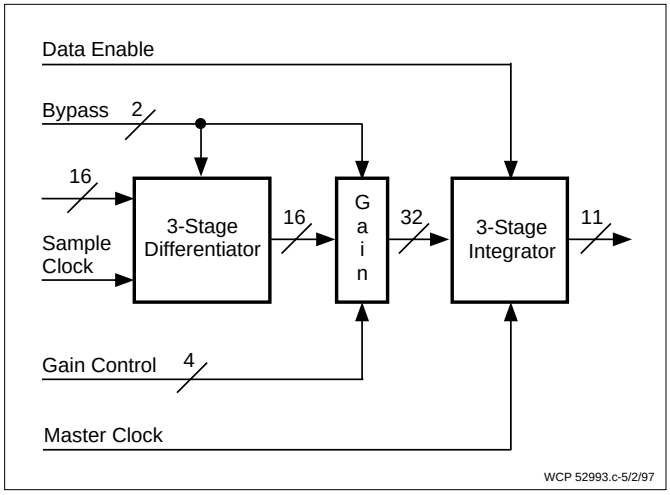


Figure 37. Interpolation Filter Block Diagram

will overflow which will destroy the output spectral characteristics. To compensate for this, the interpolation filter has a gain function. This gain is normally set empirically. If the output spectrum is broad band noise or if it appears correct but has regular momentary "hits" of broad band spectral noise, then the digital gain is too high. The interpolation filter gain is the first place to adjust gain because it does not directly affect the shape of the signal spectrum and it has a very wide adjustment range. Overall, gain can affected in the FIR filter function, the interpolation gain function, and by the number of interpolation stages (and therefore accumulators) used.

Normally, three interpolation stages are used, but there is a bypass option for use when the interpolation is very high. It should be used only as a last resort after all other gain reduction options have been exercised because of the severe impact to spurious performance.

The register bits that affect the interpolation filter functions are shown in Table 45 and Table 46.

Modulator

The interpolated I and Q data signals are input from the Interpolation Filter, fed into two complex modulators, and multiplied by the sine and cosine carriers which are generated by the NCO. The I channel signal is multiplied by the cosine output from the NCO and the Q channel signal is multiplied by the sine output. The resulting modulated sine and cosine carriers are applied to an adder and either added or subtracted together according to the register settings shown in Table 47. This provides control over the characteristics of the resulting RF signal by allowing either or both of the two products to be inverted prior to the addition.

Data Enable Output. The TXDATAENO output is a modified replica of the TXDATAENI input. TXDATAENO is asserted as a high 2 symbols after TXDATAENI goes high and it is asserted as a low 13 symbols after TXDATAENI goes low. In this way, a high on the TXDATAENO line indicates the active period of the DAC during transmission of the data burst. However, if the guard time between the current and next data burst is less than 13 symbols, then the TXDATAENO line will be held high through the next burst.

Table 45. Interpolation Filter Bypass Control

Number of Interpolation Stages Selected	Interpolation Filter Bypass Register 2B Bits 5,4
3	0 0
2	0 1
2	1 0
1	1 1

Table 46. Interpolation Filter Signal Level Control

Gain Factor (Relative)	Filter Gain Control Register 2A Bits 7-4
2^0	0_H
2^1	1_H
2^2	2_H
2^3	3_H
2^4	4_H
2^5	5_H
2^6	6_H
2^7	7_H
2^8	8_H
2^9	9_H
2^{10}	A_H
2^{11}	B_H
2^{12}	C_H
2^{13}	D_H
2^{14}	E_H
2^{15}	F_H

Table 47. Signal Inversion Control

Output of Adder Block	Invert I/Q Channel Register 2B Bits 1,0
Sum = I · cos(ωt) + Q · sin(ωt)	0 0
Sum = –I · cos(ωt) + Q · sin(ωt)	0 1
Sum = I · cos(ωt) – Q · sin(ωt)	1 0
Sum = –I · cos(ωt) – Q · sin(ωt)	1 1

10-Bit DAC

The 10-bit Digital-to-Analog Converter (DAC) receives the modulated digital data and the Master clock. The DAC samples the digital data at the rate of the Master clock and outputs a direct analog RF signal at a frequency of 5 to 65 MHz. The DAC outputs, DACOUTP and DACOUTN, are complementary current sources designed to drive double terminated 50Ω or 75Ω (25Ω or 37.5Ω total) load to ground. The nature of digitally sampled signals creates an image spur at a frequency equal to the Master Clock minus the output RF frequency. This image spur should be filtered by a user supplied low pass filter. For best overall spurious performance, the gain of the STEL-2176 should be the highest possible (before digital overflow occurs - see Interpolation Filter discussion).

CONTROL UNIT DESCRIPTION

Bus Interface Unit

The Bus Interface Unit (BIU) is part of the Microcontroller Interface (see page 11). If contains the Block 2 Registers (90 programmable 8-bit registers). The Reset ($\overline{\text{TXRSTB}}$) input signal is the master reset for the STEL-2176. Asserting a low on $\overline{\text{TXRSTB}}$ will reset the contents of all Block 2 Registers to 00_H (as well as clearing the data path registers). Asserting a high on $\overline{\text{TXRSTB}}$ enables normal operation. After power is applied and prior to configuring the STEL-2176, a low should be asserted on $\overline{\text{TXRSTB}}$. Since $\overline{\text{TXRSTB}}$ is asynchronous, the TXCLKEN input should be held low whenever $\overline{\text{TXRSTB}}$ is low.

The parallel address bus ($ADDR_{5-0}$) is used to select one of the 90 Block 2 Registers by placing its address on the $ADDR_{5-0}$ bus lines. The data bus ($DATA_{7-0}$) is an 8-bit, bi-directional data bus for writing data into or reading data from the selected Block 2 Register.

The access operation is performed using the control signals $\overline{\text{DSB}}$, $\overline{\text{CS}}$, and $\overline{\text{WRB}}$. The Chip Select ($\overline{\text{CS}}$) input signal is used to enable or disable access operations to the STEL-2176. When a high is asserted on $\overline{\text{CS}}$, all access operations are disabled and a low is asserted to enable the access operations. The $\overline{\text{CS}}$ input only affects Block 2 Register access and has no effect on the data path.

The Data Strobe ($\overline{\text{DSB}}$) input signal is used to write the data that is on the data bus ($DATA_{7-0}$) into the Block 2 Register selected by $ADDR_{5-0}$. The Write/Read ($\overline{\text{WRB}}$) input signal is used to control the direction of the Block 2 Register access operation. When $\overline{\text{WRB}}$ is high, the data in the selected Block 2 Register is output onto the $DATA_{7-0}$ bus. When $\overline{\text{WRB}}$ is low, the rising edge of $\overline{\text{DSB}}$ is used to latch the data on the $DATA_{7-0}$ bus into the selected Block 2 Register. (Refer to the Write and Read Timing diagrams in the Timing Diagrams section.)

Some of the Block 2 Register data fields are used for factory test and must be set to specific values for normal operation. These values are noted in Table 50.

Master Transmit Clock Generator

The STEL-2176 uses a master clock (CLK) to control the transmit timing functions. CLK can be generated in either of three ways as shown in Figure 38.

A transmit bypass clock can be applied to the TXBYPCLK input and selected to drive CLK.

An external clock can be applied to the TXOSCIN input or a crystal can be connected across the TXOSCIN and TXOSCOUT inputs. The oscillator circuit outputs a 20-50 MHz signal to a frequency multiplier PLL, which upconverts the signal to a 100-150 MHz clock. When the bypass clock is not used, the multiplexer is set to select the output of the frequency multiplier to drive the CLK signal. The frequency multiplier output can also be routed to the TXPLLCLK output for test purposes.

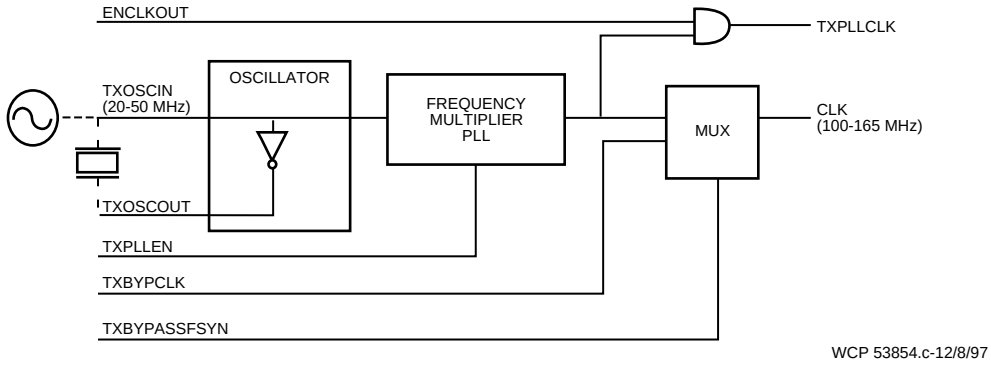


Figure 38. Master Clock Generation

Clock Generator

The timing of the STEL-2176 is controlled by the Clock Generator, which uses an master clock (CLK) and programmable dividers to generate all of the internal and output clocks. There are primarily two clock systems, the auxiliary clock and the data path timing signals (bit, symbol, and sampling rate signals).

The auxiliary clock (TXACLK) output is primarily for use in master mode where users may need a clock to run control circuits during the guard time between bursts (when TXCLKEN is low and TXBITCLK has stopped). The output clock rate is set by the frequency (f_{CLK}) of the external master clock and the value (N) of the Auxiliary Clock Rate Control field (bits 3-0 of Block 2 Register $2A_H$). The clock rate is set to:

$$\text{TXACLK} = \left. \frac{f_{CLK}}{N+1} \right| \; 2 \le N \le 15$$

If N is set to 1 or 0, the TXACLK output will remain set high, thereby disabling this function. If the TXACLK signal is not required, it is recommended that it be set in this mode to conserve power consumption. The TXACLK output is a pulse that will be high for 2 cycles of CLK and low for (N-1) CLK cycles. Unlike other functions, the TXACLK output is not affected by TXCLKEN.

The data path timing is based on the ratio of the master clock frequency to the symbol data rate. The ratio must be a value of four times an integer number (N+1). The value of N must be in the range of 3 to 4095. This value is represented by a 12-bit binary number that is programmed by LSB and MSB Sampling Rate Control fields [Block 2 Register 29_H (LSB) and bits 3-0 of Block 2 Register 39_H (MSB)], which sets the TXSYMPLS frequency [based on the frequency (f_{CLK}) of the external master clock] to:

$$\text{Symbol Rate} = \left. \frac{1}{4} * \frac{f_{CLK}}{N+1} \right| \; 3 \le N \le 4095$$

The symbol pulse (TXSYMPLS) signal output is intended to allow the user to verify synchronization of the external serial data (TXTSDATA) with the STEL-2176 symbol timing. TXSYMPLS is normally low and pulses high for a period of one CLK cycle at the point where the last bit of the current symbol is internally latched by the falling edge of the internal BIT Clock (TXBITCLK) signal. (Refer to the Timing Diagrams section.)

The internal TXBITCLK period is a function of the MOD field (bits 3-2 of Block 2 Register $2C_H$), which determines the signal modulation. TXBITCLK has a 50% duty cycle for BPSK and QPSK modes. It also has a 50% duty cycle in 16QAM mode when N+1 is even. If N+1 is odd, then TXBITCLK will be high for (N÷2)+1 clocks and then low for N÷2 clocks. (Refer to the Bit Clock Synchronization Timing diagram in the Timing Diagrams section.)

The **TXBITCLK** frequency is determined by :

$$\text{BITCLK} = \left. \frac{\text{CLK}}{(N+1) * K} \right| \begin{array}{l} K = 1 \text{ for 16QAM,} \\ \quad\; 2 \text{ for QPSK,} \\ \quad\; 4 \text{ for BPSK} \\ 3 \le N \le 4095 \end{array}$$

NCO

A 24-bit, Numerically Controlled Oscillator (NCO) is used to synthesize a digital carrier for output to the Modulator. The NCO gives a frequency resolution of about 6 Hz at a clock frequency of 100 MHz. The NCO also uses 12-bit sine and cosine lookup tables (LUTs) to synthesize a carrier with very high spectral purity, typically better than -75 dBc at the digital outputs.

The STEL-2176 provides register space for three different carrier frequencies. The carrier frequency that will drive the modulator is selected by the $TXFCWSEL_{1-0}$ control pin input signals. A high on the TXNCOLD input pin causes the registers selected by TXFCWSEL to drive the NCO at the frequency determined by the register value.

The NCO's frequency is programmable using the NCO field (Block 2 Registers 08_H -00_H). The nine 8-bit registers at addresses 00_H through 08_H are used to store the three 24-bit frequency control words FCW 'A', FCW 'B' and FCW 'C' as shown in Table 48.

The output carrier frequency of the NCO (f_{CARR}) will be:

$$f_{CARR} = \frac{f_{CLK} \cdot FCW}{2^{24}}$$

where, f_{CLK} is the frequency of the CLK input signal.

The FZSINB field (bit 7 Block 2 Register $2D_H$) controls the sine component output of the NCO. This can be used in BPSK to rotate the constellation 45 degrees (to 'on axis' modulation). For normal operation, it should be set to one.

Table 48. FCW Selection

$TXFCWSEL_{1-0}$	FCW Selected	FCW Value Bits		
		23 - 16	15 - 8	7 - 0
00	FCW A	Register 02_H Bits 7 - 0	Register 01_H Bits 7 - 0	Register 00_H Bits 7 - 0
01	FCW B	Register 05_H Bits 7 - 0	Register 04_H Bits 7 - 0	Register 03_H Bits 7 - 0
10	FCW C	Register 08_H Bits 7 - 0	Register 07_H Bits 7 - 0	Register 06_H Bits 7 - 0
11	Zero Frequency			

TRANSMIT REGISTER DESCRIPTIONS

Programming the 2176 Transmit and Receive Functions

The STEL-2176 has a total of xxx registers and they are arranged as three banks of registers. As indicated in Table 49, Bank 0 is sub-divided into two groups of registers which yields a total of four register groups. Table 49 shows the Bank Address that must be written to location FF_H in order to access the respective register group. The registers comprising The Bank 0 and Bank 1 registers are described in the Receiver Section (see page 20). The registers comprising Bank 2 are described below. When the Bank 2 (Group 4) registers are accessed, the hexadecimal register addresses listed in Table 50 are sent to the Microcontroller Interface (see page 11) for doing a read or write operation on a specific register.

Table 49. Addresses of the STEL-2176 Register Groups

Group	Bank	Group Name	Bank Address (location FF_H)
1	0	Universal Registers	00_H
2	0	QAM Demodulator Registers Universal Registers	00_H
3	1	Downstream FEC Registers	01_H
4	2	Upstream, or transmitter, Registers	02_H

Block 2, Upstream Registers (Group 4)

Description

Each of the Block 2 registers (see Table 50) is an 8-bit, Read/Write register and each register contains one or more data fields, described below. The data fields are the transmit parameters which control the transmit characteristics of the STEL-2176. When a transmit parameter requires more than 8 bits, it is stored in multiple data fields and stored used two or more registers.

Table 50. Transmit Block 2 Register Data Fields

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08-00	NCO Frequency Control Word							
28-09	FIR Filter Coefficients							
29	Sampling Rate Control							
2A	CIC Filter Gain Control				Auxiliary Clock Rate Control			
2B	DCINB	ICIN	Int. Filt. Bypass		MSB	ACCIN	Invert I/Q Chan.	
2C	TCLK Sel.		ENDAC	FWDB	GAINB		PN Sel	PN Mod
2D	FZSIN	NITV	LSB	REV	GAINB		PN Sel	PN Mod
2E	MAPBPB	MAPSEL		CLRFIR				Sync
2F								TEST
30	SCRAMBLER Init Reg [7:0]							
31	SCRAMBLER Init Reg [15:8]							
32	SCRAMBLER Init Reg[23:16]							
33	SCRAMBLER Mask Reg [7:0]							
34	SCRAMBLER Mask Reg[15:8]							
35	SCRAMBLER Mask Reg[23:16]							
36	PP	BPB	S-RS	ssync	T			
37	K							
38	DATA-ENBP	DATA-ENSEL	RSENBP	RSENS-EL	SCRME-NBP	SCRM-ENSEL	DiffDC-BP	DiffDCS-EL
39			TRLSBP	LDLSBF	MSB Sampling rate			
3A-59	FIR Filter Coefficients							

Transmit Parameter Descriptions

Auxiliary Clock Rate Divider — Sets the divide-by ratio of f_{CLK} for generating an output clock for use with external control circuits.

Bit Mapping — Selects the Bit-to-Symbol mapping option when QPSK or 16QAM modulation is selected.

Bit Sync Re-arm — Used to arm the TXBITCLK synchronization circuit when TXCLKEN cannot be applied low between bursts.

BypassB — Allows the Scrambler and Reed-Solomon Encoder to be bypassed.

CLRFIR — Controls the Gain of the FIR Filter.

DATAENBPB — Continuously enables or disables the input multiplexer of the Bit Encoder Block.

DATAENSEL — Selects software (DATAENBPB) or hardware (input pin 109) control for enabling the input multiplexer of the Bit Encoder Block.

DiffDCBPB — Allows the Differential Encoder to be bypassed.

DiffDCSEL — Selects software (DiffDCBPB) or hardware (input pin 116) control for enabling the Differential Encoder.

ENDAC — Setting this bit to 0 will make the DAC output enable controlled by the TXDATAENO signal (see page 65). Setting it to 1 will make the DAC enabled all the time. The default is 0.

FIR bypass — Controls routing of I/Q data through or around the FIR filters.

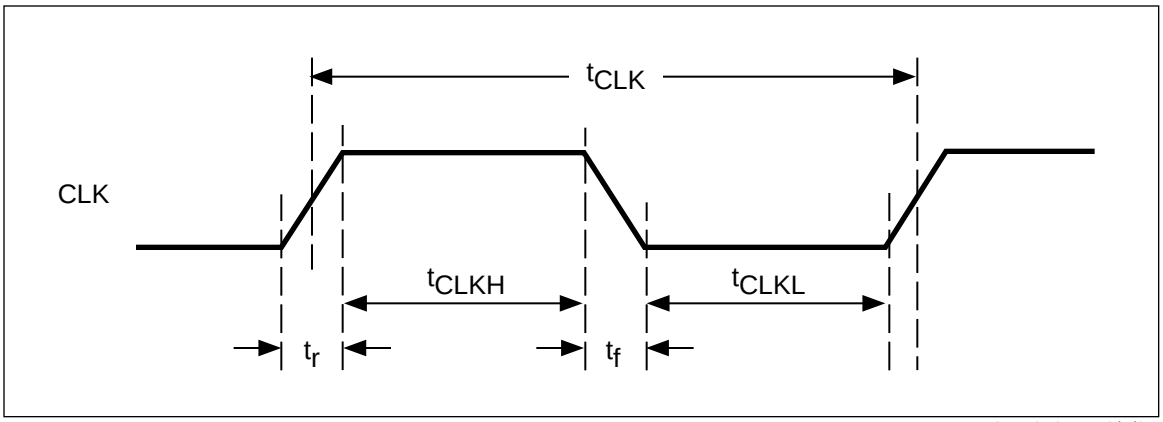
FIR Filter Coefficients — Sixteen 10-bit FIR coefficients. Each coefficient is applied to two taps of the FIR filter to control its filter characteristics.

FZSINB — Controls the sine component of the NCO output. Setting the field to 0 rotates the constellation by 45° for on-axis modulation of a BPSK signal.

Interpolation Filt. Bypass	Controls the number of filter stages the Interpolation Filter will use for filtering the signal.
Interpolation Filter Gain Control	Sets the gain of the Interpolation Filter.
Invert I/Q Chan.	Controls the signal inversion of the I and Q channels by using an adder to add or subtract the two channels.
K	Defines the length of the User Data Packet in bytes.
LDLSBF	Determines whether the MSB or LSB of the checksum byte is to be output as the first bit of the serial output data.
LSB Sampling Rate Control	A 12-bit word that controls the sampling rate of the 10-Bit DAC. Register 29 contains the 8 LSBs and Register 39 contains the 4 MSBs.
MOD	Selects type of modulation (BPSK, QPSK, or 16QAM).
NCO	Three 24-bit frequency control words. The word selected for setting the frequency of the NCO carrier is selected by the input pins TXFCWSEL[1-0] .
PN Code Sel	Selects one of two PN codes when pseudo-random generator is enabled.
PN On/Off	Enables or disables the pseudo-random generator
PPolynomial	Selects one of two primitive polynomials for use with the Reed-Solomon Encoder for encoding data.
RSENBPB	Allows the Reed-Solomon Encoder to be bypassed.
RSENSEL	Selects software (RSENBPB) or hardware (input pin 117) control for enabling the Reed-Solomon Encoder.
SCRAMBLER Init Registers	A 24-bit word that is loaded into the PN generator to initialize its shift register.
SCRAMBLER Mask Registers	A 24-bit word that is masks the output of the PN generator shift register.
SCRMENBPB	Allows the Scrambler to be bypassed.
SCRMENSEL	Selects software (SCRMENBPB) or hardware (input pin 118) control for enabling the Scrambler.
Self-Sync	Controls selection of the self sync or frame sync signal for routing back to the PN generator shift circuit.
S-RS	Controls whether the input data is to be scrambled then encoded by the Scrambler and Reed-Solomon Encoder or whether it is to be encoded then scrambled.
Symbol Mapping	Selects one of five symbol mapping options when 16QAM modulation is selected.
T	Sets the error correction capability of the error correction encoding.
TCLK Sel.	Selects an externally generated clock for external control of data latching.
TRLSBF	Determines whether the first input bit is the MSB or LSB of the byte applied to the RS Encoder.

TIMING DIAGRAMS

CLOCK TIMING



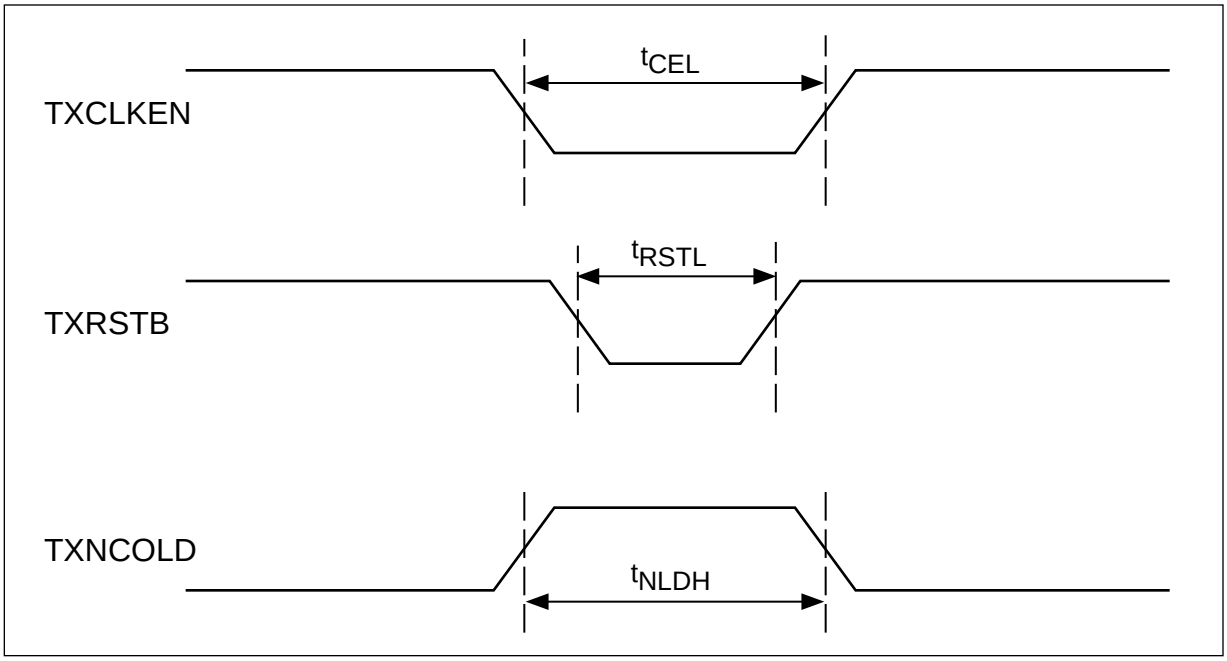
WCP 52787.c-12/5/97

Table 51. Clock Timing AC Characteristics

(V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, T_a = –40° to 85° C)

Symbol	Parameter	Min.	Nom.	Max.	Units	Conditions
	Clock Frequency ($\frac{1}{t_{CLK}}$)			165	MHz	
t_{CLK}	Clock Period	6			nsec	
t_{CLKH}	Clock High Period	2.5			nsec	
t_{CLKL}	Clock Low Period	2.5			nsec	
t_R	Clock Rising Time			0.5	nsec	
t_F	Clock Falling Time			0.5	nsec	

TRANSMIT PULSE WIDTH



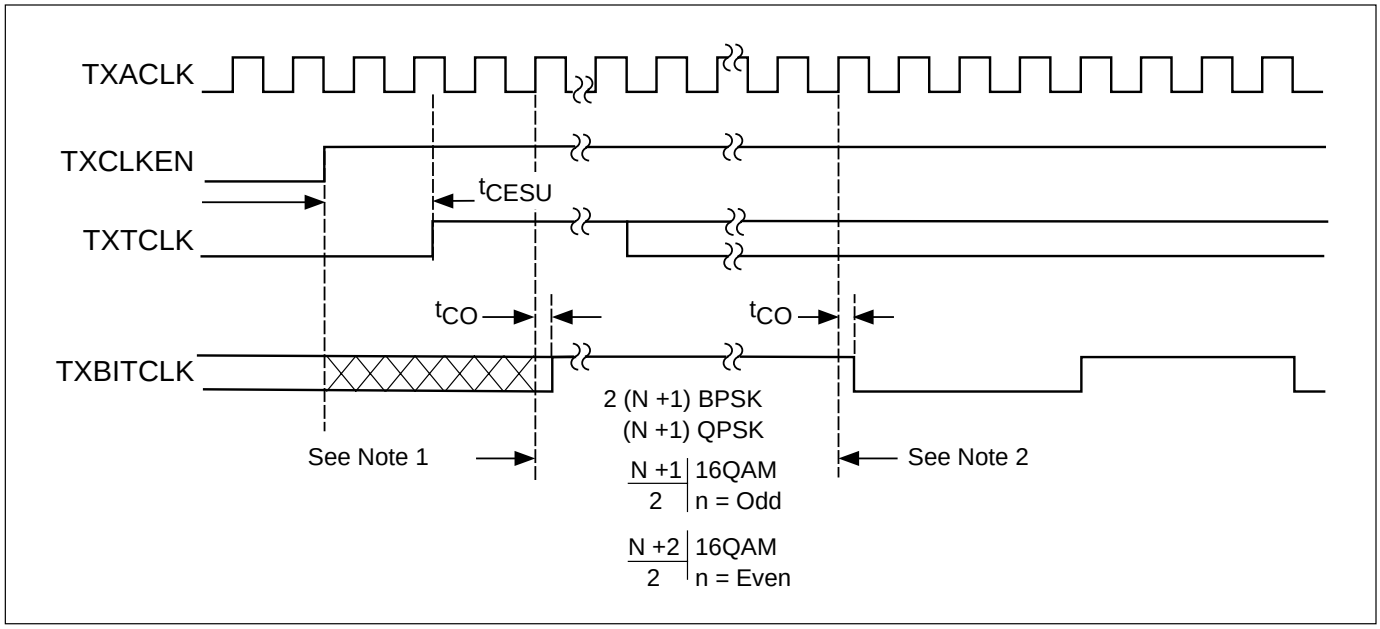
WCP 53811.c-12/5/97

Table 52. Pulse Width AC Characteristics

(V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, T_a = –40° to 85° C)

Symbol	Parameter	Min.	Nom.	Max.	Units	Conditions
t_{CEL}	Clock Enable (TXCLKEN) Low	4			nsec	
t_{RSTL}	Reset (TXRSTB) Low	5			nsec	
t_{NLDH}	NCO Load (TXNCOLD) High	1			CLK cycles	

BIT CLOCK SYNCHRONIZATION



WCP 53826.c-12/5/97

Note 1: TXBITCLK will be forced high on the second rising edge of CLK following the rising edge of TXTCLK.

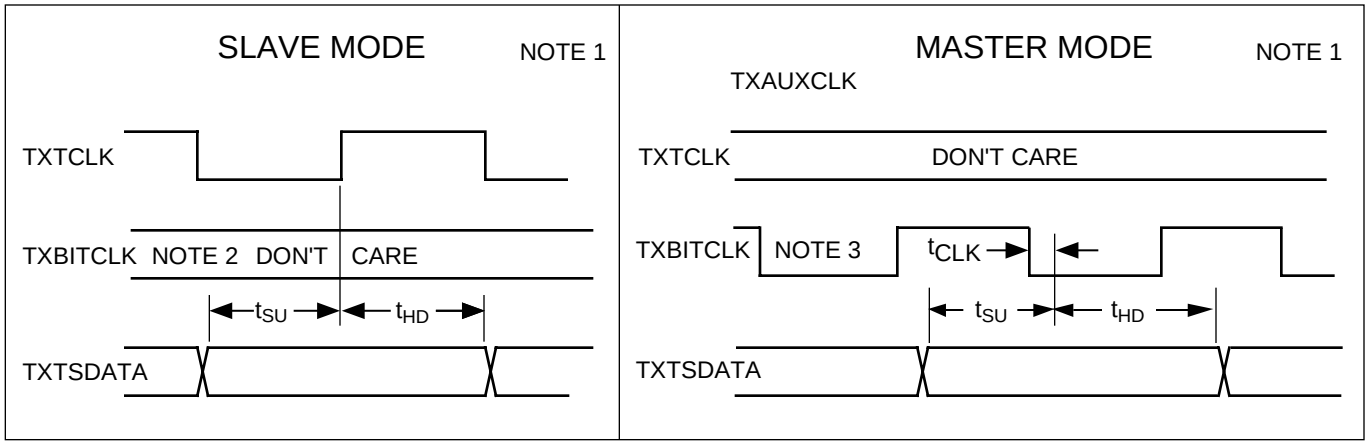
Note 2: The period of time that TXBITCLK is high is measured in cycles of CLK (e.g. (N + 1) in QPSK). "N" is a 12-bit binary number formed by taking bits 3-0 of Block 2 Register 39_H as the MSB's and taking bits 7-0 of Block 2 Register 29_H as the LSB's. The TXBITCLK low period is the same except for 16QAM when "N" is even in which case the low period is (N/2) yielding the correct TXBITCLK period but not a perfect squarewave.

Table 53. Bit Clock Synchronization AC Characteristics

(V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, T_a = –40° to 85° C)

Symbol	Parameter	Min.	Nom.	Max.	Units	Conditions
t_{CO}	Clock to TXBITCLK, TXSYMPLS, TXDATAENO, or TXACLK edge			2	nsec	
t_{CESU}	Clock Enable (TXCLKEN to TXTCLK Setup)	3			nsec	

TRANSMIT INPUT DATA AND CLOCK TIMING



Note 1: Mode is determined by setting of BIT 7 in Block 2 Register $2C_H$. Bit 7 high is slave mode; Bit 7 low is master mode.

Note 2: In slave mode, even though TXBITCLK is shown as "Don't Care", it should be noted that internally the STEL 2176 will relatch the data on the next falling edge of TXBITCLK. Thus, avoid changing the control signal inputs (TXDATAENI, TXDIFFEN, TXRDSLEN, TXSCRMEN) at the falling edges of TXBITCLK.

Note 3: In the STEL-2176, data is latched on the rising edge of the CLK that follows the falling edge of TXBITCLK. Thus, the data validity window is one CLK period (t_{CLK}) delayed. CLK not shown.

Table 54. Input Data and Clock AC Characteristics

(V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, T_a = –40° to 85° C)

Symbol	Parameter	Min.	Nom.	Max.	Units	Conditions
t_{CLK}	Clock Period	6			nsec	
t_{SU}	TXTSDATA to Clock Setup	2			nsec	
t_{HD}	TXTSDATA to Clock Hold	2			nsec	

WRITE TIMING

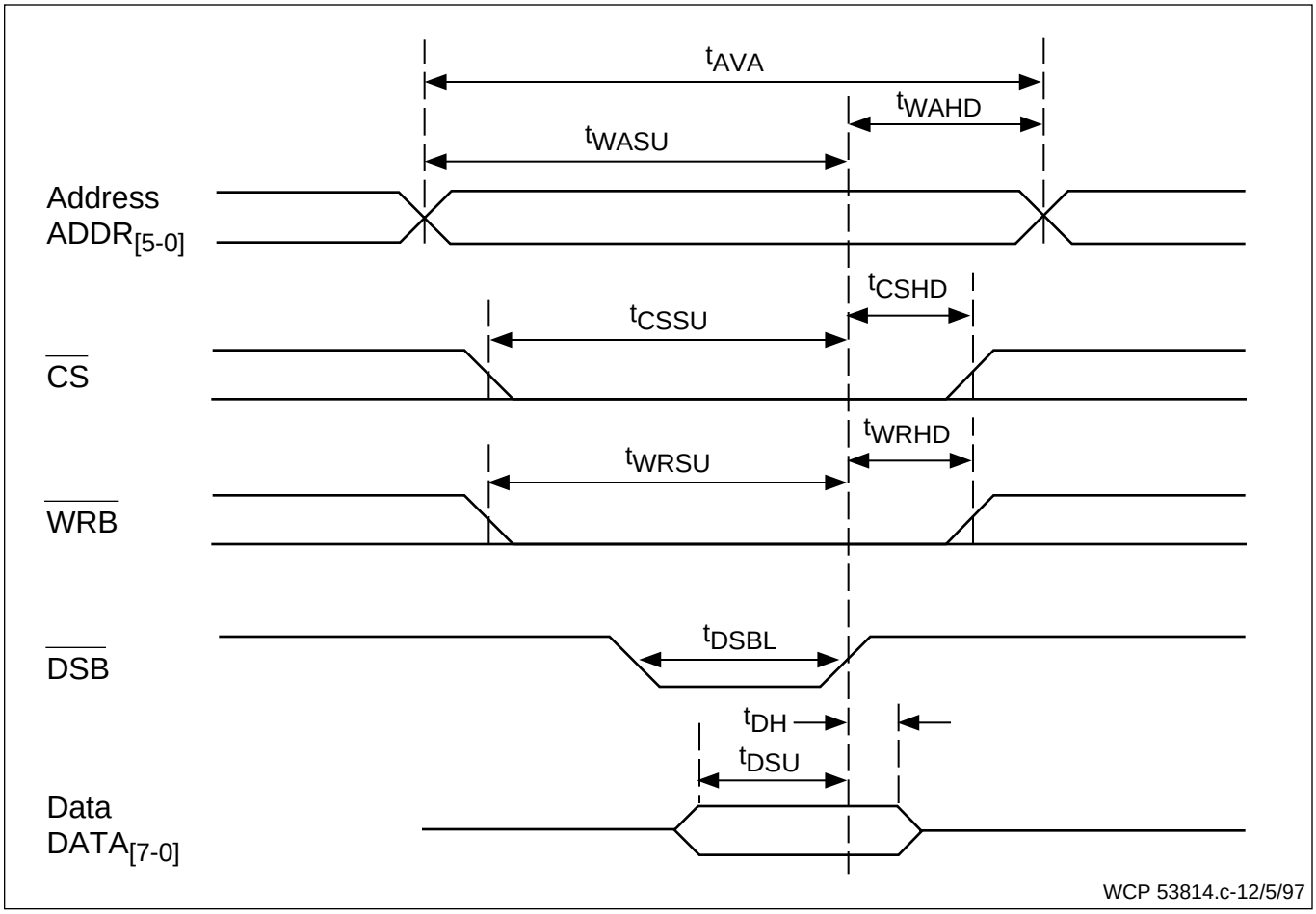


Table 55. Write Timing AC Characteristics

(V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, T_a = –40° to 85° C)

Symbol	Parameter	Min.	Nom.	Max.	Units	Conditions
t_{WASU}	Write Address Setup	10			nsec	
t_{WAHD}	Write Address Hold	6			nsec	
t_{AVA}	Address Valid Period	20			nsec	
t_{CSSU}	Chip Select ($\overline{CS}$) Setup	5			nsec	
t_{CSHD}	Chip Select ($\overline{CS}$) Hold	3			nsec	
t_{WRSU}	Write Setup ($\overline{WRB}$)	5			nsec	
t_{WRHD}	Write Hold ($\overline{WRB}$)	3			nsec	
t_{DSBL}	Data Strobe Pulse Width	10			nsec	
t_{DH}	Data Hold Time	1			nsec	
t_{DSU}	Data Setup Time	3			nsec	

READ TIMING

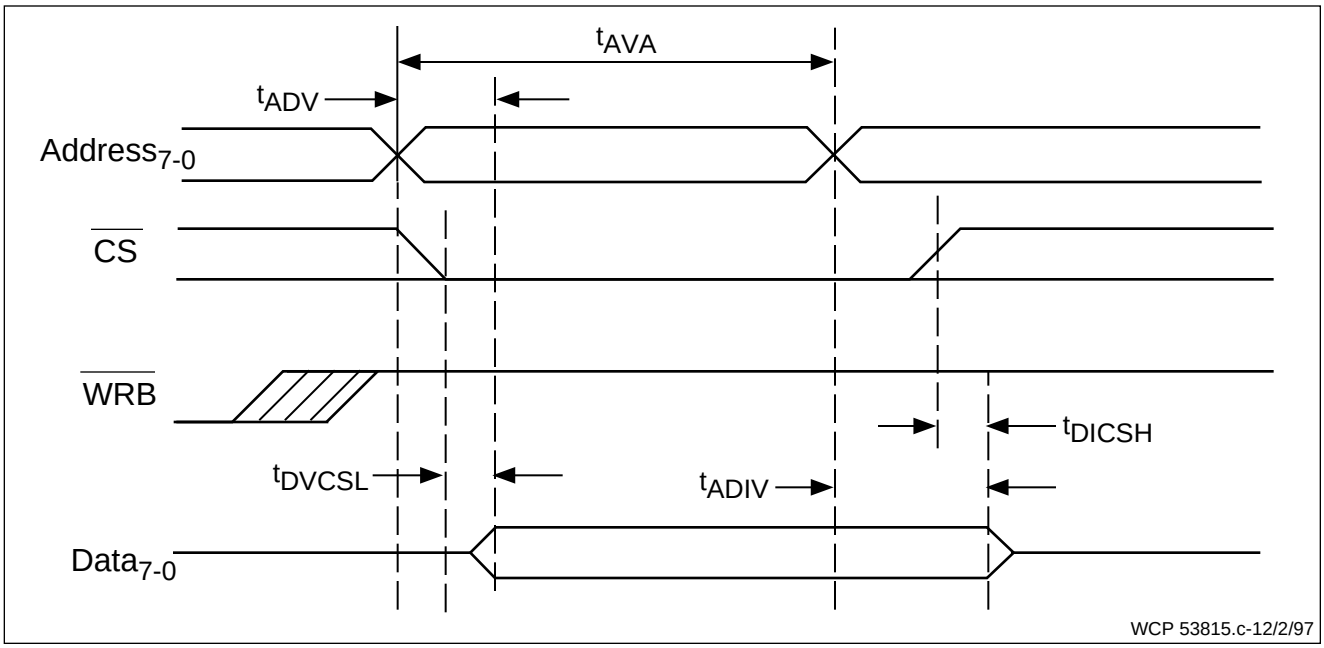
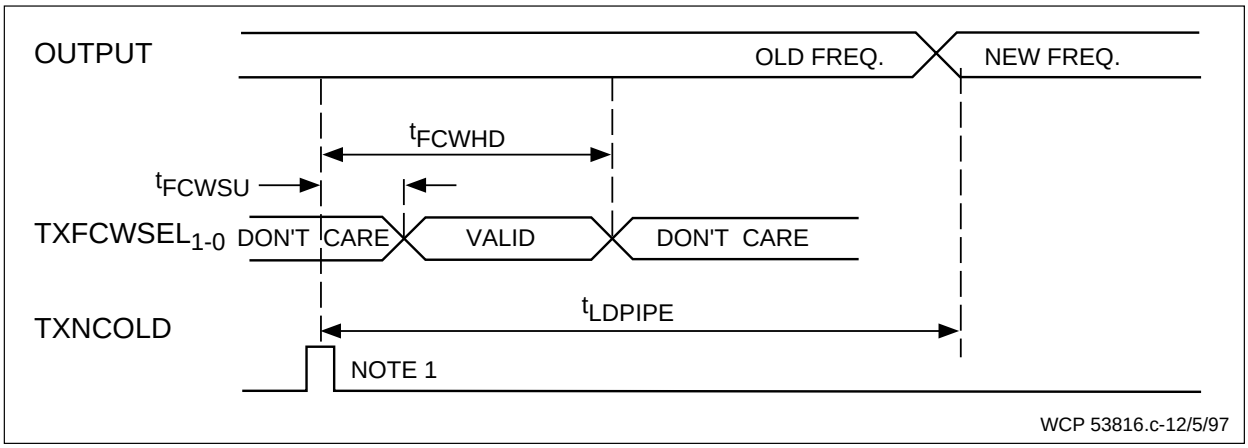


Table 56. Read Timing AC Characteristics

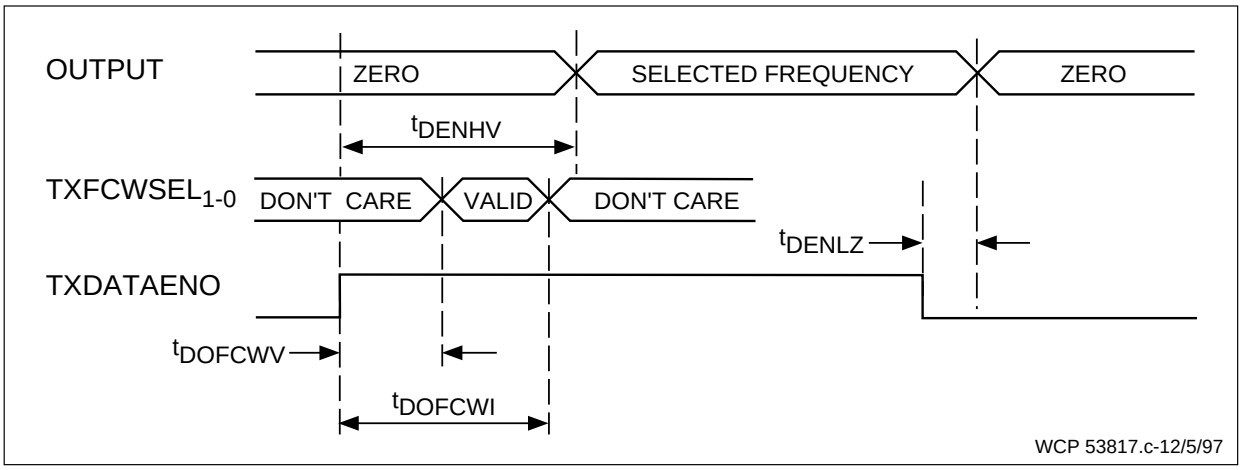
(V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, T_a = –40° to 85° C)

Symbol	Parameter	Min.	Nom.	Max.	Units	Conditions
t_{AVA}	Address Valid Period	20			nsec	
t_{ADV}	Address to Data Valid Delay			9	nsec	
t_{ADIV}	Address to Data Invalid Delay	6			nsec	
t_{DVCSL}	Data Valid After Chip Select Low	2			nsec	
t_{DICSH}	Data Invalid After Chip Select High			1	nsec	

NCO LOADING (USER CONTROLLED)



NCO LOADING (AUTOMATIC)



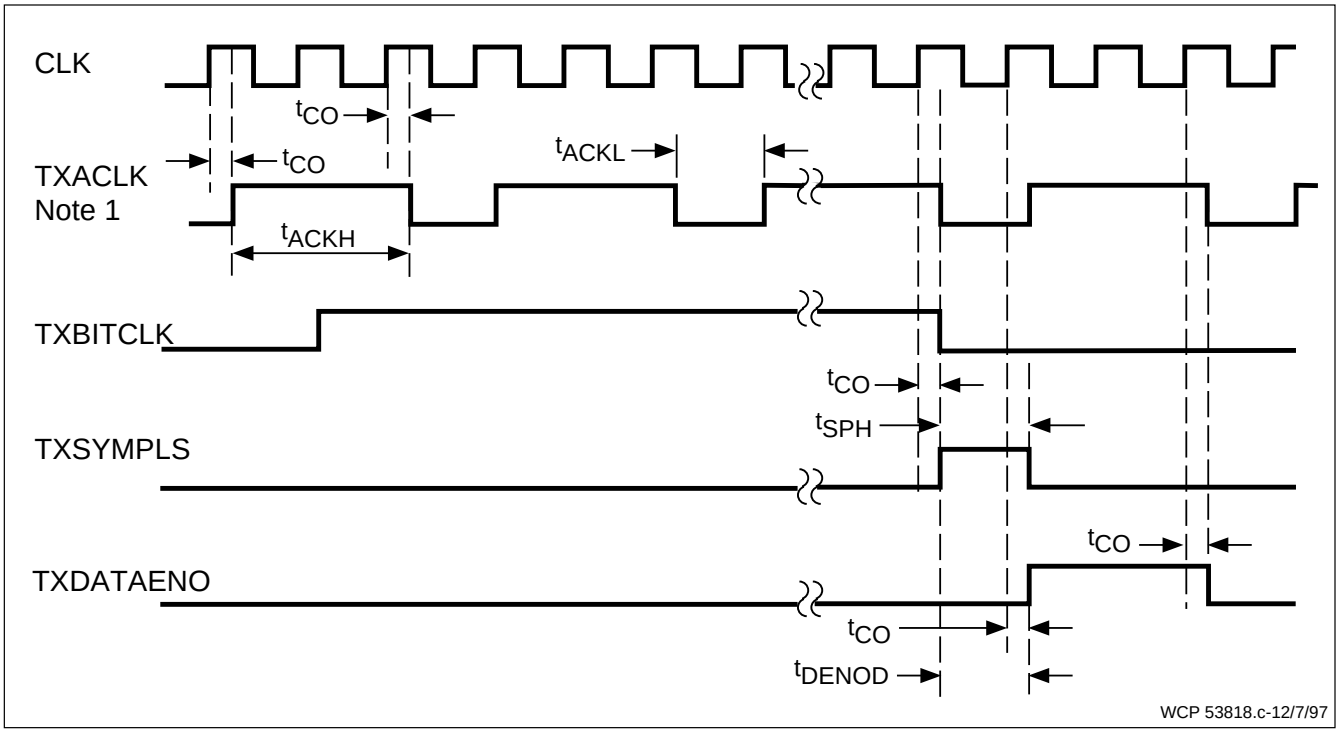
NOTE 1: The first rising edge of CLK after TXNCOLD goes high initiates the load process.

Table 57. NCO Loading AC Characteristics

(V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, T_a = –40° to 85° C)

Symbol	Parameter	Min.	Nom.	Max.	Units	Conditions
t_{LDPIPE}	NCO-LD to Change in Output Frequency Pipeline Delay		23		CLK cycles	
t_{FCWSU}	TXFCWSEL$_{1-0}$ to NCO-LD Setup			3	CLK cycles	
t_{FCWHD}	TXFCWSEL$_{1-0}$ to NCO-LD Hold	10			CLK cycles	
t_{DENLZ}	TXDATAENO Low to Zero Frequency Out Delay		23		CLK cycles	
t_{DENHV}	TXDATAENO High to Valid Frequency Out Delay		23		CLK cycles	
t_{DOFCWV}	TXDATAENO to TXFCWSEL$_{1-0}$ Valid			3	CLK cycles	
t_{DOFCWI}	TXDATAENO to TXFCWSEL$_{1-0}$ Invalid	10			CLK cycles	

DIGITAL OUTPUT TIMING



NOTE 1: TXACLK shown for "n" equal to 2: where n is the 4-bit binary value in Block 2 Register $2A_H$, BITS 3-0.

Table 58. Digital Output Timing AC Characteristics

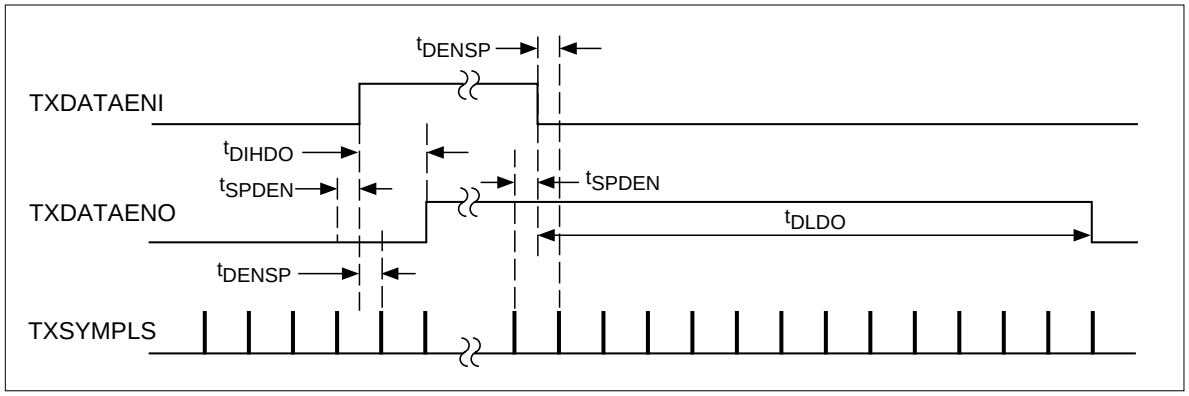
(V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, T_a = –40° to 85° C)

Symbol	Parameter	Min.	Nom.	Max.	Units	Conditions
t_{CO}	Clock to **TXBITCLK**, TXSYMPLS, TXDATAENO, or TXACLK edge			2	nsec	
t_{ACKH}	Auxiliary Clock (TXACLK) High		2		CLK cycles	
t_{ACKL}	Auxiliary Clock (TXACLK) Low		(n-1)		CLK cycles	Note 1
t_{SPH}	Symbol Pulse (TXSYMPLS) High		1		CLK cycles	
t_{DENOD}	TXBITCLK Low to TXDATAENO edge		1		CLK cycles	

Notes:

1. "n" is the 4-bit binary value in Block 2 Register $2A_H$, bits 3-0.

TXDATAENI TO TXDATAENO TIMING



WCP 53819.c-12/5/97

Table 59. TXDATAENI to TXDATAENO Timing AC Characteristics

(V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, T_a = –40° to 85° C)

Symbol	Parameter	Min.	Nom.	Max.	Units	Conditions
t_{DIHDO}	TXDATAENI High to TXDATAENO High		2nd		TXSYMPLS	Note 1
t_{DLDO}	TXDATAENI Low to TXDATAENO Low		13th		TXSYMPLS	Note 1
t_{SPDEN}	TXSYMPLS (trailing edge) to TXDATAENI Setup	3			nsec	
t_{DENSP}	TXDATAENI to TXSYMPLS (trailing edge) Setup	5			nsec	

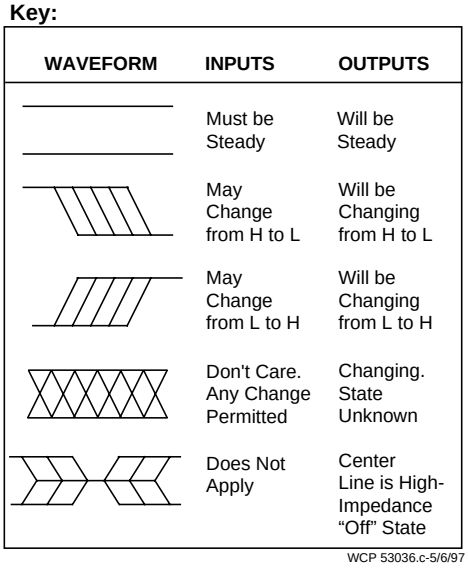
Notes:

1. Shown for Block 2 Register 36_H, bit 6=0 (No Reed-Solomon). If bit 6 of Register 36_H is a "1", then the edges of TXDATAENO will be delayed from those illustrated by 8, 4, or 2 TXSYMPLS for BPSK, QPSK, or 16QAM, respectively.

BURST TIMING EXAMPLES

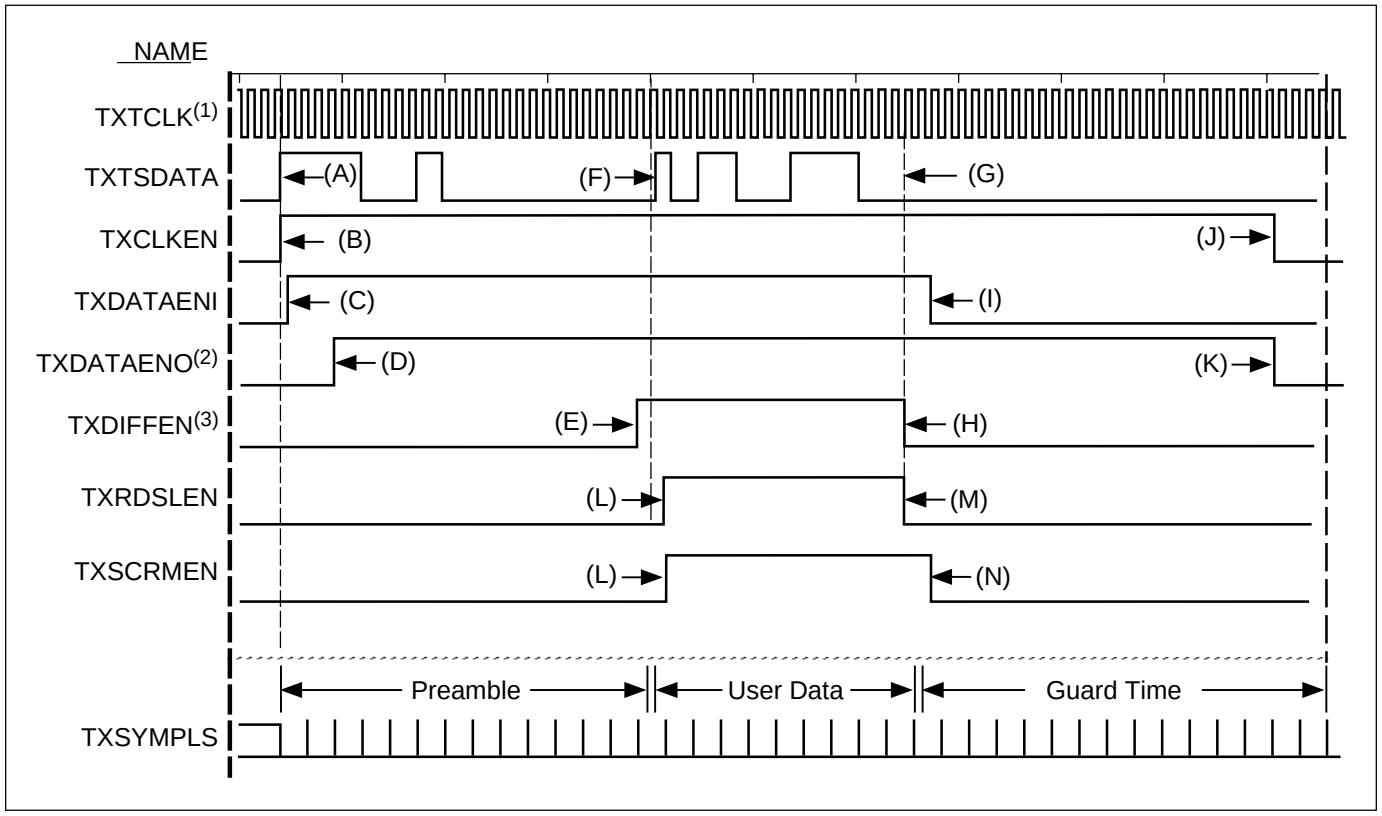
The following seven timing diagrams are qualitative in nature and meant to illustrate the functional relationships between the control inputs and signal outputs in various modes of burst operation. Use the key at right to interpret the timing marks. Only the first diagram is of a complete and realistic burst. The remaining diagrams are too short in duration to show TXDATAENO and TXCLKEN going low.

Key:



WCP 53036.c-5/6/97

SLAVE MODE, QPSK - BURST TIMING: FULL BURST



WCP 53820.c -12/5/97

NOTES:

(1) All input signals shown are derived from TXTCLK. Each edge is delayed from a TXTCLK edge by typically 6 to 18 nsec. DATAENO does not depend on TXTCLK but its edges are synchronized to TXTCLK. TXTCLK itself can be turned off after TXDATAENI goes low.

(2) DATAENO shown at its minimum pipeline delay position. This is achieved by setting bit 6 of Block 2 Register 36_H to zero. Reed-Solomon cannot be used in this mode. If bit 6 is set high, allowing Reed-Solomon an additional pipeline delay of 8 bits is inserted into the data path. This will shift both edges of DATAENO to the right by 8 cycles of TXTCLK.

(3) If the preamble is not encoded the same as the user data, the TXDIFFEN control can be toggled in mid transmission as shown. Otherwise, the TXDIFFEN control can be held high or low depending on encoding desired.

(A) First data bit transition on falling edge of TXTCLK (first of 14 preamble symbols). The data will be valid on the next rising edge of TXTCLK.

(B) TXCLKEN rises on the same falling edge of TXTCLK that the data starts on. TXCLKEN is allowed to rise any time earlier than shown.

(C) TXDATAENI rises on the first rising edge of TXTCLK (middle of the first preamble bit).

(D) DATAENO rises on the falling edge of TXTCLK (at the end of the second symbol).

(E) TXDIFFEN rises on the rising edge of TXTCLK one symbol before the first user data symbol.

(F) User data bits change on the falling edge of TXTCLK and must be valid during the next rising edge of TXTCLK.

(G) End of user data. Note that the data is allowed to go away immediately after it is latched in by the rising of TXTCLK which occurs in the middle of the last user data bit.

(H) TXDIFFEN goes low on rising edge of TXTCLK (last user data symbol).

(I) TXDATAENI goes low on rising edge of TXTCLK (on the cycle of TXTCLK after the last user data bit).

(J) TXCLKEN must stay high until any time on or after the point where DATAENO goes low.

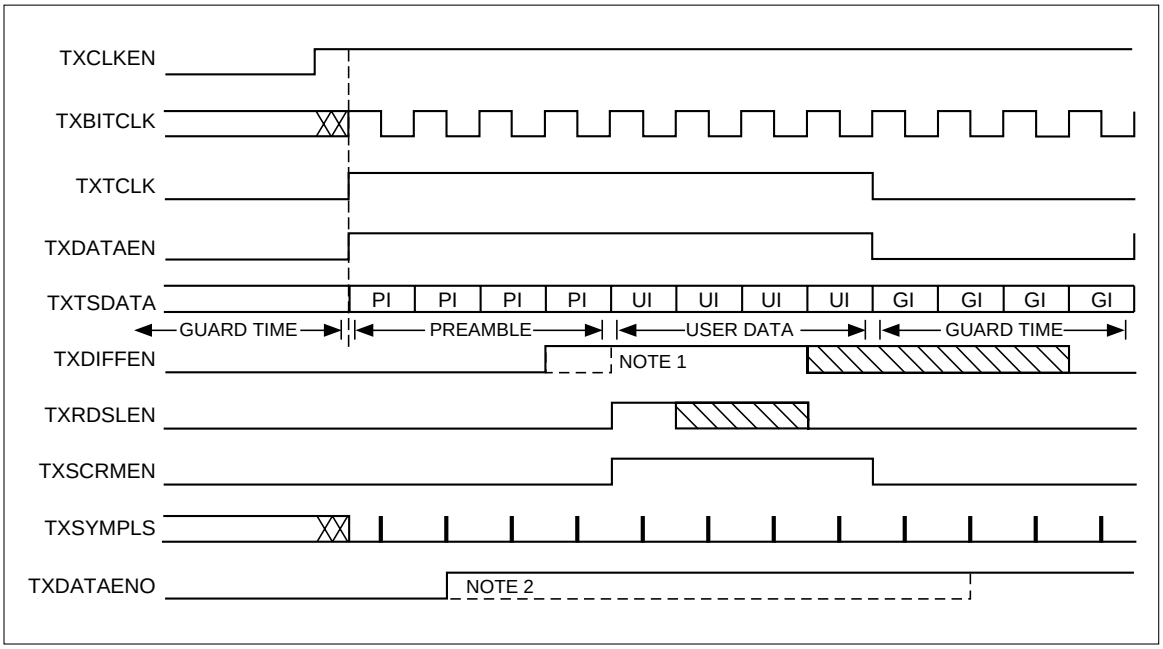
(K) DATAENO stays high until the 13th TXSYMPLS after TXDATAENI goes low.

(L) TXRDSLEN and TXSCRMEN go high on the first rising edge of TXTCLK in the User Data.

(M) TXRDSLEN goes low on the rising edge of TXTCLK (last user data symbol).

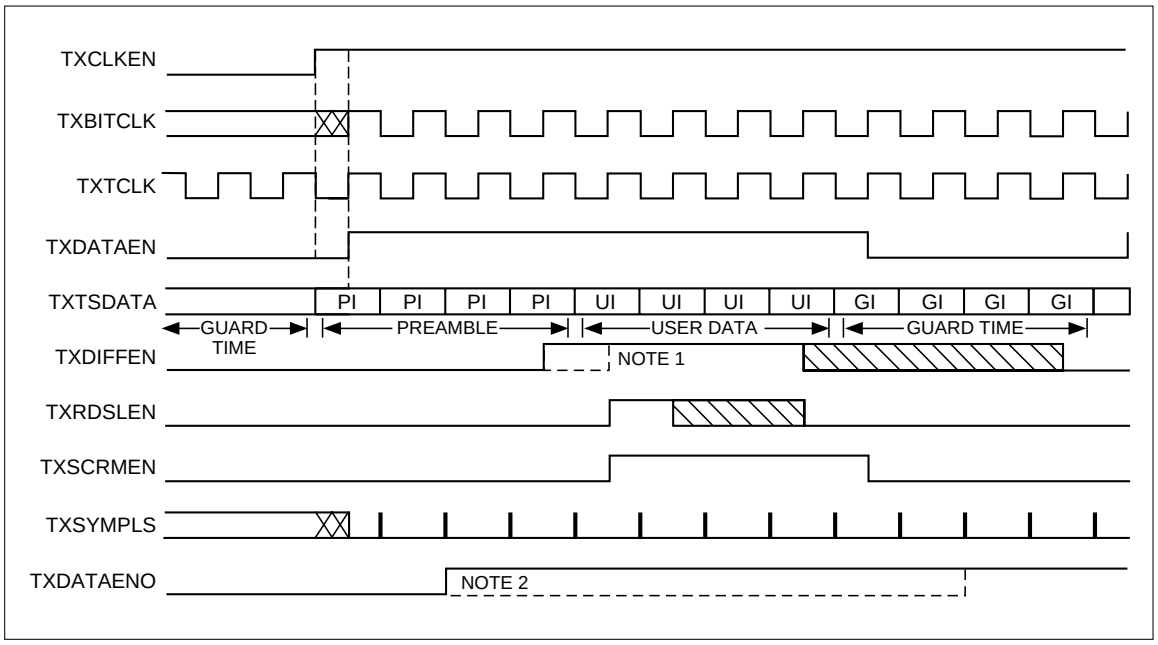
(N) TXSCRMEN goes low on the rising edge of TXTCLK (on the cycle of TXTCLK after the last user data bit).

MASTER MODE, BPSK - BURST TIMING SIGNAL RELATIONSHIPS



WCP 53837.c-12/5/97

SLAVE MODE, BPSK - BURST TIMING SIGNAL RELATIONSHIPS

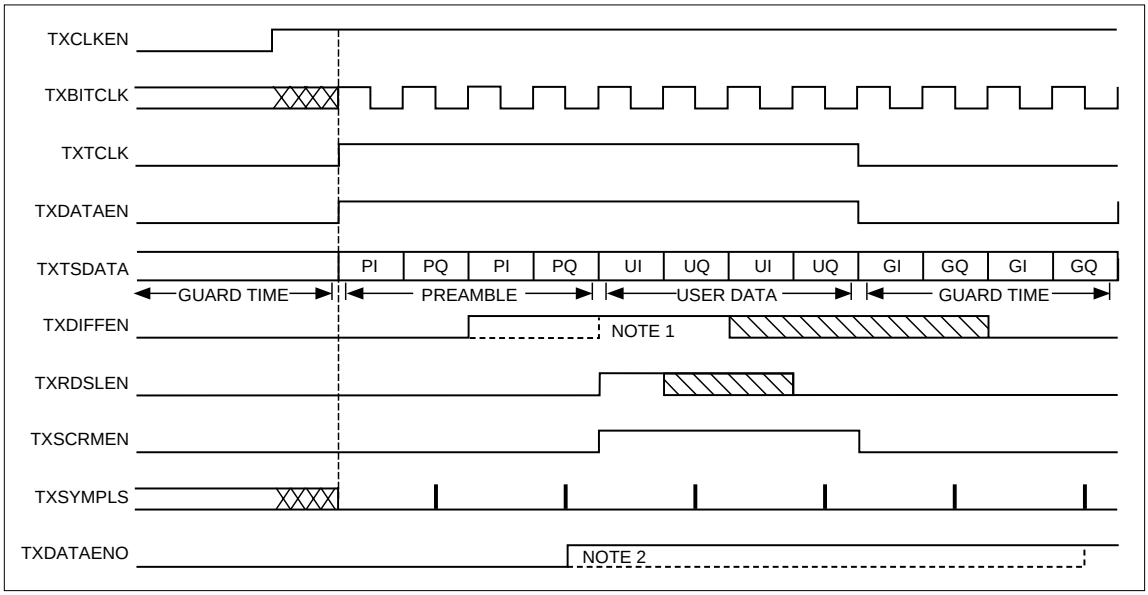


WCP 53838.c-12/5/97

NOTE 1: STEL receivers differentially decode relative to the last preamble symbol. To encode the first symbol against a "zero" symbol reference instead, bring TXDIFFEN high at the leading edge of the user data packet (dotted line).

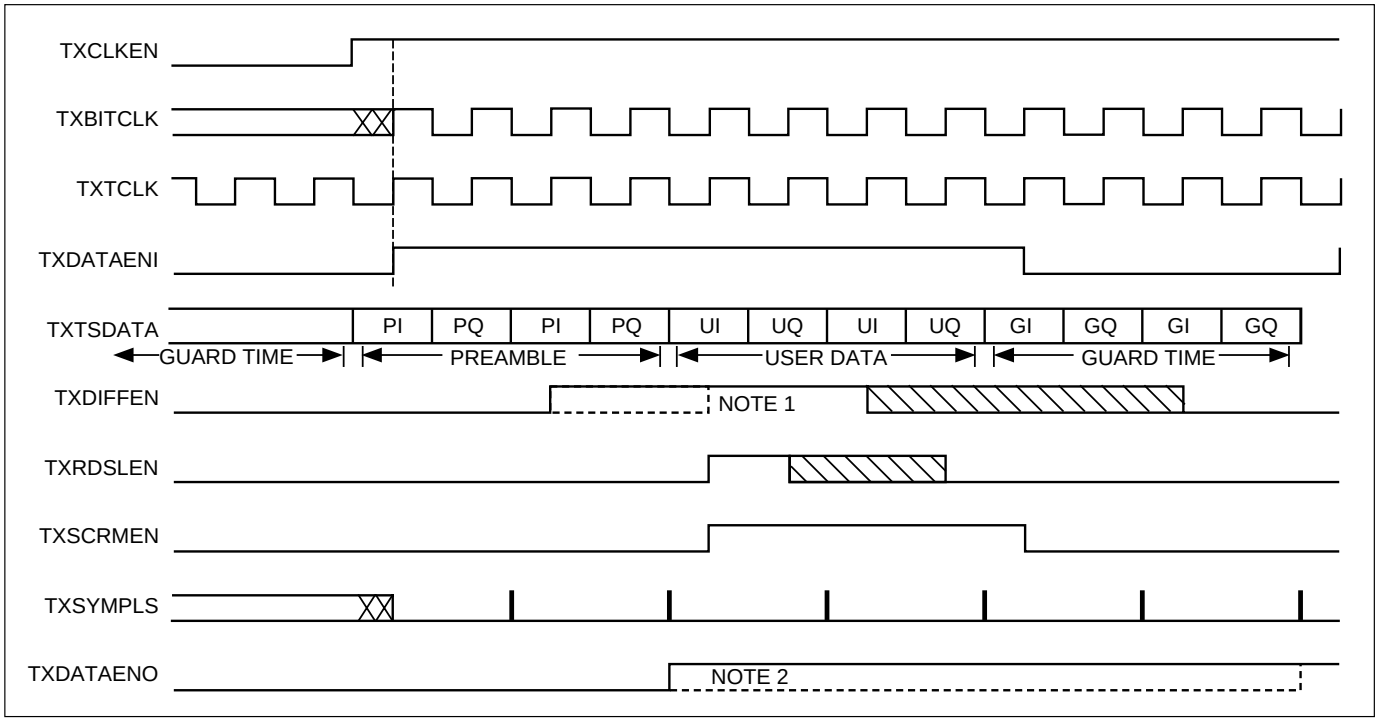
NOTE 2: If bit 6 of Block 2 Register 36_H is a "1" then the rising edge of DATAENO will be delayed by eight cycles of TXBITCLK (dotted line). This is required if the Reed-Solomon encoder is used.

MASTER MODE, QPSK - BURST TIMING SIGNAL RELATIONSHIPS



WCP 53821.c-12/5/97

SLAVE MODE, QPSK: FULL VIEW - BURST TIMING SIGNAL RELATIONSHIPS

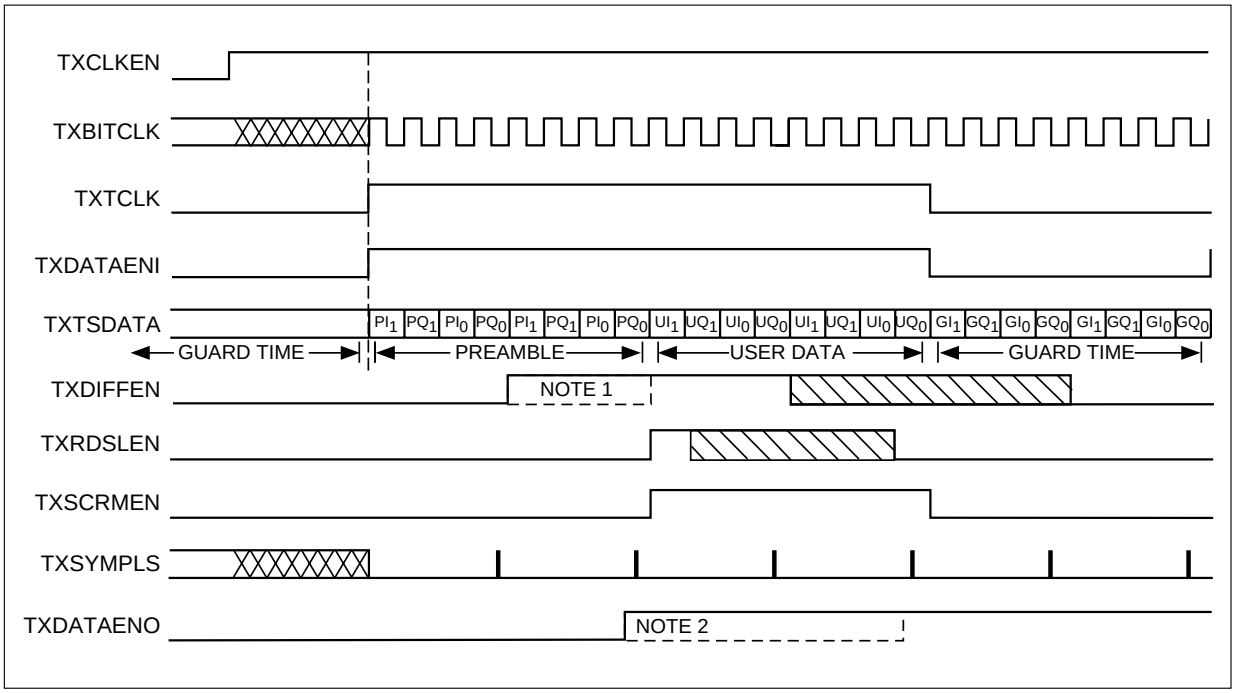


WCP 53822.c-12/5/97

NOTE 1: STEL receivers differentially decode relative to the last preamble symbol. To encode the first symbol against a "zero" symbol reference instead, bring TXDIFFEN high at the leading edge of the user data packet (dotted line).

NOTE 2: If bit 6 of Block 2 Register 36_H is a "1" then the rising edge of DATAENO will be delayed by eight cycles of TXBITCLK (dotted line). This is required if the Reed-Solomon encoder is used.

MASTER MODE, 16QAM - BURST TIMING SIGNAL RELATIONSHIPS

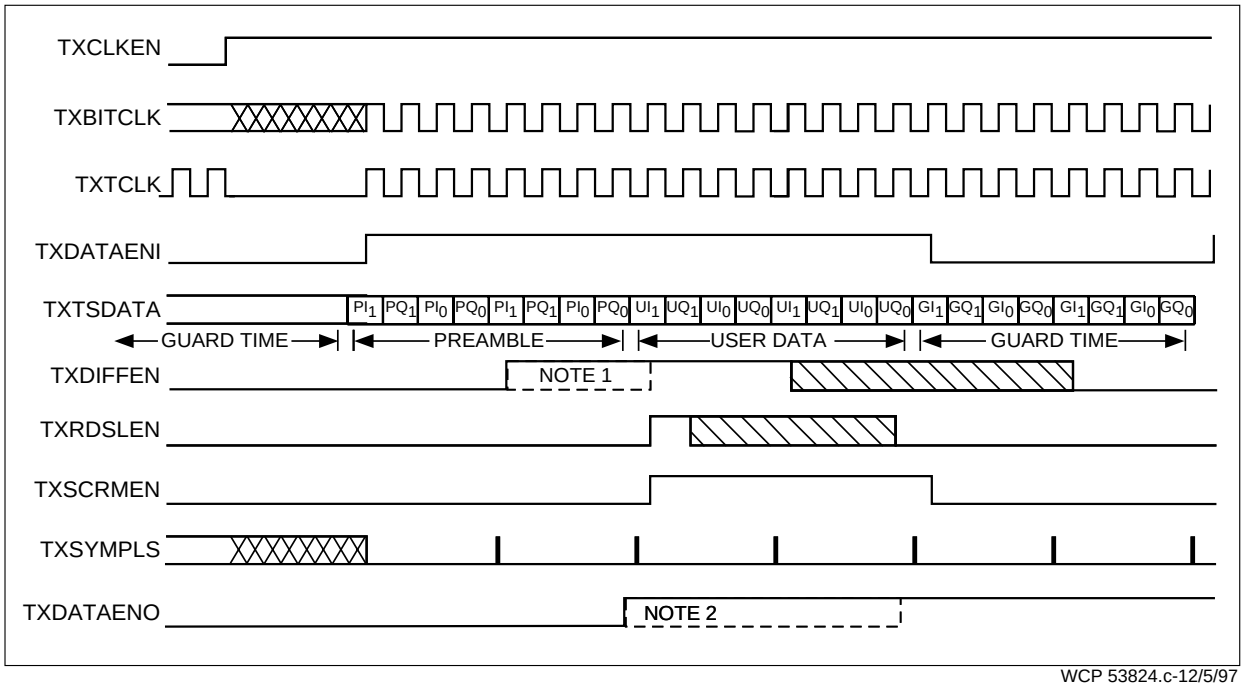


WCP 53823.c-12/5/97

NOTE 1: STEL receivers differentially decode relative to the last preamble symbol. To encode the first symbol against a "zero" symbol reference instead, bring TXDIFFEN high at the leading edge of the user data packet (dotted line).

NOTE 2: If bit 6 of Block 2 Register 36_H is a "1" then the rising edge of DATAENO will be delayed by eight cycles of TXBITCLK (dotted line). This is required if the Reed-Solomon encoder is used.

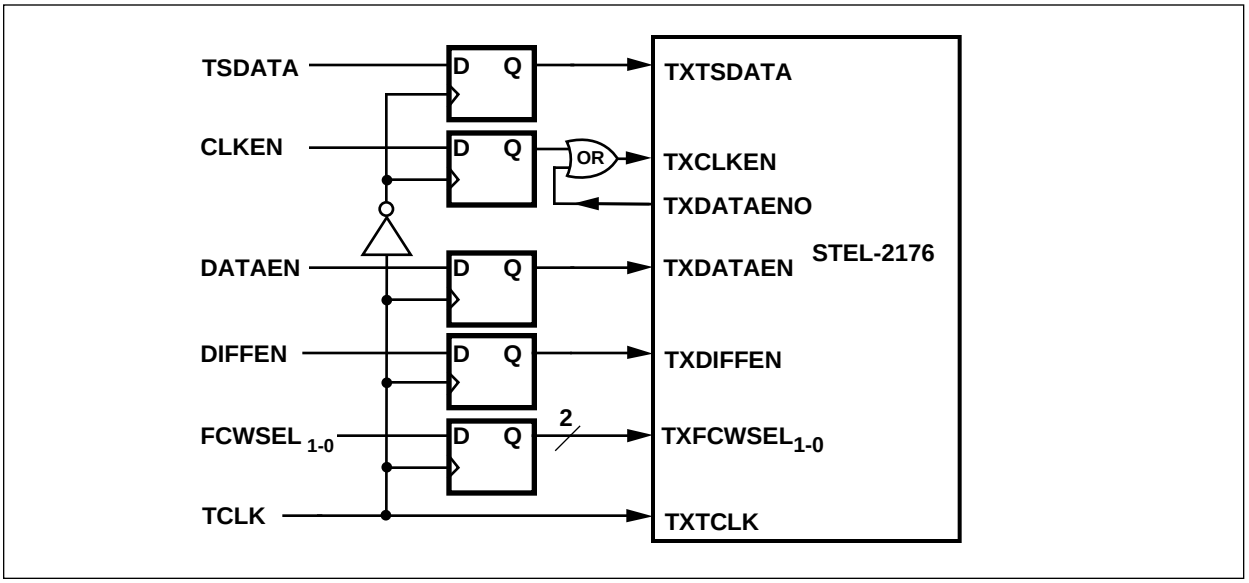
SLAVE MODE, 16QAM - BURST TIMING SIGNAL RELATIONSHIPS



WCP 53824.c-12/5/97

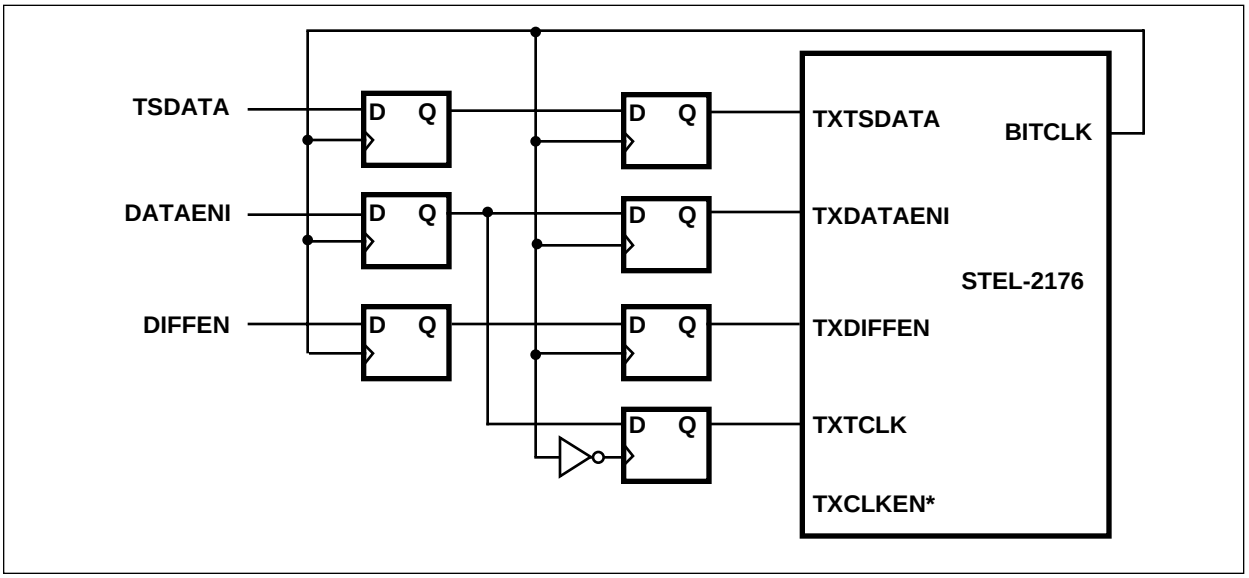
RECOMMENDED INTERFACE CIRCUITS

SLAVE MODE INTERFACE



WCP 52995.c-5/2/97

MASTER MODE INTERFACE



WCP 52115A.c 5/2/97

* TXCLKEN may be turned off between bursts to conserve power as long as it is kept on until after TXDATAENO goes low. Note that the TXBITCLK output goes inactive whenever TXCLKEN is low.

For Further Information Call or Write

INTEL CORPORATION
Cable Network Operation
350 E. Plumeria Drive, San Jose, CA 95134
Customer Service Telephone: (408) 545-9700
Technical Support Telephone: (408) 545-9799
FAX: (408) 545-9888

WCP 970317