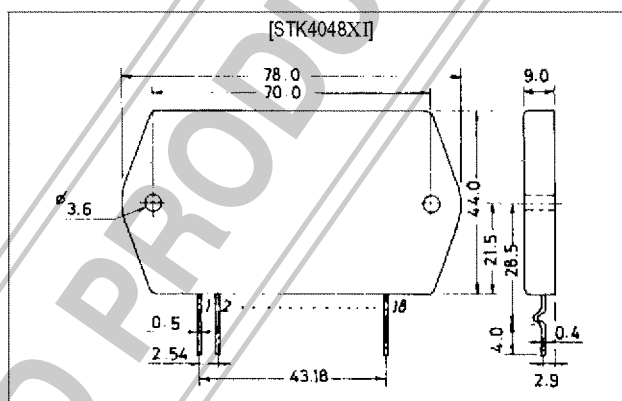


SANYO**STK4048XI****AF Power Amplifier (Split Power Supply)
(150W min, THD = 0.008%)****Features**

- The use of a current mirror circuit, cascode circuit, pure complementary circuit provides low distortion (THD= 0.008%/100kHz LPF ON).
- Possible to design electronic supplementary circuits (pop noise muting at the time of power ON/OFF, load short protector, thermal shutdown)

Package Dimensions

unit: mm

4051A**Specifications****Maximum Ratings** at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$		± 87	V
Thermal resistance	θ_{j-c}	Per power Transistor	1.2	$^\circ\text{C/W}$
Junction temperature	T_j		150	$^\circ\text{C}$
Operating substrate temperature	T_c		125	$^\circ\text{C}$
Storage temperature	T_{stg}		-30 to +125	$^\circ\text{C}$

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

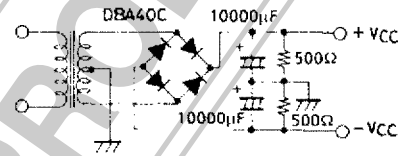
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		± 60	V
Load resistance	R_L		8	Ω

Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = \pm 60\text{V}$, $R_L = 8\Omega$, $V_G = 40\text{dB}$, $R_g = 600\Omega$, 100kHz LPF ON,
 R_L : noninductive load

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	I_{CC}	$V_{CC} = \pm 72\text{V}$	15		120	mA
Output power	P_o	THD = 0.008%, $f = 20\text{Hz to } 20\text{kHz}$	150			W
Total harmonic distortion	THD	$P_o = 1.0\text{W}$, $f = 1\text{kHz}$			0.008	%
Frequency response	f_L, f_H	$P_o = 1.0\text{W}$, $+0_{-3}\text{ dB}$		20 to 50k		Hz
Input impedance	r_i	$P_o = 1.0\text{W}$, $f = 1\text{kHz}$		55		$k\Omega$
Output noise voltage	V_{NO}^*	$V_{CC} = \pm 72\text{V}$, $R_g = 10k\Omega$			1.2	mVrms
Neutral voltage	V_N	$V_{CC} = \pm 72\text{V}$	-70	0	+70	mV

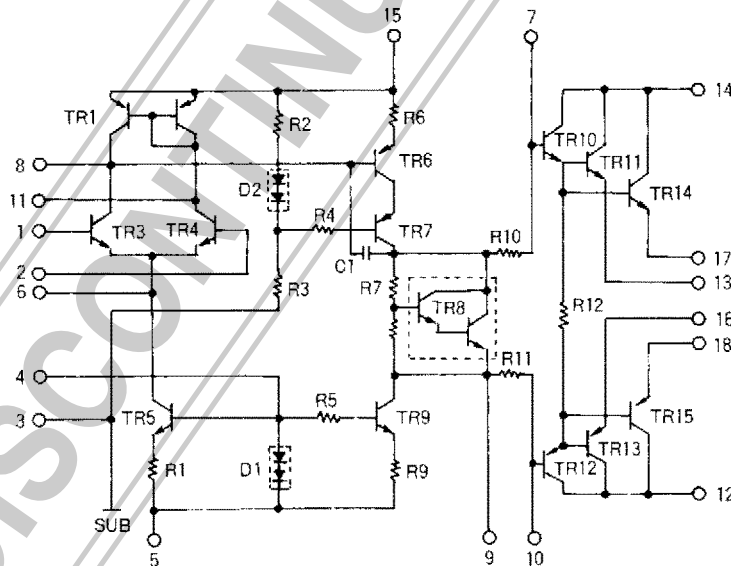
Notes. For power supply at the time of test, use a constant-voltage power supply unless otherwise specified.

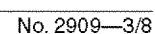
*The output noise voltage is represented by the peak value on rms scale (VTVM) of average value indicating type. The noise voltage waveform includes no flicker noise. For measurement of the output noise voltage, use the specified transformer power supply shown right.

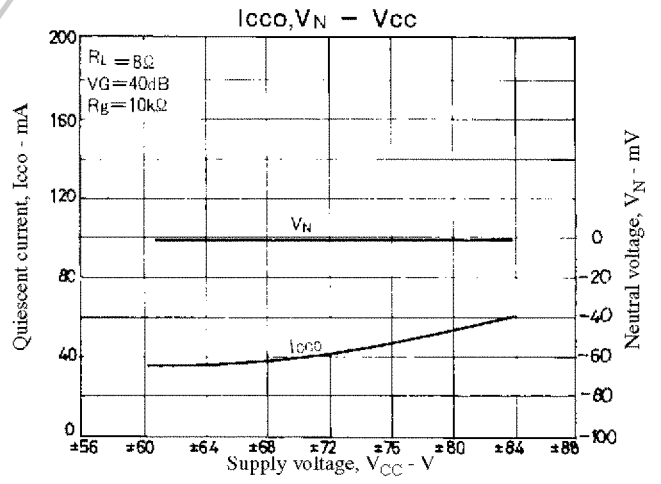
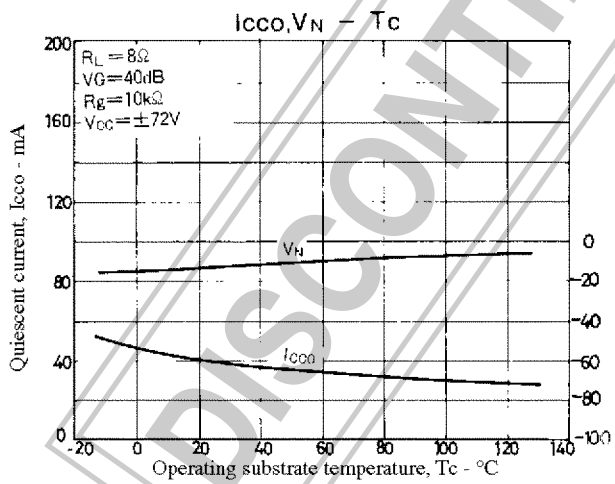
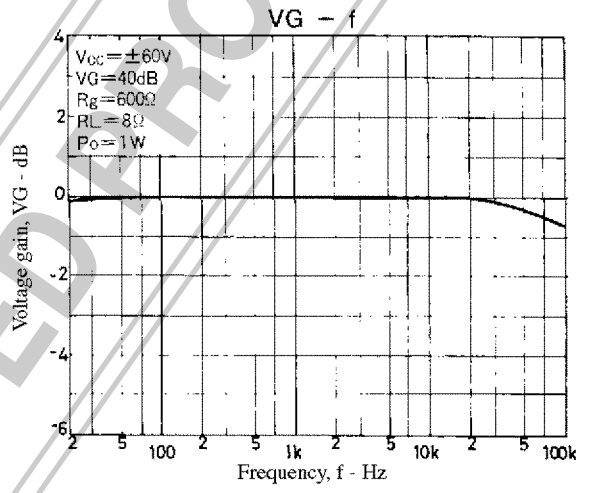
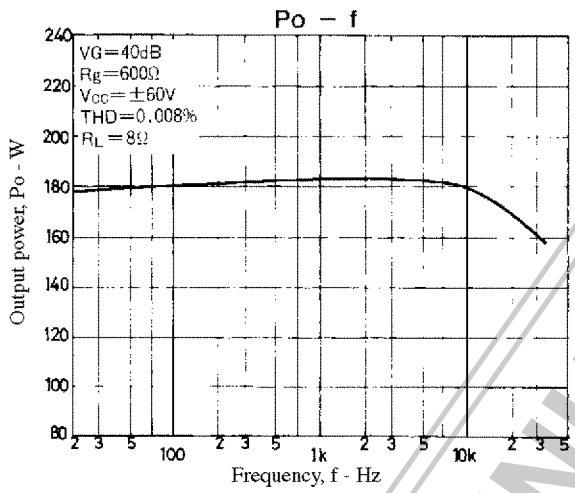
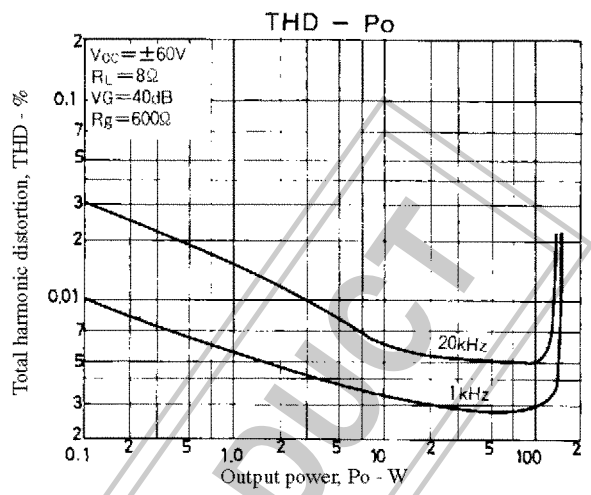
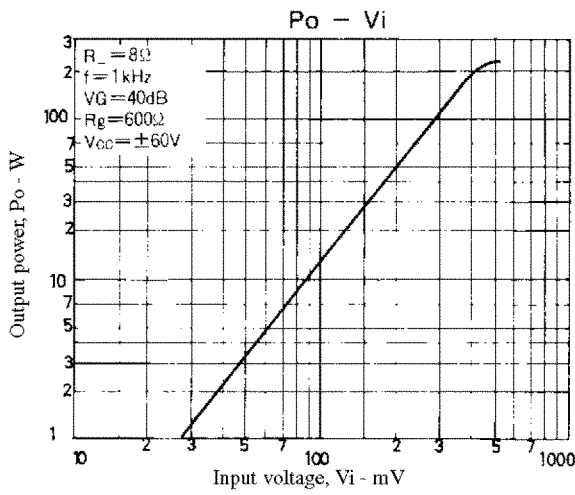


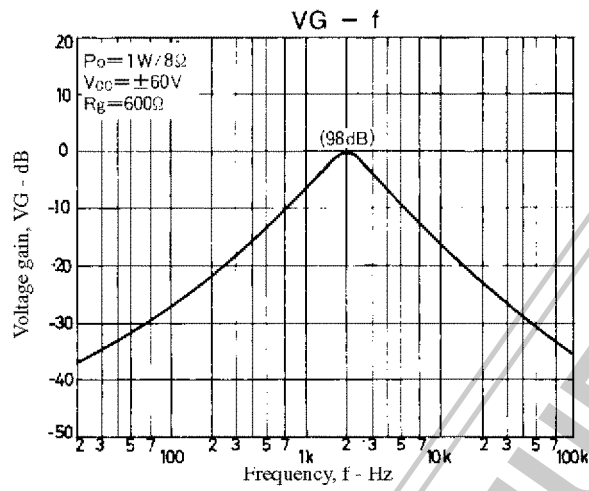
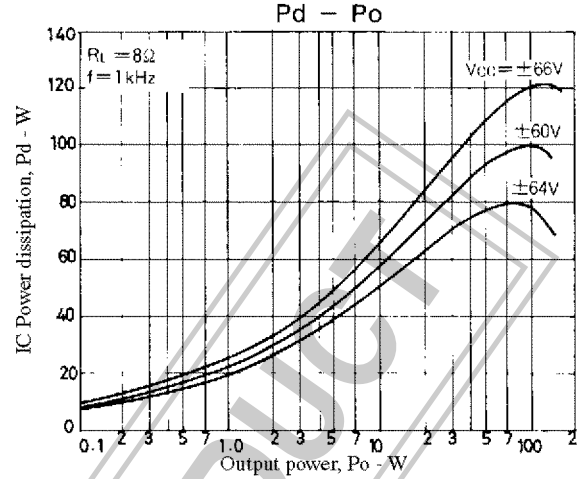
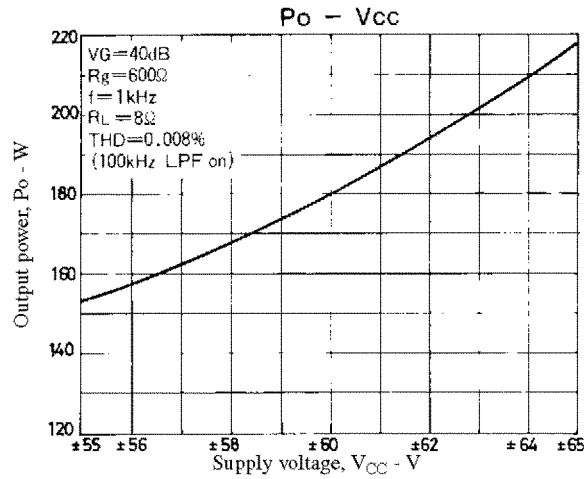
Specified Transformer Power Supply
(Equivalent to MG250)

Equivalent Circuit

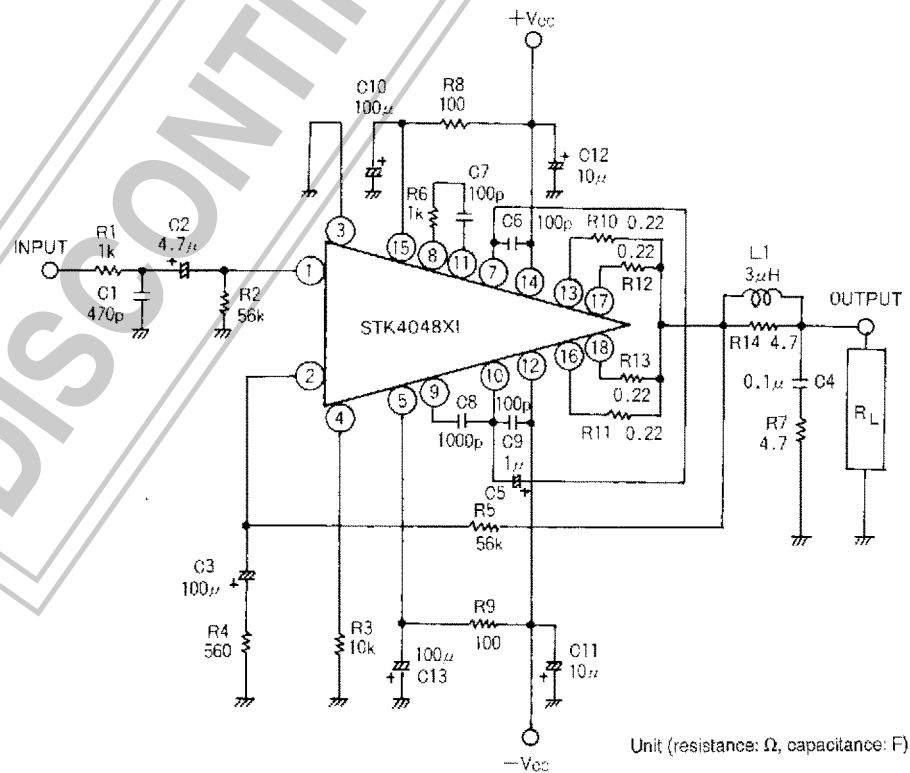


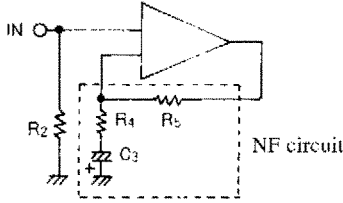






Description of External Parts



R1, C1	Input filter circuit • Used to reduce noise at high frequencies.
C2	Input coupling capacitor • Used to block DC current. When the reactance of the capacitor increases at low frequencies, the dependence of 1/f noise on signal source resistance causes the output noise to worsen. It is better to decrease the reactance.
R2	Input bias resistor • Used to bias the input pin to zero. • Affects V_N stability. (See NF circuit.) • Because of differential input, this resistor fixes the input resistance practically.
R4, R5 C3 (C2)	<p>NFB circuit (AC NF circuit). It is desirable that the error of the resistor value is 1% or less.</p>  <p>C3 : Capacitor for AC NF R4, R5 : Used to set VG</p> <p>• VG setting obtained by using R4, R5 $VG = \log 20 \cdot \frac{R_5}{R_4} (40\text{dB is recommended})$</p> <p>• Low cutoff frequency setting obtained by using, R4, C3 $f_L = \frac{1}{2\pi \cdot R_4 \cdot C_3} (\text{Hz})$</p> <p>• Change of VG setting • It is desirable to change R4. In this case, the low cutoff frequency setting needs to be rechecked. • When VG setting is changed by changing R5, R5 must be made equal to R2 to ensure V_N balance. If the resistor value is increased more than the existing value, it may be hard to ensure V_N balance and the temperature characteristic of V_N may be also deteriorated.</p>
R3	First-stage constant-current bias resistor
R6, C7	Used for oscillation blocking and phase compensation
R7, C4	Used for oscillation blocking and phase compensation (C4 : A polyester film capacitor is recommended.)
C6, C9	Used for oscillation blocking and phase compensation (Must be connected near the pin) C6 : Power amp on (+) side C9 : Power amp on (–) side
C4	Used for oscillation blocking and phase compensation (Used for oscillation blocking before clip)
C5	Used for oscillation blocking and distortion improvement
C8, C10	Ripple filter circuit on (+) side
R9, C13	Ripple filter circuit on (–) side
C11, C12	Used for oscillation blocking • Used to decrease the power supply impedance to operate the IC stably. Must be connected near the IC pin. It is desirable to use an electrolytic capacitor.
L1, R14	Used for oscillation blocking
R10, R11 R12, R13	Output limiting resistors

Thermal Design

The IC power dissipation of the STK4048XI at the IC-operated mode is 100W max. at load resistance 8Ω for continuous sine wave as shown in Figure 1.

In an actual application where a music signal is used, it is impractical to estimate the power dissipation based on the continuous signal as shown right, because too large a heat sink must be used. It is reasonable to estimate the power dissipation as $1/10 P_o$ max. (EIAJ).

That is, $P_d = 65W$ at 8Ω

Thermal resistance θ_{c-a} of a heat sink for this IC power dissipation (P_d) is fixed under conditions 1 and 2 shown below.

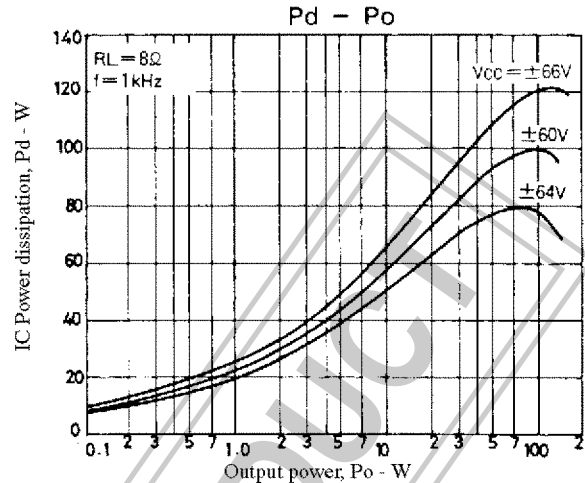


Figure 1. STK4048XI $P_d - P_o$ ($R_L = 8\Omega$)

$$\text{Condition 1: } T_c = P_d \times \theta_{c-a} + T_a \leq 125^\circ\text{C} \quad (1)$$

where T_a : Specified ambient temperature
 T_c : Operating substrate temperature

$$\text{Condition 2: } T_j = P_d \times (\theta_{c-a}) + P_d/4 \times (\theta_{j-c}) + T_a \leq 150^\circ\text{C} \quad (2)$$

where T_j : Junction temperature of power transistor

Assuming that the power dissipation is shared equally among the four power transistors, thermal resistance θ_{j-c} is 1.2°C/W and

$$P_d \times (\theta_{c-a} + 1.2/4) + T_a \leq 150^\circ\text{C} \quad (3)$$

Thermal resistance θ_{c-a} of a heat sink must satisfy inequalities (1) and (3).

Figure 2 shows the relation between P_d and θ_{c-a} given from (1) and (3) with T_a as a parameter.

[Example] The thermal resistance of a heat sink is obtained when the ambient temperature specified for a stereo amplifier is 50°C .

Assuming $V_{CC} = \pm 60V$, $R_L = 8\Omega$,
 $R_L = 8\Omega$: $P_d = 65W$ at $1/10 P_o$ max.

The thermal resistance of a heat sink is obtained from Figure 2.

$R_L = 8\Omega$: $\theta_{c-a1} = 1.15^\circ\text{C/W}$

T_j when a heat sink is used is obtained from (3).

$R_L = 8\Omega$: $T_j = 144.3^\circ\text{C}$

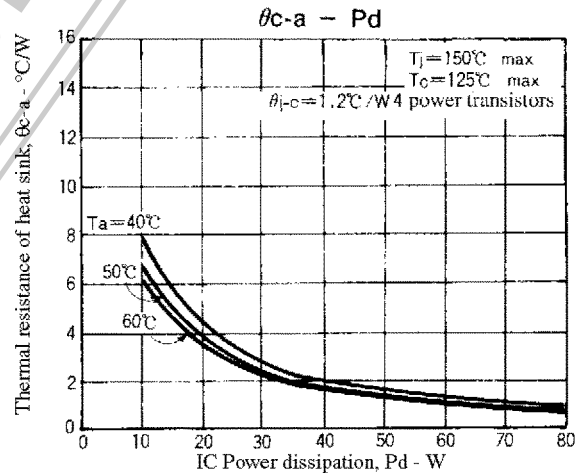


Figure 2. STK4048XI $\theta_{c-a} - P_d$

This design is based on the use of a constant-voltage regulated power supply. P_d differs when a transformer power supply is used. Redesign must be made based on P_d that suits the regulation of each transformer.

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