



STR71xF

ARM7TDMI™ 16/32-BIT MCU WITH FLASH, USB, CAN 5 TIMERS, ADC, 10 COMMUNICATIONS INTERFACES

PRELIMINARY DATA

■ Memories

- Up to 256+16 Kbytes Flash memory (100,000 cycles endurance, 20 yrs retention)
- Up to 64 Kbytes RAM
- External Memory Interface (EMI) for up to 4 banks of SRAM, Flash, ROM.
- Multi-boot capability

■ Clock, Reset and Supply Management

- 3.3V application supply and I/O interface
- Internal 1.8V voltage regulator for core supply
- 0 to 16 MHz external main oscillator
- 32 kHz external backup oscillator
- Embedded PLL for CPU clock
- Up to 50 MHz CPU operating frequency when executing from Flash
- Realtime Clock for clock-calendar function
- 4 power saving modes: SLOW, WAIT, STOP and STANDBY modes

■ Nested interrupt controller

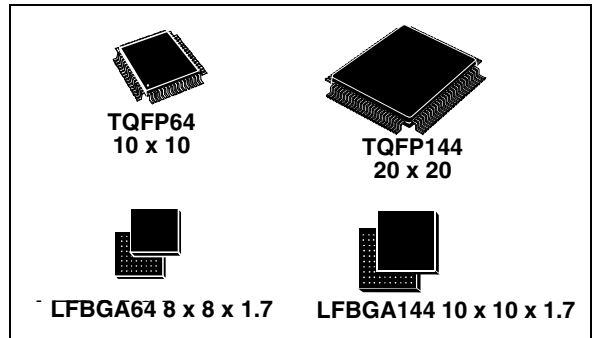
- Fast interrupt handling with multiple vectors
- 32 vectors with 16 IRQ priority levels
- 2 maskable FIQ sources

■ Up to 48 I/O ports

- 30/32/48 multifunctional bidirectional I/O lines
- 14 ports with interrupt capability

■ 5 Timers

- 16-bit watchdog timer
- 4 16-bit timers with: 2 input captures, 2 output compares, PWM and pulse counter modes



■ 10 Communications Interfaces

- 2 I²C interfaces (1 multiplexed with SPI)
- 4 UART asynchronous serial interfaces
- Smart Card ISO7816-3 interface on UART1
- 2 BSPI synchronous serial interfaces
- CAN interface (2.0B Active)
- USB v 2.0 Full Speed (12Mbit/s) Device Function with Suspend and Resume support
- HDLC synchronous communications

■ 4-channel 12-bit A/D Converter

- Conversion time:
 - 4 channels: up to 500 Hz (2 ms)
 - 1 channel: up to 1 kHz (1 ms)
- Conversion range: 0 to 2.5V

■ Development Tools Support

- JTAG with debug mode trigger request

Table 1. Device Summary

| Features | STR710FZ | | STR711FR | | | STR712FR | | | STR715FR |
|----------------------|---|--------|--|--------|--------|--------------|--------|--------|----------|
| | 1 | 2 | 0 | 1 | 2 | 0 | 1 | 2 | 0 |
| FLASH - Kbytes | 128+16 | 256+16 | 64+16 | 128+16 | 256+16 | 64+16 | 128+16 | 256+16 | 64+16 |
| RAM - Kbytes | 32 | 64 | 16 | 32 | 64 | 16 | 32 | 64 | 16 |
| Peripheral Functions | CAN, EMI, USB, 48 I/Os | | USB, 30 I/Os | | | CAN, 32 I/Os | | | 32 I/Os |
| Operating Voltage | 3.0 to 3.6V (optional 1.8V for core) | | | | | | | | |
| Operating Temp. | -40 to +85°C | | | | | | | | |
| Packages | T=TQFP144 20 x 20 H=LFBGA144 10 x 10 | | T=TQFP64 10 x 10 / H=LFBGA64 8 x 8 x 1.7 | | | | | | |

Rev. 6

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Note: For detailed information on the STR71xF Microcontroller memory, registers and peripherals. please refer to the STR71xF Reference Manual.

1 INTRODUCTION

This Preliminary Data provides the STR71x Ordering Information, Mechanical and Electrical Device Characteristics.

For complete information on the STR71xF Microcontroller memory, registers and peripherals, please refer to the STR71xF Reference Manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash Programming Reference Manual

For information on the ARM7TDMI core please refer to the ARM7TDMI Technical Reference Manual.

1.1 Overview

ARM® core with embedded Flash & RAM

The STR71xF series is a family of ARM-powered 16/32-bit Microcontrollers with embedded Flash and RAM. It combines the high performance ARM7TDMI CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. The STR71xF family has an embedded ARM core and is therefore compatible with all ARM tools and software.

For information on the **ARM Realview Developer Kit for ST** and third-party development tools, please refer to the <http://www.st.com> website

Package Choice: Low Pin-Count 64-pin or Feature-Rich 144-pin TQFP or BGA

The STR71xF family is available in 4 main versions.

The 144-pin versions have the full set of all features including CAN, USB and External Memory Interface.

- **STR710F:** 144-pin BGA or TQFP with CAN, USB and EMI

The three 64-pin versions (BGA or TQFP) do not include External Memory Interface.

- **STR715F:** 64-pin BGA or TQFP without CAN or USB
- **STR711F:** 64-pin BGA or TQFP with USB
- **STR712F:** 64-pin BGA or TQFP with CAN



Optional External Memory (STR710F)

The non-multiplexed 16-bit data/24-bit address bus available on the STR710F (144-pin) supports four 16-Mbyte banks of external memory. Wait states are programmable individually for each bank allowing different memory types (Flash, EPROM, ROM, SRAM etc.) to be used to store programs or data.

Figure 1 shows the general block diagram of the device family.

Flexible Power Management

To minimize power consumption, you can program the STR71xF to switch to SLOW, WAIT FOR INTERRUPT, STOP or STANDBY mode depending on the current system activity in the application.

Flexible Clock Control

Two external clock sources can be used, a main clock and a 32 kHz backup clock. The embedded PLL allows the internal system clock (up to 50 MHz) to be generated from a main clock frequency of 16 MHz or less. The PLL output frequency can be programmed using a wide selection of multipliers and dividers.

Voltage Regulators

The STR71xF requires an external 3.0-3.6V power supply. There are two internal Voltage Regulators for generating the 1.8V power supply for the core and peripherals. The main VR is switched off and the Low Power VR switched on when the application puts the STR71xF in Standby or Low Power Wait for Interrupt (LPWFI) mode.

Low Voltage Detectors

Each voltage regulator has an embedded LVD that monitors the internal 1.8V supply. If the voltage drops below a certain threshold, the LVD will reset the STR71xF.

On-Chip Peripherals

CAN Interface (STR710F and STR712F)

The CAN module is compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud.

USB Interface (STR710F and STR711F)

The full-speed USB interface is USB V2.0 compliant and provides up to 8 bidirectional/16 unidirectional endpoints, up to 12 Mb/s (full-speed), support for bulk transfer and USB Suspend/Resume functions.

Standard Timers

Each of the four timers have a 16-bit free-running counter with 7-bit prescaler, up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency.

Realtime Clock (RTC)

The RTC provides a set of continuously running counters driven by a low power 32kHz internal oscillator. The RTC can be used as a general timebase or clock/calendar/alarm function. When the STR71xF is in Standby mode the RTC can be kept running, powered by the low power voltage regulator and driven by the 32kHz internal oscillator.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 625 kb/s.

Smart Card Interface

UART1 is configurable to function either as a general purpose UART or as an asynchronous Smart Card interface as defined by ISO 7816-3. It includes Smart Card clock generation and provides support features for synchronous cards.

Buffered Serial Peripheral Interfaces (BSPI)

Each of the two SPIs allow full duplex, synchronous communications with external devices, master or slave communication at up to 5.5Mb/s in Master mode and 4 Mb/s in Slave mode.

I²C Interfaces

The two I²C Interfaces provide multi-master and slave functions, support normal and fast I²C mode (400 kHz) and 7 or 10-bit addressing modes.

One I²C Interface is multiplexed with one SPI, so either 2xSPI+1x I²C or 1xSPI+2x I²C may be used at a time.

HDLC interface

The High Level Data Link Controller (HDLC) unit supports full duplex operation and NRZ, NRZI, FM0 or MANCHESTER protocols. It has an internal 8-bit baud rate generator.

A/D Converter

The Analog to Digital Converter, converts in single channel or up to 4 channels in single-shot or continuous conversion modes. Resolution is 12-bit with a sample rate of 0.5 kHz (1 kHz in single channel mode). The input voltage range is 0-2.5V.

Watchdog

The 16-bit Watchdog Timer protects the application against hardware or software failures and ensures recovery by generating a reset.

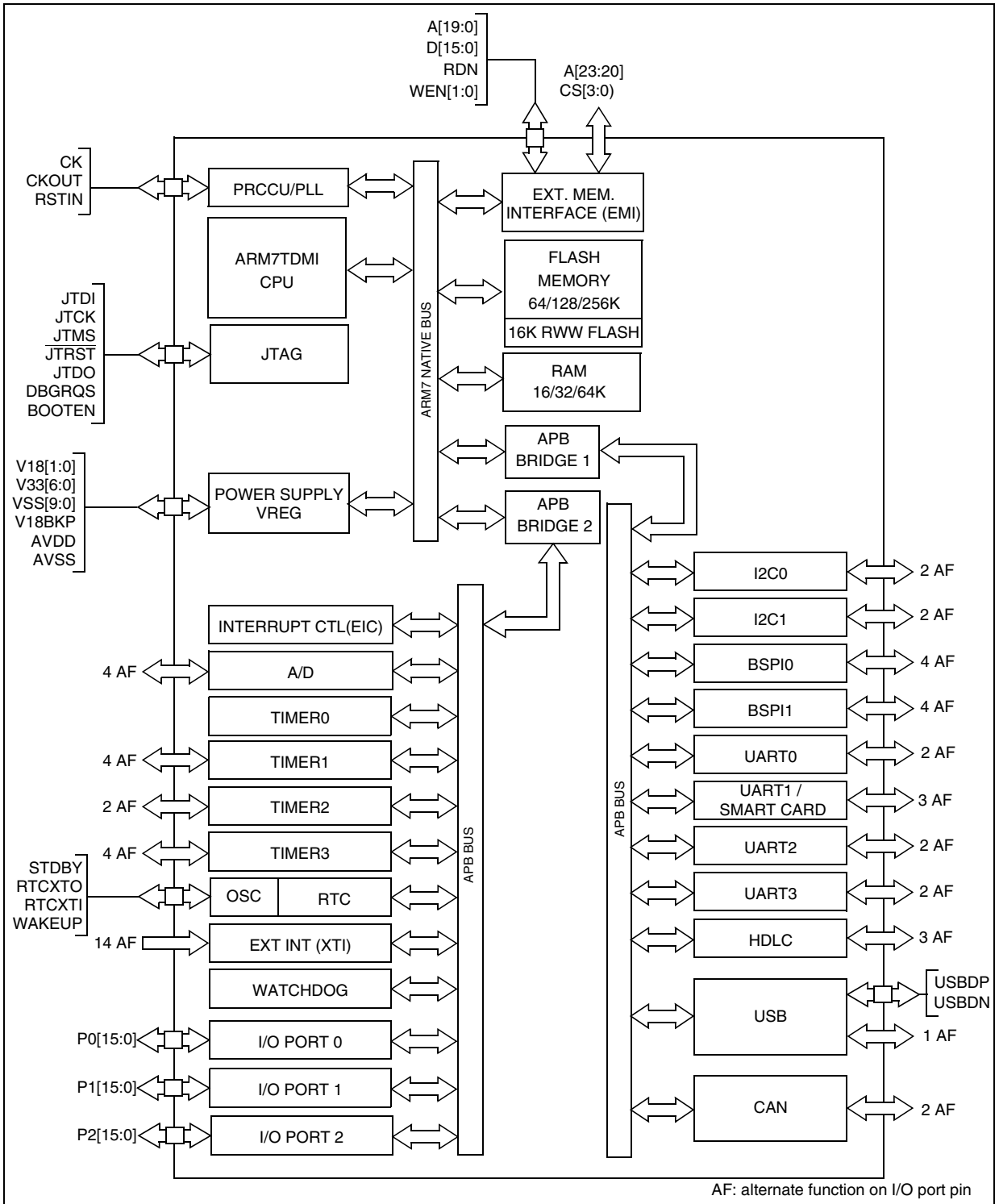
I/O Ports

The 48 I/O ports are programmable as Inputs or Outputs.

External Interrupts

Up to 14 external interrupts are available for application use or to wake-up the application from STOP mode.

Figure 1. STR71xF Block Diagram



1.2 Related Documentation

Available from www.arm.com:

ARM7TDMI Technical Reference Manual

Available from <http://www.st.com>:

STR71x Reference Manual

STR7 Flash Programming Reference Manual

AN1774 - Getting Started with STR71xF Software development

AN1775 - Getting Started with STR71xF Hardware development

AN1776 - STR71xF Enhanced Interrupt Controller

AN1777 - STR71xF Memory Mapping

AN1778 - STR71xF Multi-ICE Setup

AN1780 - Real Time Clock with STR71xF

AN1781 - Four 7 Segment Display Drive Using the STR71xF

The above is a selected list only, a full list STR71x application notes can be viewed at <http://www.st.com>.

1.3 Pin Description for 144-Pin Packages

Figure 2. STR710 TQFP Pinout

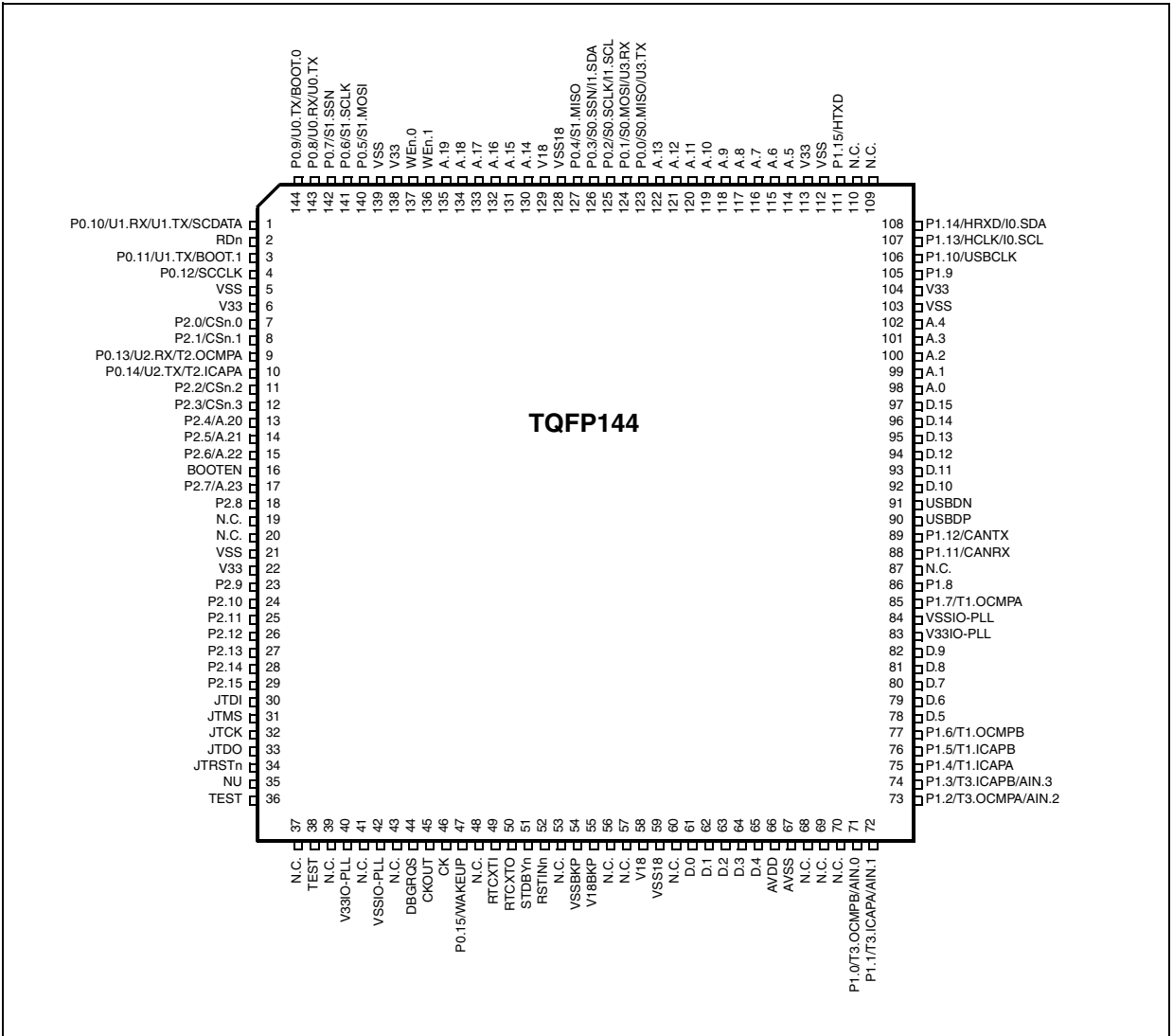


Table 2. STR710 BGA Ball Connections

| | A | B | C | D | E | F | G | H | J | K | L | M |
|-----------|----------|----------|----------|----------|----------|----------|-----------------|-----------------|-------------|----------|---------------|------------|
| 1 | P0.10 | P2.0 | P2.1 | VSS | P2.2 | P2.6 | BOOT EN | P2.12 | P2.13 | P2.15 | JTDI | N.C. |
| 2 | VSS | RDn | P0.11 | V33 | P2.3 | P2.8 | P2.9 | JTMS | JTRSTn | TEST | TEST | N.C. |
| 3 | V33 | P0.9 | P0.12 | P0.13 | P2.4 | VSS | P2.10 | JTCK | NU | V33 | N.C. | DBG RQS |
| 4 | P0.6 | P0.7 | P0.8 | P0.14 | P2.5 | N.C. | P2.11 | JTDO | CK | CKOUT | VSSIO- PLL | N.C. |
| 5 | A.19 | WEn.1 | WEn.0 | P0.5 | P2.7 | N.C. | P2.14 | nc | RTCX- TO | RTCXTI | nc | P0.15 |
| 6 | P0.3 | A.15 | A.16 | A.17 | A.18 | V33 | V18 | N.C. | N.C. | V18BKP | VSS BKP | STDBYn |
| 7 | P0.2 | P0.1 | P0.4 | VSS18 | V18 | A.14 | D.12 | D.1 | D.0 | nc | VSS18 | RSTINn |
| 8 | A.9 | A.10 | A.11 | A.13 | P0.0 | A.0 | D.11 | P1.12/ CANTX | N.C. | AVSS | D.3 | D.2 |
| 9 | VSS | V33 | A.5 | A.6 | V33 | D.15 | D.10 | P1.8 | D.9 | P1.0 | N.C. | N.C. |
| 10 | A.8 | N.C. | P1.15 | P1.13 | VSS | D.14 | USBDN | P1.7 | D.8 | P1.5 | P1.1 | D.4 |
| 11 | A.7 | N.C. | P1.14 | P1.10 | A.2 | D.13 | USBDP | VSS | D.5 | P1.4 | P1.3 | AVDD |
| 12 | A.12 | A.4 | A.3 | P1.9 | A.1 | N.C. | P1.11/ CANRX | V33IO- PLL | P1.6 | D.7 | D.6 | P1.2 |

Legend / Abbreviations for Table 3:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS 0.3V_{DD}/0.7V_{DD},

C_T= CMOS 0.8V / 2V with input trigger

T_T= TTL 0.3V_{DD}/0.7V_{DD} with input trigger

C/T = Programmable levels: CMOS 0.3V_{DD}/0.7V_{DD} or TTL 0.8V / 2V

Port and control configuration:

- Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.
- Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5V tolerant.

Table 3. STR710 Pin Description

| Pin n° | | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|---------|--------|-----------------------------------|------|---------------------------------|----------------|-----------|------------|----|----|-----------------|-----------------------------|--|---------------------------------|
| TQFP144 | BGA144 | | | | Input Level | interrupt | Capability | OD | PP | | | Port | |
| 1 | A1 | P0.10/U1.RX/ U1.TX/ SC.DATA | I/O | pd | C _T | X | 4mA | T | | | Port 0.10 | UART1: Receive Data input | UART1: Transmit data output. |
| | | | | | | | | | | | | Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress | |
| 2 | B2 | \overline{RD} | O | | | | | | X | | | External Memory Interface: Active low read signal for external memory. It maps to the OE_N input of the external components. | |
| 3 | C2 | P0.11/ BOOT.1/ U1.TX | I/O | pd | C _T | | 4mA | X | X | | Port 0.11 | Select Boot Configuration input | UART1: Transmit data output. |
| 4 | C3 | P0.12/SC.CLK | I/O | pd | C _T | | 4mA | | | | Port 0.12 | Smartcard reference clock output | |
| 5 | D1 | V _{SS} | S | | | | | | | | | Ground voltage for digital I/Os | |
| 6 | D2 | V ₃₃ | S | | | | | | | | | Supply voltage for digital I/Os | |
| 7 | B1 | P2.0/ $\overline{CS.0}$ | I/O | pu | C _T | | 8mA | X | X | | Port 2.0 | External Memory Interface: Select Memory Bank 0 output Note: This pin is forced to output mode at reset to allow boot from external memory | |
| 8 | C1 | P2.1/ $\overline{CS.1}$ | I/O | pu ₂₎ | C _T | | 8mA | X | X | | Port 2.1 | External Memory Interface: Select Memory Bank 1 output | |
| 9 | D3 | P0.13/U2.RX/ T2.OCMPA | I/O | pu | C _T | X | 4mA | X | X | | Port 0.13 | UART2: Receive Data input | Timer2: Output Compare A output |
| 10 | D4 | P0.14/U2.TX/ T2.ICAPA | I/O | pu | C _T | | 4mA | X | X | | Port 0.14 | UART2: Transmit data output | Timer2: Input Capture A input |
| 11 | E1 | P2.2/ $\overline{CS.2}$ | I/O | pu ₂₎ | C _T | | 8mA | X | X | | Port 2.2 | External Memory Interface: Select Memory Bank 3 output | |

Table 3. STR710 Pin Description

| Pin n° | TQFP144 | BGA144 | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function |
|--------|---------|-------------------------|----------|------------------|---------------------------------|-------------|-----------|------------|----|----|-----------------|-----------------------------|---|
| | | | | | | Input Level | interrupt | Capability | OD | PP | | | |
| 12 | E2 | P2.3/ $\overline{CS.3}$ | I/O | pu ₂₎ | C _T | | | 8mA | X | X | | Port 2.3 | External Memory Interface: Select Memory Bank 4 output |
| 13 | E3 | P2.4/A.20 | I/O | pd ₃₎ | C _T | | | 8mA | X | X | | Port 2.4 | External Memory Interface: address bus |
| 14 | E4 | P2.5/A.21 | I/O | pd ₃₎ | C _T | | | 8mA | X | X | | Port 2.5 | |
| 15 | F1 | P2.6/A.22 | I/O | pd ₃₎ | C _T | | | 8mA | X | X | | Port 2.6 | |
| 16 | G1 | BOOTEN | I | | C _T | | | | | | | | Boot control input. Enables sampling of BOOT[1:0] pins |
| 17 | E5 | P2.7/A.23 | I/O | pd ₃₎ | C _T | | | 8mA | X | X | | Port 2.7 | External Memory Interface: address bus |
| 18 | F2 | P2.8 | I/O | pu | C _T | X | | 4mA | X | X | | Port 2.8 | External interrupt INT2 |
| 19 | F4 | N.C. | | | | | | | | | | | Not connected (not bonded) |
| 20 | F5 | N.C. | | | | | | | | | | | Not connected (not bonded) |
| 21 | F3 | V _{SS} | S | | | | | | | | | | Ground voltage for digital I/Os |
| 22 | F6 | V ₃₃ | S | | | | | | | | | | Supply voltage for digital I/Os |
| 23 | G2 | P2.9 | I/O | pu | C _T | X | | 4mA | X | X | | Port 2.9 | External interrupt INT3 |
| 24 | G3 | P2.10 | I/O | pu | C _T | X | | 4mA | X | X | | Port 2.10 | External interrupt INT4 |
| 25 | G4 | P2.11 | I/O | pu | C _T | X | | 4mA | X | X | | Port 2.11 | External interrupt INT5 |
| 26 | H1 | P2.12 | I/O | pu | C _T | | | 4mA | X | X | | Port 2.12 | |
| 27 | J1 | P2.13 | I/O | pu | C _T | | | 4mA | X | X | | Port 2.13 | |
| 28 | G5 | P2.14 | I/O | pu | C _T | | | 4mA | X | X | | Port 2.14 | |
| 29 | K1 | P2.15 | I/O | pu | C _T | | | 4mA | X | X | | Port 2.15 | |
| 30 | L1 | JTDI | I | | T _T | | | | | | | | JTAG Data input. External pull-up required. |
| 31 | H2 | JTMS | I | | T _T | | | | | | | | JTAG Mode Selection Input. External pull-up required. |
| 32 | H3 | JTCK | I | | C | | | | | | | | JTAG Clock Input. External pull-up or pull-down required. |
| 33 | H4 | JTDO | O | | | | | 8mA | | X | | | JTAG Data output. Note: Reset state = HiZ. |
| 34 | J2 | \overline{JTRST} | I | | T _T | | | | | | | | JTAG Reset Input. External pull-up required. |
| 35 | J3 | NU | | | | | | | | | | | Reserved, must be forced to ground. |
| 36 | K2 | TEST | | | | | | | | | | | Reserved, must be forced to ground. |
| 37 | L3 | N.C. | | | | | | | | | | | Not connected (not bonded) |
| 38 | L2 | TEST | | | | | | | | | | | Reserved, must be forced to ground. |
| 39 | M1 | N.C. | | | | | | | | | | | Not connected (not bonded) |

Table 3. STR710 Pin Description

| Pin n° | | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function |
|---------|--------|---------------------------|------|---------------------------------|----------------|-----------|------------|----|----|-----------------|---|---------------------------------|
| TQFP144 | BGA144 | | | | Input Level | interrupt | Capability | OD | PP | | | |
| 40 | K3 | V _{33IO-PLL} | S | | | | | | | | Supply voltage for digital I/O circuitry and for PLL reference | |
| 41 | M2 | N.C. | | | | | | | | | Not connected (not bonded) | |
| 42 | L4 | V _{SSIO-PLL} | S | | | | | | | | Ground voltage for digital I/O circuitry and for PLL reference | |
| 43 | M4 | N.C. | | | | | | | | | Not connected (not bonded) | |
| 44 | M3 | DBG RQS | I | | C _T | | | | | | Debug Mode request input (active high) | |
| 45 | K4 | CKOUT | O | | | | 8mA | | X | | Clock output (f _{PCLK2}) Note: Enabled by CKDIS register in APB Bridge 2 | |
| 46 | J4 | CK | I | | C | | | | | | Reference clock input | |
| 47 | M5 | P0.15/WAKE-UP | I | pu | T _T | X | 4mA | | | X | Port 0.15 | Wakeup from Standby mode input. |
| 48 | L5 | N.C. | | | | | | | | | Not connected (not bonded) | |
| 49 | K5 | RTCXTI | | | | | | | | | Realtime Clock input and input of 32 kHz oscillator amplifier circuit | |
| 50 | J5 | RTCXTO | | | | | | | | | Output of 32 kHz oscillator amplifier circuit | |
| 51 | M6 | $\overline{\text{STDBY}}$ | I/O | | C _T | | 4mA | X | | X | Input: Hardware Standby mode entry input active low. Caution: External pull-up to V ₃₃ required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. Note: In Standby mode all pins are in high impedance except those marked Active in Stdby | |
| 52 | M7 | $\overline{\text{RSTIN}}$ | I | | C _T | | | | | X | Reset input | |
| 53 | J6 | N.C. | | | | | | | | | Not connected (not bonded) | |
| 54 | L6 | V _{SSBKP} | | | S | | | | | X | Stabilisation for low power voltage regulator. | |
| 55 | K6 | V _{18BKP} | | | S | | | | | X | Stabilisation for low power voltage regulator. Requires external capacitors of at least 1µF between V _{18BKP} and V _{SS18BKP} . See Figure 5 . Note: If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply. | |
| 56 | H5 | N.C. | | | | | | | | | Not connected (not bonded) | |
| 57 | H6 | N.C. | | | | | | | | | Not connected (not bonded) | |
| 58 | G6 | V ₁₈ | S | | | | | | | | Stabilisation for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V ₁₈ and V _{SS18} . See Figure 5 . | |
| 59 | L7 | V _{SS18} | S | | | | | | | | Stabilisation for main voltage regulator. | |
| 60 | K7 | N.C. | | | | | | | | | Not connected (not bonded) | |

Table 3. STR710 Pin Description

| Pin n° | | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|---------|--------|---------------------------------|------|---------------------------------|----------------|-----------|------------|----|----|-----------------|--|--|-------------------------------|
| TQFP144 | BGA144 | | | | Input Level | interrupt | Capability | OD | PP | | | | |
| 61 | J7 | D.0 | I/O | | | | 8mA | | | | External Memory Interface: data bus | | |
| 62 | H7 | D.1 | I/O | | | | 8mA | | | | | | |
| 63 | M8 | D.2 | I/O | | | | 8mA | | | | | | |
| 64 | L8 | D.3 | I/O | | | | 8mA | | | | | | |
| 65 | M10 | D.4 | I/O | | | | 8mA | | | | | | |
| 66 | M11 | V _{DDA} | S | | | | | | | | Supply voltage for A/D Converter | | |
| 67 | K8 | V _{SSA} | S | | | | | | | | Ground voltage for A/D Converter | | |
| 68 | J8 | N.C. | | | | | | | | | Not connected (not bonded) | | |
| 69 | L9 | N.C. | | | | | | | | | Not connected (not bonded) | | |
| 70 | M9 | N.C. | | | | | | | | | Not connected (not bonded) | | |
| 71 | K9 | P1.0/T3.OC-MPB/AIN.0 | I/O | pu | C _T | | 4mA | X | X | | Port 1.0 | Timer 3: Output Compare B | ADC: Analog input 0 |
| 72 | L10 | P1.1/T3.ICA-PA/T3.EXT-CLK/AIN.1 | I/O | pu | C _T | | 4mA | X | X | | Port 1.1 | Timer 3: Input Capture A or External Clock input | ADC: Analog input 1 |
| 73 | M12 | P1.2/T3.OCM-PA/AIN.2 | I/O | pu | C _T | | 4mA | X | X | | Port 1.2 | Timer 3: Output Compare A | ADC: Analog input 2 |
| 74 | L11 | P1.3/T3.ICAPB/AIN.3 | I/O | pu | C _T | | 4mA | X | X | | Port 1.3 | Timer 3: Input Capture B | ADC: Analog input 3 |
| 75 | K11 | P1.4/T1.ICA-PA/T1.EXT-CLK | I/O | pu | C _T | | 4mA | X | X | | Port 1.4 | Timer 1: Input Capture A | Timer 1: External Clock input |
| 76 | K10 | P1.5/T1.ICAPB | I/O | pu | C _T | | 4mA | X | X | | Port 1.5 | Timer 1: Input Capture B | |
| 77 | J12 | P1.6/T1.OC-MPB | I/O | pu | C _T | | 4mA | X | X | | Port 1.6 | Timer 1: Output Compare B | |
| 78 | J11 | D.5 | I/O | | | | 8mA | | | | External Memory Interface: data bus | | |
| 79 | L12 | D.6 | I/O | | | | 8mA | | | | | | |
| 80 | K12 | D.7 | I/O | | | | 8mA | | | | | | |
| 81 | J10 | D.8 | I/O | | | | 8mA | | | | | | |
| 82 | J9 | D.9 | I/O | | | | 8mA | | | | | | |
| 83 | H12 | V _{33IO-PLL} | S | | | | | | | | Supply voltage for digital I/O circuitry and for PLL reference | | |
| 84 | H11 | V _{SSIO-PLL} | S | | | | | | | | Ground voltage for digital I/O circuitry and for PLL reference | | |
| 85 | H10 | P1.7/T1.OCM-PA | I/O | pu | C _T | | 4mA | X | X | | Port 1.7 | Timer 1: Output Compare A | |
| 86 | H9 | P1.8 | I/O | pd | C _T | | 4mA | X | X | | Port 1.8 | | |
| 87 | F12 | N.C. | | | | | | | | | Not connected (not bonded) | | |

Table 3. STR710 Pin Description

| Pin n° | | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|---------|--------|-------------------|------|---------------------------------|----------------|-----------|------------|----|----|-----------------|-----------------------------|--|--|
| TQFP144 | BGA144 | | | | Input Level | interrupt | Capability | OD | PP | | | | |
| 88 | G12 | P1.11/CANRX | I/O | pu | C _T | X | 4mA | X | X | | Port 1.11 | CAN: receive data input Note: On STR710 and STR712 only | |
| 89 | H8 | P1.12/CANTX | I/O | pu | C _T | X | 4mA | X | X | | Port 1.12 | CAN: Transmit data output Note: On STR710 and STR712 only | |
| 90 | G11 | USBDP | I/O | | C _T | | | | | | | USB bidirectional data (data +). Reset state = HiZ Note: On STR710 and STR711 only This pin requires an external pull-up to V ₃₃ to maintain a high level. | |
| 91 | G10 | USBDN | I/O | | C _T | | | | | | | USB bidirectional data (data -). Reset state = HiZ Note: On STR710 and STR711 only. | |
| 92 | G9 | D.10 | I/O | | | | 8mA | | | | | External Memory Interface: data bus | |
| 93 | G8 | D.11 | I/O | | | | 8mA | | | | | | |
| 94 | G7 | D.12 | I/O | | | | 8mA | | | | | | |
| 95 | F11 | D.13 | I/O | | | | 8mA | | | | | | |
| 96 | F10 | D.14 | I/O | | | | 8mA | | | | | | |
| 97 | F9 | D.15 | I/O | | | | 8mA | | | | | | |
| 98 | F8 | A.0 | O | | | | 8mA | | | | | External Memory Interface: address bus | |
| 99 | E12 | A.1 | O | | | | 8mA | | | | | | |
| 100 | E11 | A.2 | O | | | | 8mA | | | | | | |
| 101 | C12 | A.3 | O | | | | 8mA | | | | | | |
| 102 | B12 | A.4 | O | | | | 8mA | | | | | | |
| 103 | E10 | V _{SS} | S | | | | | | | | | Ground voltage for digital I/O circuitry | |
| 104 | E9 | V ₃₃ | S | | | | | | | | | Supply voltage for digital I/O circuitry | |
| 105 | D12 | P1.9 | I/O | pd | C _T | | 4mA | X | X | | Port 1.9 | | |
| 106 | D11 | P1.10/USB-CLK | I/O | pu | C/T | | 4mA | X | X | | Port 1.10 | USB: 48 MHZ clock input | |
| 107 | D10 | P1.13/HCLC/I0.SCL | I/O | pu | C _T | X | 4mA | X | X | | Port 1.13 | HDLC: reference clock input I2C clock | |
| 108 | C11 | P1.14/HRXD/I0.SDA | I/O | pu | C _T | X | 4mA | X | X | | Port 1.14 | HDLC: Receive data input I2C serial data | |
| 109 | B11 | N.C. | | | | | | | | | | Not connected (not bonded) | |
| 110 | B10 | N.C. | | | | | | | | | | Not connected (not bonded) | |
| 111 | C10 | P1.15/HTXD | I/O | pu | C _T | X | 4mA | X | X | | Port 1.15 | HDLC: Transmit data output | |
| 112 | A9 | V _{SS} | S | | | | | | | | | Ground voltage for digital I/O circuitry | |
| 113 | B9 | V ₃₃ | S | | | | | | | | | Supply voltage for digital I/O circuitry | |

Table 3. STR710 Pin Description

| Pin n° | | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|---------|--------|-----------------------------|------|---------------------------------|----------------|-----------|------------|----|----|-----------------|---|-------------------------------|--|
| TQFP144 | BGA144 | | | | Input Level | interrupt | Capability | OD | PP | | | | |
| | | | | | | | | | | | | | |
| 114 | C9 | A.5 | O | | | | 8mA | | | | External Memory Interface: address bus | | |
| 115 | D9 | A.6 | O | | | | 8mA | | | | | | |
| 116 | A11 | A.7 | O | | | | 8mA | | | | | | |
| 117 | A10 | A.8 | O | | | | 8mA | | | | | | |
| 118 | A8 | A.9 | O | | | | 8mA | | | | | | |
| 119 | B8 | A.10 | O | | | | 8mA | | | | | | |
| 120 | C8 | A.11 | O | | | | 8mA | | | | | | |
| 121 | A12 | A.12 | O | | | | 8mA | | | | | | |
| 122 | D8 | A.13 | O | | | | 8mA | | | | | | |
| 123 | E8 | P0.0/S0.MISO/ U3.TX | I/O | pu | C _T | | 4mA | X | X | Port 0.0 | SPI0 Master in/ Slave out data | UART3 Transmit data output | |
| | | | | | | | | | | | Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register. | | |
| 124 | B7 | P0.1/S0.MOSI/ U3.RX | I/O | pu | C _T | X | 4mA | X | X | Port 0.1 | BSPi0: Master out/Slave in data | UART3: Receive Data input | |
| | | | | | | | | | | | Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register. | | |
| 125 | A7 | P0.2/ S0.SCLK/ I1.SCL | I/O | pu | C _T | X | 4mA | X | X | Port 0.2 | BSPi0: Serial Clock | I2C1: Serial clock | |
| | | | | | | | | | | | Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register. | | |
| 126 | A6 | P0.3/S0.SS/ I1.SDA | I/O | pu | C _T | | 4mA | X | X | Port 0.3 | SPI0: Slave Se- lect input active low. | I2C1: Serial Data | |
| | | | | | | | | | | | Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register. | | |
| 127 | C7 | P0.4/S1.MISO | I/O | pu | C _T | | 4mA | X | X | Port 0.4 | SPI1: Master in/Slave out data | | |
| 128 | D7 | V _{SS18} | S | | | | | | | | Stabilisation for main voltage regulator. | | |
| 129 | E7 | V ₁₈ | S | | | | | | | | Stabilisation for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V ₁₈ and V _{SS18} . See Figure 5 . | | |
| 130 | F7 | A.14 | O | | | | 8mA | | | | External Memory Interface: address bus | | |
| 131 | B6 | A.15 | O | | | | 8mA | | | | | | |
| 132 | C6 | A.16 | O | | | | 8mA | | | | | | |
| 133 | D6 | A.17 | O | | | | 8mA | | | | | | |
| 134 | E6 | A.18 | O | | | | 8mA | | | | | | |
| 135 | A5 | A.19 | O | | | | 8mA | | | | | | |

Table 3. STR710 Pin Description

| Pin n° | | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|---------|--------|--------------------------|------|---------------------------------|----------------|-----------|------------|----|----|-----------------|--|-------------------------------------|------------------------------|
| TQFP144 | BGA144 | | | | Input Level | interrupt | Capability | OD | PP | | | | |
| 136 | B5 | $\overline{WE}.1$ | O | | | | 8mA | | | | External Memory Interface: active low MSB write enable output | | |
| 137 | C5 | $\overline{WE}.0$ | O | | | | 8mA | | | | External Memory Interface: active low LSB write enable output | | |
| 138 | A3 | V ₃₃ | S | | | | | | | | Supply voltage for digital I/Os | | |
| 139 | A2 | V _{SS} | S | | | | | | | | Ground voltage for digital I/Os | | |
| 140 | D5 | P0.5/S1.MOSI | I/O | pu | C _T | | 4mA | X | X | | Port 0.5 | SPI1: Master out/Slave In data | |
| 141 | A4 | P0.6/S1.SCLK | I/O | pu | C _T | X | 4mA | X | X | | Port 0.6 | SPI1: Serial Clock | |
| 142 | B4 | P0.7/S1. \overline{SS} | I/O | pu | C _T | | 4mA | X | X | | Port 0.7 | SPI1: Slave Select input active low | |
| 143 | C4 | P0.8/U0.RX/ U0.TX | I/O | pd | C _T | X | 4mA | T | | | Port 0.8 | UART0: Receive Data input | UART0: Transmit data output. |
| | | | | | | | | | | | Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress | | |
| 144 | B3 | P0.9/U0.TX/ BOOT.0 | I/O | pd | C _T | | 4mA | X | X | | Port 0.9 | Select Boot Configuration input | UART0: Transmit data output |

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to [Table 7, “Port Bit Configuration Table,” on page 26](#). The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset

2. In reset state, these pins configured as Input PU/PD with weak pull-up enabled. They must be configured by software as Alternate Function (see [Table 7, “Port Bit Configuration Table,” on page 26](#)) to be used by the External Memory Interface.

3. In reset state, these pins configured as Input PU/PD with weak pull-down enabled to output Address 0x0000 0000 using the External Memory Interface. To access memory banks greater than 1Mbyte, they need to be configured by software as Alternate Function (see [Table 7, “Port Bit Configuration Table,” on page 26](#)).

1.4 Pin Description for 64-Pin Packages

Figure 3. STR712F/STR715F TQFP64 Pinout

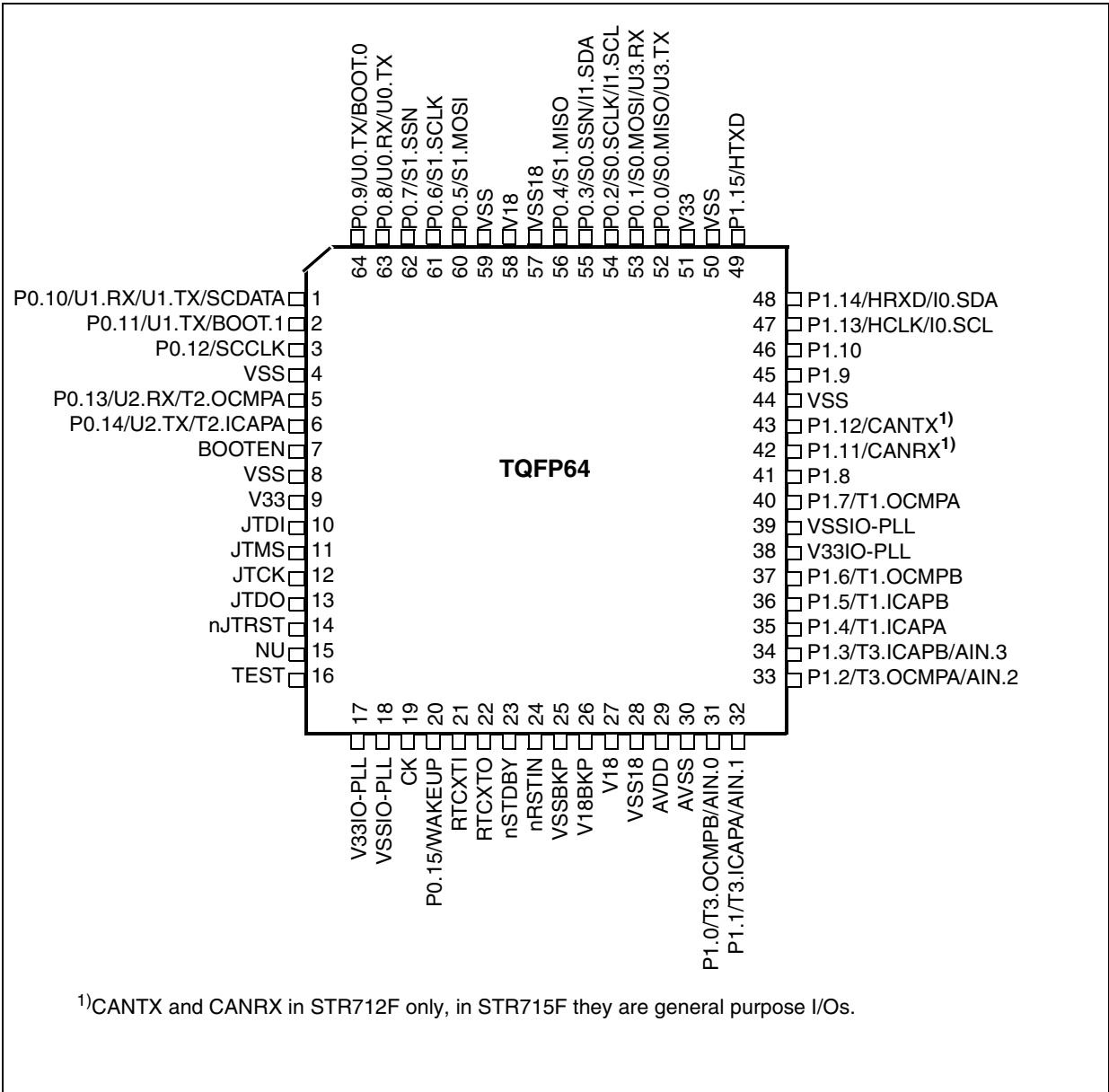


Figure 4. STR711F TQFP64 Pinout

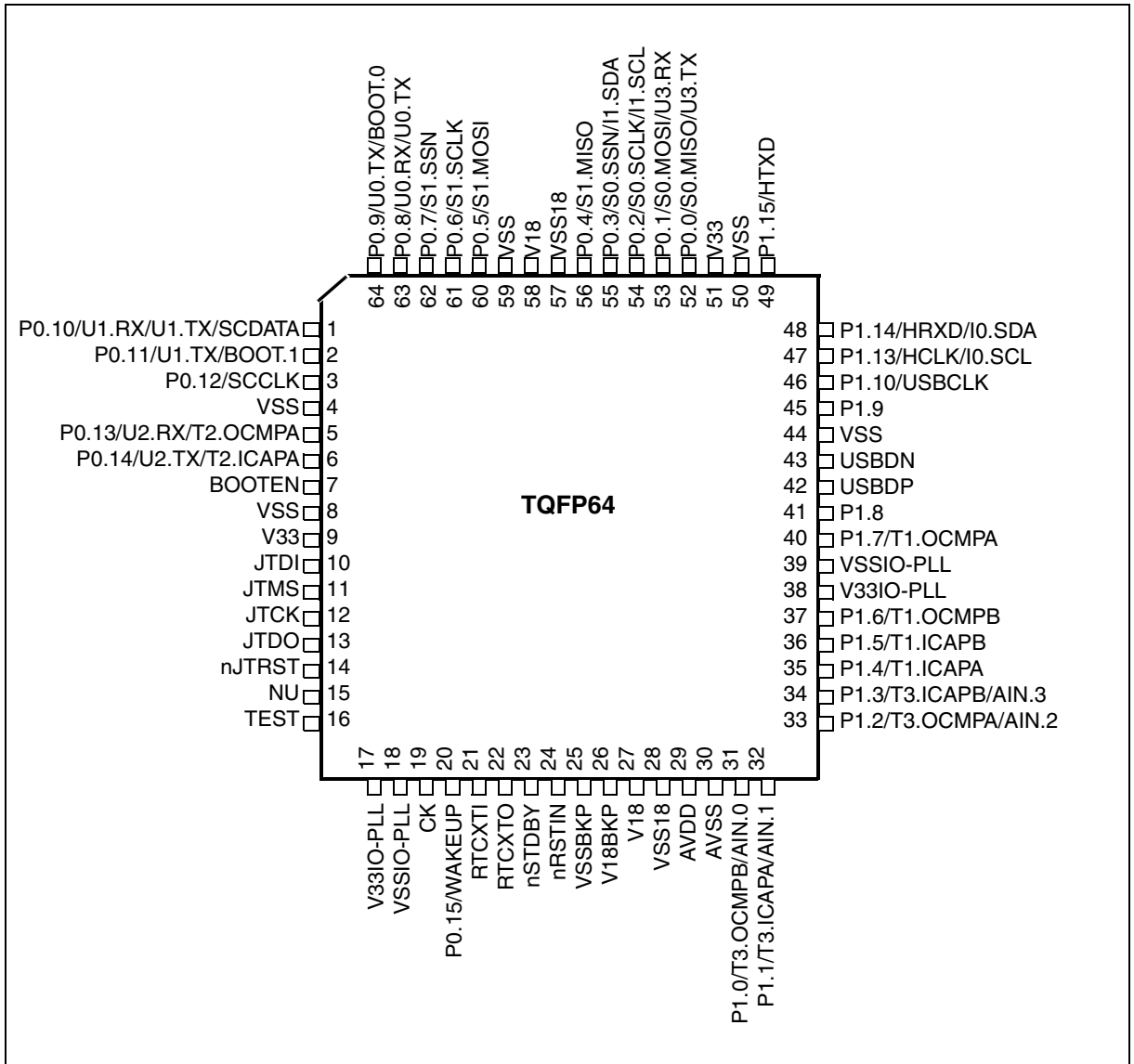


Table 4. STR711F BGA Ball Connections

| | A | B | C | D | E | F | G | H |
|----------|----------|----------|----------|----------|-----------|-----------|----------|-----------|
| 1 | P0.10 | P0.11 | P0.12 | P0.14 | V33 | JTCK | TEST | V33IO-PLL |
| 2 | P0.9 | VSS | P0.13 | VSS | JTMS | JTRSTn | P0.15 | VSSIO-PLL |
| 3 | P0.5 | P0.7 | BOOTEN | JTDI | NU | STDBYn | RTCXTI | CK |
| 4 | VSS18 | VSS | P0.8 | JTDO | AVDD | V18BKP | RSTINn | RTCXTO |
| 5 | P0.2 | P0.4 | V18 | P0.6 | P1.9 | P1.0 | V18 | VSSBKP |
| 6 | V33 | P0.1 | P0.3 | P1.13 | USBDP | VSSIO-PLL | AVSS | VSS18 |
| 7 | VSS | P0.0 | P1.10 | USBDN | P1.7 | P1.6 | P1.5 | P1.1 |
| 8 | P1.15 | P1.14 | VSS | P1.8 | V33IO-PLL | P1.4 | P1.3 | P1.2 |

Table 5. STR712F/715F BGA Ball Connections

| | A | B | C | D | E | F | G | H |
|----------|----------|----------|----------|-------------------------------|-------------------------------|-----------|----------|-----------|
| 1 | P0.10 | P0.11 | P0.12 | P0.14 | V33 | JTCK | TEST | V33IO-PLL |
| 2 | P0.9 | VSS | P0.13 | VSS | JTMS | JTRSTn | P0.15 | VSSIO-PLL |
| 3 | P0.5 | P0.7 | BOOTEN | JTDI | NU | STDBYn | RTCXTI | CK |
| 4 | VSS18 | VSS | P0.8 | JTDO | AVDD | V18BKP | RSTINn | RTCXTO |
| 5 | P0.2 | P0.4 | V18 | P0.6 | P1.9 | P1.0 | V18 | VSSBKP |
| 6 | V33 | P0.1 | P0.3 | P1.13 | P1.11/ CANRX ¹⁾ | VSSIO-PLL | AVSS | VSS18 |
| 7 | VSS | P0.0 | P1.10 | P1.12/ CANTX ¹⁾ | P1.7 | P1.6 | P1.5 | P1.1 |
| 8 | P1.15 | P1.14 | VSS | P1.8 | V33IO-PLL | P1.4 | P1.3 | P1.2 |

¹⁾CANTX and CANRX in STR712F only, in STR715F they are general purpose I/Os.

Legend / Abbreviations for Table 3:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS 0.3V_{DD}/0.7V_{DD},

C_T= CMOS 0.8V / 2V with input trigger

T_T= TTL 0.3V_{DD}/0.7V_{DD} with input trigger

C/T = Programmable levels: CMOS 0.3V_{DD}/0.7V_{DD} or TTL 0.8V / 2V

Port and control configuration:

- Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.
- Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5V tolerant.

Table 6. STR711/STR712/STR715 Pin Description

| Pin n° | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|--------|----------|-----------------------------------|---------------------------------|-------------|----------------|------------|-----|----|-----------------|-----------------------------|--|---------------------------------|
| | | | | Input Level | interrupt | Capability | OD | PP | | | | |
| TQFP64 | BGA64 | | | | | | | | | | | |
| 1 | A1 | P0.10/U1.RX/ U1.TX/ SC.DATA | I/O | pd | C _T | X | 4mA | T | | Port 0.10 | UART1: Receive Data input | UART1: Transmit data output. |
| | | | | | | | | | | | Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress | |
| 2 | B1 | P0.11/ BOOT.1/ U1.TX | I/O | pd | C _T | | 4mA | X | X | Port 0.11 | Select Boot Configuration input | UART1: Transmit data output. |
| 3 | C1 | P0.12/SC.CLK | I/O | pd | C _T | | 4mA | | | Port 0.12 | Smartcard reference clock output | |
| 4 | B2 | V _{SS} | S | | | | | | | | Ground voltage for digital I/Os | |
| 5 | C2 | P0.13/U2.RX/ T2.OCMPA | I/O | pu | C _T | X | 4mA | X | X | Port 0.13 | UART2: Receive Data input | Timer2: Output Compare A output |
| 6 | D1 | P0.14/U2.TX/ T2.ICAPA | I/O | pu | C _T | | 4mA | X | X | Port 0.14 | UART2: Transmit data output | Timer2: Input Capture A input |
| 7 | C3 | BOOTEN | I | | C _T | | | | | | Boot control input. Enables sampling of BOOT[1:0] pins | |
| 8 | D2 | V _{SS} | S | | | | | | | | Ground voltage for digital I/Os | |
| 9 | E1 | V ₃₃ | S | | | | | | | | Supply voltage for digital I/Os | |
| 10 | D3 | JTDI | I | | T _T | | | | | | JTAG Data input. External pull-up required. | |
| 11 | E2 | JTMS | I | | T _T | | | | | | JTAG Mode Selection Input. External pull-up required. | |
| 12 | F1 | JTCK | I | | C | | | | | | JTAG Clock Input. External pull-up or pull-down required. | |
| 13 | D4 | JTDO | O | | | | 8mA | | X | | JTAG Data output. Note: Reset state = HiZ. | |
| 14 | F2 | JTRST | I | | T _T | | | | | | JTAG Reset Input. External pull-up required. | |
| 15 | E3 | NU | | | | | | | | | Reserved, must be forced to ground. | |

Table 6. STR711/STR712/STR715 Pin Description

| Pin n° | | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|--------|-------|---------------------------------|------|---------------------------------|----------------|-----------|------------|----|----|-----------------|---|--|---------------------|
| TQFP64 | BGA64 | | | | Input Level | interrupt | Capability | OD | PP | | | | |
| 16 | G1 | TEST | | | | | | | | | Reserved, must be forced to ground. | | |
| 17 | H1 | V _{33IO-PLL} | S | | | | | | | | Supply voltage for digital I/O circuitry and for PLL reference | | |
| 18 | H2 | V _{SSIO-PLL} | S | | | | | | | | Ground voltage for digital I/O circuitry and for PLL reference | | |
| 19 | H3 | CK | I | | C | | | | | | Reference clock input | | |
| 20 | G2 | P0.15/WAKE-UP | I | pu | T _T | X | 4mA | | | X | Port 0.15 | Wakeup from Standby mode input. | |
| 21 | G3 | RTCXTI | | | | | | | | | Realtime Clock input and input of 32 kHz oscillator amplifier circuit | | |
| 22 | H4 | RTCXTO | | | | | | | | | Output of 32 kHz oscillator amplifier circuit | | |
| 23 | F3 | $\overline{\text{STDBY}}$ | I/O | | C _T | | 4mA | X | | X | <p>Input: Hardware Standby mode entry input active low. Caution: External pull-up to V₃₃ required to select normal mode.</p> <p>Output: Standby mode active low output following Software Standby mode entry.</p> <p>Note: In Standby mode all pins are in high impedance except those marked Active in Stdby</p> | | |
| 24 | G4 | $\overline{\text{RSTIN}}$ | I | | C _T | | | | | X | Reset input | | |
| 25 | H5 | V _{SSBKP} | | | S | | | | | X | Stabilisation for low power voltage regulator. | | |
| 26 | F4 | V _{18BKP} | | | S | | | | | X | <p>Stabilisation for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and V_{SS18BKP}. See Figure 5.</p> <p>Note: If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.</p> | | |
| 27 | G5 | V ₁₈ | S | | | | | | | | <p>Stabilisation for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V₁₈ and V_{SS18}. See Figure 5.</p> | | |
| 28 | H6 | V _{SS18} | S | | | | | | | | Stabilisation for main voltage regulator. | | |
| 29 | E4 | V _{DDA} | S | | | | | | | | Supply voltage for A/D Converter | | |
| 30 | G6 | V _{SSA} | S | | | | | | | | Ground voltage for A/D Converter | | |
| 31 | F5 | P1.0/T3.OC-MPB/AIN.0 | I/O | pu | C _T | | 4mA | X | X | | Port 1.0 | Timer 3: Output Compare B | ADC: Analog input 0 |
| 32 | H7 | P1.1/T3.ICA-PA/T3.EXT-CLK/AIN.1 | I/O | pu | C _T | | 4mA | X | X | | Port 1.1 | Timer 3: Input Capture A or External Clock input | ADC: Analog input 1 |
| 33 | H8 | P1.2/T3.OCM-PA/AIN.2 | I/O | pu | C _T | | 4mA | X | X | | Port 1.2 | Timer 3: Output Compare A | ADC: Analog input 2 |
| 34 | G8 | P1.3/T3.ICAPB/AIN.3 | I/O | pu | C _T | | 4mA | X | X | | Port 1.3 | Timer 3: Input Capture B | ADC: Analog input 3 |

Table 6. STR711/STR712/STR715 Pin Description

| Pin n° | | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|--------|-------|---------------------------|------|---------------------------------|----------------|-----------|------------|----|----|-----------------|--|---|-------------------------------|
| TQFP64 | BGA64 | | | | Input Level | interrupt | Capability | OD | PP | | | | |
| 35 | F8 | P1.4/T1.ICA-PA/T1.EXT-CLK | I/O | pu | C _T | | 4mA | X | X | | Port 1.4 | Timer 1: Input Capture A | Timer 1: External Clock input |
| 36 | G7 | P1.5/T1.ICAPB | I/O | pu | C _T | | 4mA | X | X | | Port 1.5 | Timer 1: Input Capture B | |
| 37 | F7 | P1.6/T1.OC-MPB | I/O | pu | C _T | | 4mA | X | X | | Port 1.6 | Timer 1: Output Compare B | |
| 38 | E8 | V _{33IO} -PLL | S | | | | | | | | | Supply voltage for digital I/O circuitry and for PLL reference | |
| 39 | F6 | V _{SSIO} -PLL | S | | | | | | | | | Ground voltage for digital I/O circuitry and for PLL reference | |
| 40 | E7 | P1.7/T1.OCMPA | I/O | pu | C _T | | 4mA | X | X | | Port 1.7 | Timer 1: Output Compare A | |
| 41 | D8 | P1.8 | I/O | pd | C _T | | 4mA | X | X | | Port 1.8 | | |
| 42 | E6 | P1.11/CANRX | I/O | pu | C _T | X | 4mA | X | X | | Port 1.11 | CAN: receive data input Note: On STR710 and STR712 only | |
| 43 | D7 | P1.12/CANTX | I/O | pu | C _T | X | 4mA | X | X | | Port 1.12 | CAN: Transmit data output Note: On STR710 and STR712 only | |
| 42 | E6 | USBDP | I/O | | C _T | | | | | | USB bidirectional data (data +). Reset state = HiZ Note: On STR710 and STR711 only This pin requires an external pull-up to V ₃₃ to maintain a high level. | | |
| 43 | D7 | USBDN | I/O | | C _T | | | | | | USB bidirectional data (data -). Reset state = HiZ Note: On STR710 and STR711 only. | | |
| 44 | C8 | V _{SS} | S | | | | | | | | Ground voltage for digital I/O circuitry | | |
| 45 | E5 | P1.9 | I/O | pd | C _T | | 4mA | X | X | | Port 1.9 | | |
| 46 | C7 | P1.10/USB-CLK | I/O | pu | C/T | | 4mA | X | X | | Port 1.10 | USB: 48 MHZ clock input | |
| 47 | D6 | P1.13/HCLK/I0.SCL | I/O | pu | C _T | X | 4mA | X | X | | Port 1.13 | HDLC: reference clock input | I2C clock |
| 48 | B8 | P1.14/HRXD/I0.SDA | I/O | pu | C _T | X | 4mA | X | X | | Port 1.14 | HDLC: Receive data input | I2C serial data |
| 49 | A8 | P1.15/HTXD | I/O | pu | C _T | X | 4mA | X | X | | Port 1.15 | HDLC: Transmit data output | |
| 50 | A7 | V _{SS} | S | | | | | | | | Ground voltage for digital I/O circuitry | | |
| 51 | A6 | V ₃₃ | S | | | | | | | | Supply voltage for digital I/O circuitry | | |
| 52 | B7 | P0.0/S0.MISO/U3.TX | I/O | pu | C _T | | 4mA | X | X | | Port 0.0 | SPI0 Master in/ Slave out data | UART3 Transmit data output |
| | | | | | | | | | | | Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register. | | |

Table 6. STR711/STR712/STR715 Pin Description

| Pin n° | | Pin Name | Type | Input Reset State ¹⁾ | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|--------|-------|-----------------------------|------|---------------------------------|----------------|-----------|------------|----|----|-----------------|-----------------------------|---|--|
| TQFP64 | BGA64 | | | | Input Level | interrupt | Capability | OD | PP | | | | |
| 53 | B6 | P0.1/S0.MOSI/ U3.RX | I/O | pu | C _T | X | 4mA | X | X | | Port 0.1 | BSPI0: Master out/Slave in data UART3: Receive Data input Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register. | |
| 54 | A5 | P0.2/ S0.SCLK/ I1.SCL | I/O | pu | C _T | X | 4mA | X | X | | Port 0.2 | BSPI0: Serial Clock I2C1: Serial clock Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register. | |
| 55 | C6 | P0.3/S0.SS/ I1.SDA | I/O | pu | C _T | | 4mA | X | X | | Port 0.3 | SPI0: Slave Select input active low. I2C1: Serial Data Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register. | |
| 56 | B5 | P0.4/S1.MISO | I/O | pu | C _T | | 4mA | X | X | | Port 0.4 | SPI1: Master in/Slave out data | |
| 57 | A4 | V _{SS18} | S | | | | | | | | | Stabilisation for main voltage regulator. | |
| 58 | C5 | V ₁₈ | S | | | | | | | | | Stabilisation for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V ₁₈ and V _{SS18} . See Figure 5 . | |
| 59 | B4 | V _{SS} | S | | | | | | | | | Ground voltage for digital I/Os | |
| 60 | A3 | P0.5/S1.MOSI | I/O | pu | C _T | | 4mA | X | X | | Port 0.5 | SPI1: Master out/Slave In data | |
| 61 | D5 | P0.6/S1.SCLK | I/O | pu | C _T | X | 4mA | X | X | | Port 0.6 | SPI1: Serial Clock | |
| 62 | B3 | P0.7/S1.SS | I/O | pu | C _T | | 4mA | X | X | | Port 0.7 | SPI1: Slave Select input active low | |
| 63 | C4 | P0.8/U0.RX/ U0.TX | I/O | pd | C _T | X | 4mA | T | | | Port 0.8 | UART0: Receive Data input UART0: Transmit data output. Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress | |
| | | | | | | | | | | | Port 0.9 | Select Boot Configuration input UART0: Transmit data output | |
| 64 | A2 | P0.9/U0.TX/ BOOT.0 | I/O | pd | C _T | | 4mA | X | X | | Port 0.9 | Select Boot Configuration input UART0: Transmit data output | |

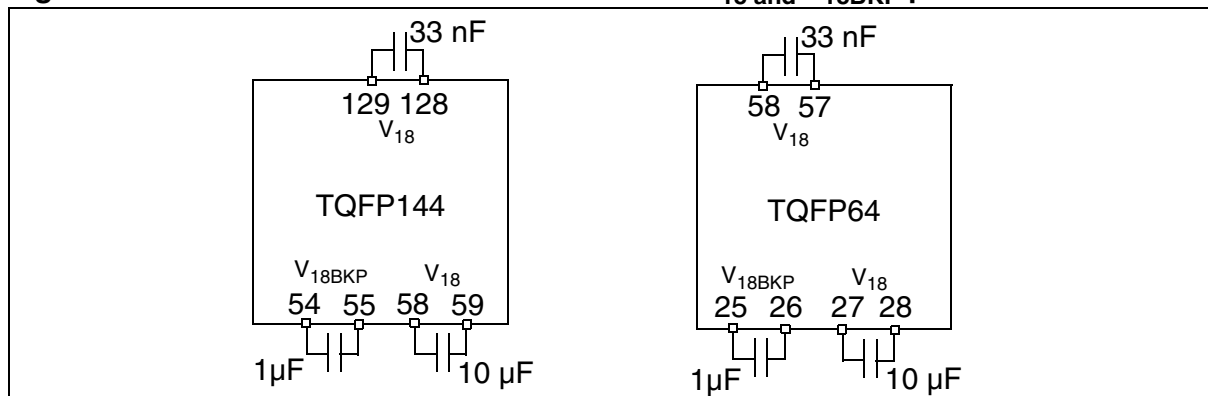
1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to [Table 7, "Port Bit Configuration Table," on page 26](#). The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset

2. In reset state, these pins configured as Input PU/PD with weak pull-up enabled. They must be configured by software as Alternate Function (see [Table 7, "Port Bit Configuration Table," on page 26](#)) to be used by the External Memory Interface.

3. In reset state, these pins configured as Input PU/PD with weak pull-down enabled to output Address 0x0000 0000 using the External Memory Interface. To access memory banks greater than 1Mbyte, they need to be configured by software as Alternate Function (see [Table 7, “Port Bit Configuration Table,”](#) on page 26).

1.5 External Connections

Figure 5. Recommended External Connection of V₁₈ and V_{18BKP} pins



1.6 I/O Port Configuration

Table 7. Port Bit Configuration Table

| Port Configuration Registers (bit) | Values | | | | | | | |
|------------------------------------|---------|-----|------|-------|------|------|------|------|
| | PC0(n) | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| PC1(n) | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| PC2(n) | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| Configuration | HiZ/AIN | IN | IN | IPUPD | OUT | OUT | AF | AF |
| Output | TRI | TRI | TRI | WP | OD | PP | OD | PP |
| Input | AIN | TTL | CMOS | CMOS | N.A. | N.A. | CMOS | CMOS |

Notes:

AF: Alternate Function

AIN: Analog Input

IPUPD: Input Pull Up /Pull Down

CMOS: CMOS Input levels

HiZ: High impedance

IN: Input

N.A. not applicable. In Output mode, a read access to the port gets the output latch value).

OD: Open Drain

OUT: Output

PP: Push-Pull

TRI: Tristate

TTL: TTL Input levels

WP: Weak Push-Pull

1.7 Memory Mapping

Figure 6. Memory Map

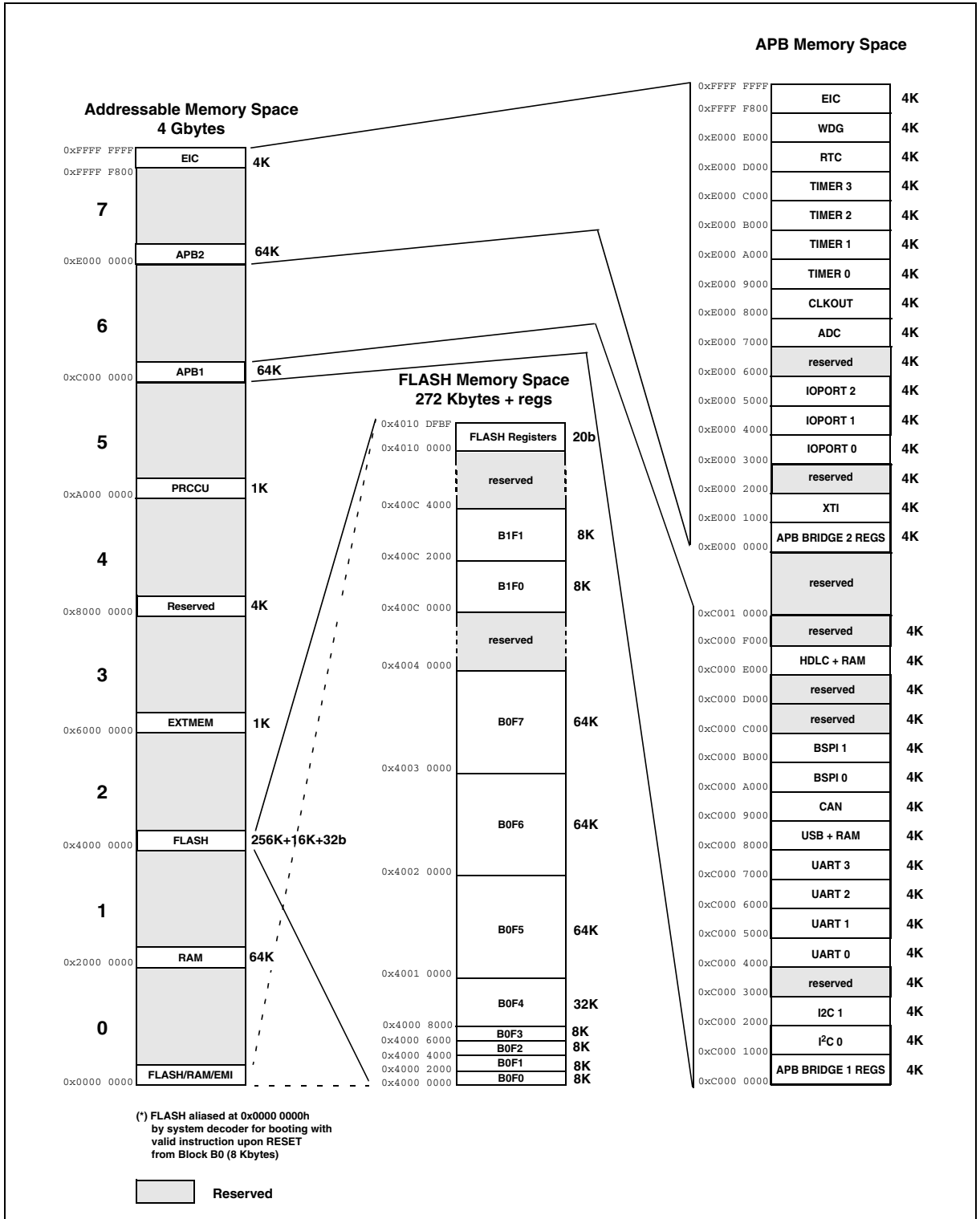


Figure 7. Mapping of Flash Memory Versions

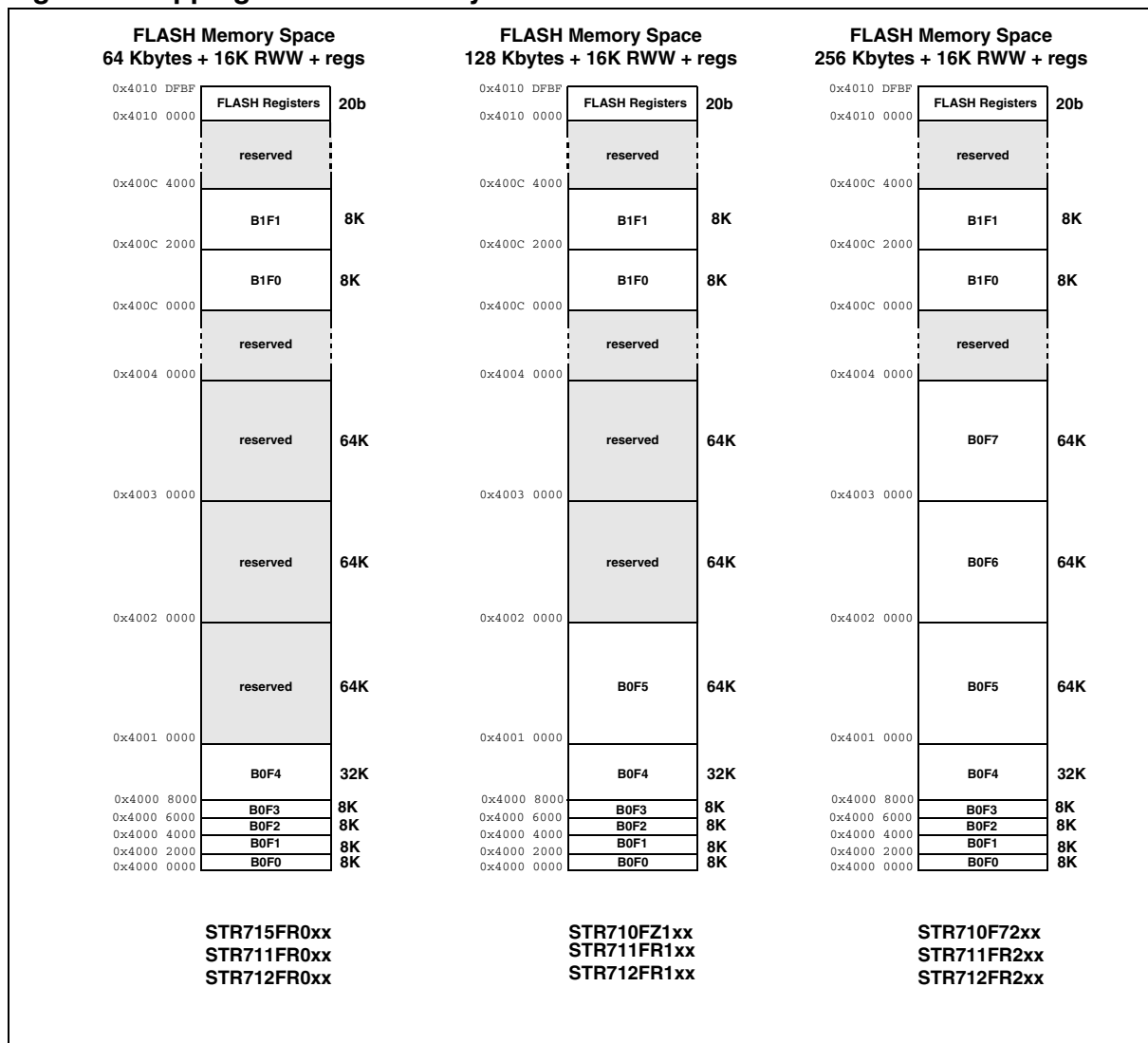
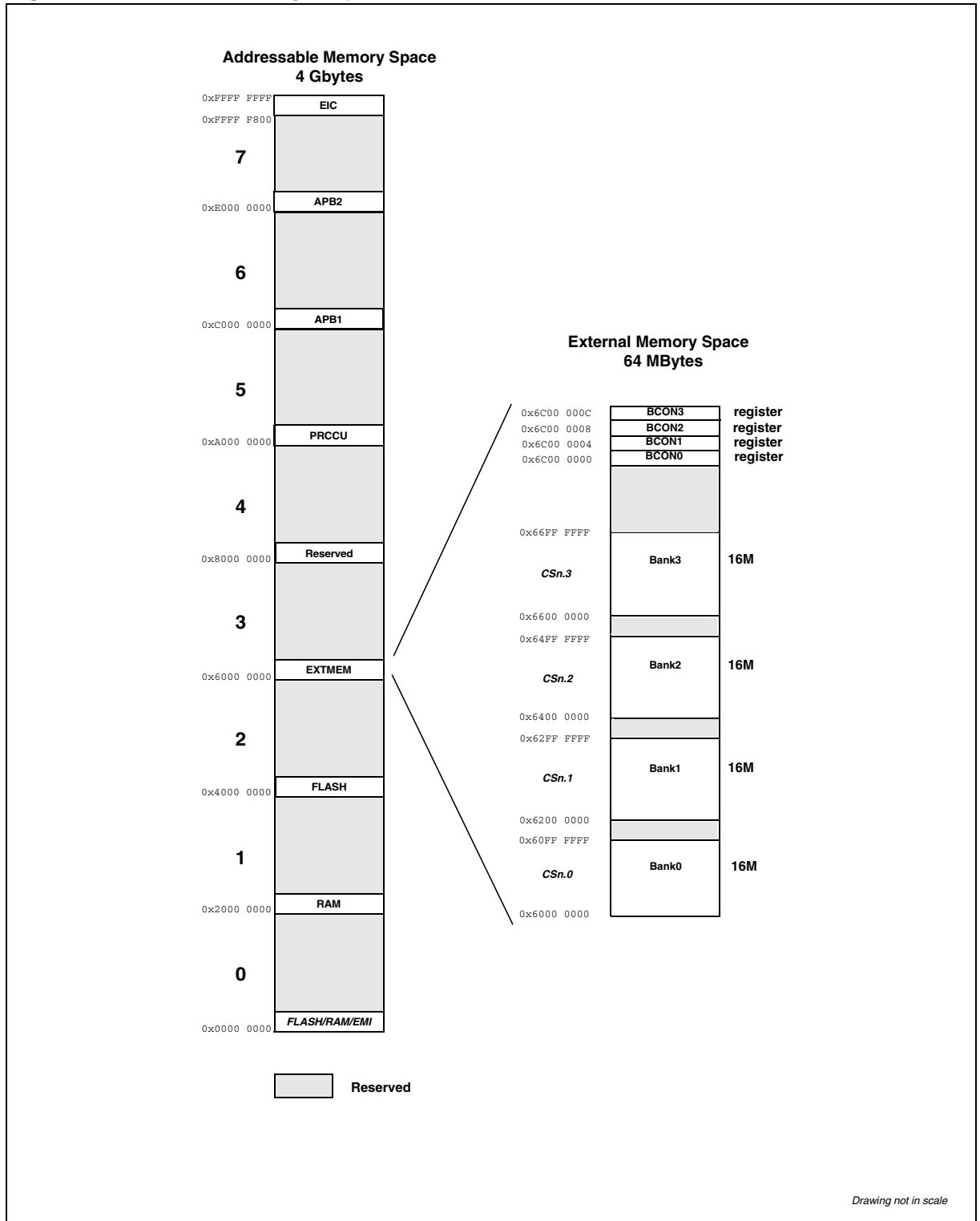


Table 8. RAM Memory Mapping

| Part Number | RAM Size | Start Address | End Address |
|---|-----------|---------------|-------------|
| STR715FR0xx STR711FR0xx STR712FR0xx | 16 Kbytes | 0x2000 0000 | 0x2000 3FFF |
| STR710FZ1xx STR711FR1xx STR712FR1xx | 32 Kbytes | 0x2000 0000 | 0x2000 7FFF |
| STR710F72xx STR711FR2xx STR712FR2xx | 64 Kbytes | 0x2000 0000 | 0x2000 FFFF |

Figure 8. External Memory Map



2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

For proper operation, it is recommended that V_{IN} and V_O be higher than V_{SS} and lower than V_{33} . Reliability is enhanced if unused inputs are connected to an appropriate logic voltage level (V_{33} or V_{SS}).

Table 9. Absolute Maximum Ratings.

| Symbol | Parameter | Value | | Unit |
|----------------|--|-------|----------------|------|
| | | Min | Max | |
| V_{33} | Voltage on V_{33} with respect to ground (V_{SS}) | -0.3 | +4.0 | V |
| $V_{33IO-PLL}$ | Voltage on $V_{33IO-PLL}$ with respect to ground (V_{SS}) | -0.3 | +4.0 | V |
| V_{18} | Voltage on V_{18} with respect to ground (V_{SS}) | -0.3 | +2.0 | V |
| V_{18BKP} | Voltage on V_{18BKP} with respect to ground (V_{SS}) | -0.3 | +2.0 | V |
| AV_{DD} | Voltage on AV_{DD} pin with respect to ground (V_{SS}) | -0.3 | +4.0 | V |
| AV_{SS} | Voltage on AV_{SS} with respect to ground (V_{SS}) | -0.1 | $V_{33} + 0.1$ | V |
| V_{IN} | Voltage on true open drain pin (P0.10) with respect to ground (V_{SS}) | -0.3 | +5.5 | V |
| | Voltage on any other pin with respect to ground (V_{SS}) | -0.3 | +4.0 | |
| I_{OV} | Input current on any pin during overload condition | -10 | +10 | mA |
| I_{TDV} | Absolute sum of all input currents during overload condition | | 200 | mA |
| T_{ST} | Storage Temperature | -55 | +150 | °C |
| ESD | ESD Susceptibility (Human Body Model) | 2000 | | V |

Note Stresses exceeding above listed recommended “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{33}$ or $V_{IN} < V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

2.2 Operating Conditions

| Symbol | Parameter | Value | | Unit |
|-----------------------|--|-----------------|-----------------|------|
| | | Min | Max | |
| V ₃₃ | Digital Supply Voltage for I/O circuitry | 3.0 | 3.6 | V |
| V _{33IO-PLL} | Digital Supply Voltage for I/O circuitry and for PLL reference | 3.0 | 3.6 | V |
| V _{18BKP} | External Supply Voltage for Backup block (Voltage Regulator off) | 1.4 | 1.8 | V |
| AV _{DD} | Analog Supply Voltage for the A/D converter | V ₃₃ | V ₃₃ | V |
| T _A | Ambient temperature under bias | -40 | +85 | °C |
| T _J | Junction temperature under bias | -40 | +105 | °C |

Note RAM data retention is guaranteed with V₃₃ not below 2.7 Volt, with the device in low power mode (Stop or Wait for Interrupt).

2.3 LVD Electrical Characteristics

V₃₃ = 3.3 ± 10%, T_A = -40 / 85 °C unless otherwise specified.

Table 10. LVD Electrical Characteristics

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|-----------------|---------------|------------------|-------|-----|------|------|
| | | | Min | Typ | Max | |
| V _{IT} | LVD Threshold | Main and LP LVDs | | 1.3 | 1.45 | V |

2.4 DC Electrical Characteristics

$V_{33} = 3.3V \pm 10\%$, $T_A = -40 / 85\text{ }^\circ\text{C}$ unless otherwise specified.

Table 11. DC Electrical Characteristics

| Symbol | Parameter | Comment | Value | | | Unit |
|-----------|---|----------------------------------|----------------|-----|-------------|-----------|
| | | | Min | Typ | Max | |
| V_{IH} | Input High Level CMOS | With or w/o hysteresis | $0.7V_{33}$ | | | V |
| | Input High Level | P0.15 (WAKEUP) only | 1.8 | | | V |
| V_{IL} | Input Low Level CMOS | With or w/o hysteresis | | | $0.3V_{33}$ | V |
| | Input Low Level | P0.15 (WAKEUP) only | | | 0.7 | V |
| V_{HYS} | Input Hysteresis CMOS Schmitt Trigger | | 0.4 | 0.8 | 1.2 | V |
| | Input Hysteresis Schmitt Trigger | P0.15 (WAKEUP) only | 0.3 | 0.5 | | V |
| V_{OH} | Output High Level High Current Pins | Push Pull, $I_{OH} = 8\text{mA}$ | $V_{33} - 0.8$ | | | V |
| | Output High Level Standard Current Pins | Push Pull, $I_{OH} = 4\text{mA}$ | $V_{33} - 0.8$ | | | V |
| V_{OL} | Output Low Level High Current Pins | Push Pull, $I_{OL} = 8\text{mA}$ | | | 0.4 | V |
| | Output Low Level Standard Current Pins | Push Pull, $I_{OL} = 4\text{mA}$ | | | 0.4 | V |
| R_{WPU} | Weak Pull-Up Resistor | Measured at $0.5V_{33}$ | | 100 | | $k\Omega$ |
| R_{WPD} | Weak Pull-Down Resistor | Measured at $0.5V_{33}$ | | 100 | | $k\Omega$ |

2.5 AC Electrical Characteristics

$V_{33} = 3.3V \pm 10\%$, $T_A = 27\text{ }^\circ\text{C}$ unless otherwise specified.

Table 12. Power Consumption

| Symbol | Parameter | Conditions | Value | | | Unit |
|-------------|----------------------|------------------------------------|-------|--------------|-----|---------------|
| | | | Min | Typ | Max | |
| I_{DDRUN} | RUN Mode current | MCLK=50 MHz | | See Table 13 | 100 | mA |
| I_{DDWFI} | WFI Mode current | 1 MHz System Clock | | 3 | 6 | mA |
| $I_{DDL P}$ | LPWFI Mode current | 32 kHz System Clock | | 200 | | μA |
| I_{DDSTP} | STOP Mode current | Main VReg off, Flash in Power-Down | | 100 | | μA |
| I_{DDSB1} | STANDBY Mode current | LP VReg and 32kHz Osc on | | 15 | 30 | μA |
| I_{DDSB0} | STANDBY Mode current | LP VReg, LVD, 32kHz Osc bypassed | | 3 | 10 | μA |

Note I_{DDRUN} is the power consumption in applications exploiting the full performances of the core (running at the maximum frequency).

Note I_{DDWFI} is the power consumption with PLLs off, VReg and Flash on. This guarantees the minimum interrupt response time.

Note $I_{DDL P}$ is the power consumption with PLLs, Main VReg and Flash off.

Table 13. I_{DDRUN} Typical Data measurements, $T_A=25^\circ\text{C}$

| Frequency | All Peripheral clocks enabled ¹⁾ (Reset Configuration) | | All Peripheral clocks disabled ¹⁾ | | Unit |
|---------------------------|--|-----------------|--|-----------------|------|
| | RAM Execution | Flash Execution | RAM Execution | Flash Execution | |
| MCLK=1 MHz PCLK=1 MHz | 15 | 15 | 11 | 11 | mA |
| MCLK=8 MHz PCLK=8 MHz | 19 | 20 | 15 | 17 | |
| MCLK=16 MHz PCLK=8 MHz | 23 | 27 | 19 | 23 | |
| MCLK=48 MHz PCLK=6 MHz | 43 | 53 | 40 | 50 | |
| MCLK=64 MHz PCLK=8 MHz | 53 | N/A | 48 | N/A | |

¹⁾Refer to APBn_CKDIS register description.

$V_{33} = 3.3V \pm 10\%$, $T_A = -40 / 85\text{ }^\circ\text{C}$ unless otherwise specified.

Table 14. AC Electrical Characteristics

| Symbol | Parameter | Conditions | Value | | | Unit |
|------------|--------------------------|---------------------------------------|-------|-----|-----|------|
| | | | Min | Typ | Max | |
| f_{MCLK} | CPU Frequency | Executing from RAM or external memory | | | 66 | MHz |
| | | Executing from Flash | | | 50 | |
| | | Executing from Flash with RWW | | | 45 | |
| | | Burst Mode disabled (FLASHLP bit =1) | | | 33 | |
| f_{PCLK} | Peripheral Clock for APB | | | 33 | | |
| f_{CK} | Clock input pin | | | 16 | | |

2.6 nRSTIN Input Filter Characteristics

$V_{33} = 3.3V \pm 10\%$, $T_A = -40 / 85\text{ }^\circ\text{C}$ unless otherwise specified.

Table 15. nRSTIN input Filter Characteristics

| Symbol | Parameter | Conditions | Value | | | Unit |
|-----------|---------------------------------|------------|-------|-----|-----|---------------|
| | | | Min | Typ | Max | |
| t_{FR} | nRSTIN Input Filtered Pulse | | | | 500 | ns |
| t_{NFR} | nRSTIN Input Not Filtered Pulse | | 1.2 | | | μs |

2.7 Oscillator Electrical Characteristics

$V_{33} = 3.3 \pm 10\%$, $T_A = -40 / 85 \text{ }^\circ\text{C}$ unless otherwise specified.

Figure 9. Crystal Oscillator and Resonator

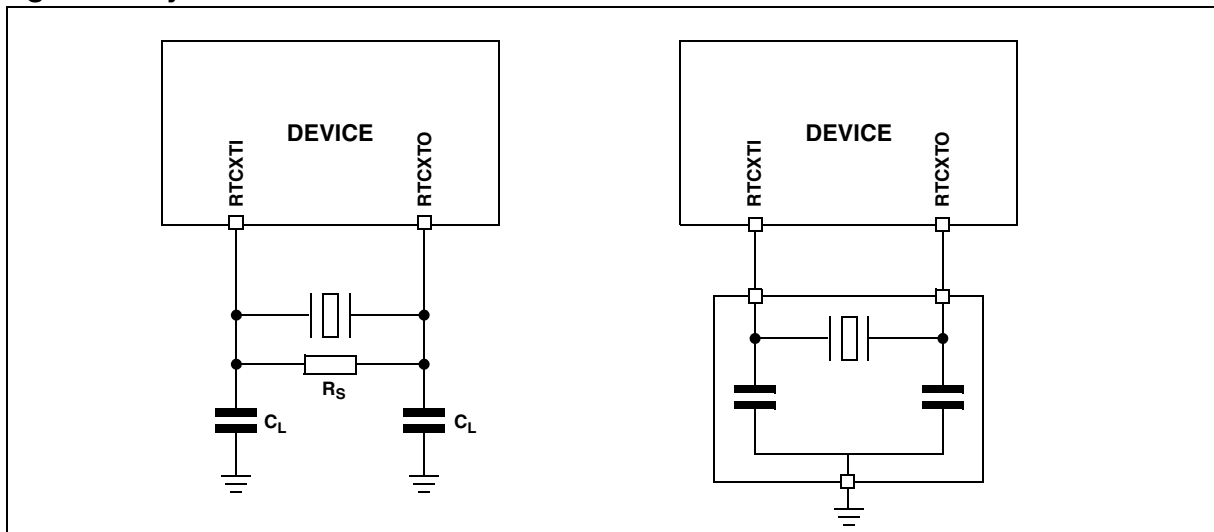


Table 16. Oscillator Electrical Characteristics

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|-------------------|-----------------------------|-----------------|-------|-----|-----|-----------------|
| | | | Min | Typ | Max | |
| g_m | Oscillator Transconductance | | | 8 | | $\mu\text{A/V}$ |
| t_{STUP} | Oscillator Start-up Time | Stable V_{33} | | | 2.5 | s |

2.8 PLL Electrical Characteristics

$V_{33} = 3.3 \pm 10\%$, $V_{33\text{IOPLL}} = 3.3 \pm 10\%$, $T_A = -40 / 85 \text{ }^\circ\text{C}$ unless otherwise specified.

Table 17. PLL1 Electrical Characteristics

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|----------------------|----------------------------|--|-------|-----|------|------|
| | | | Min | Typ | Max | |
| f_{PLLCLK1} | PLL output clock | $f_{\text{PLL1}} \times 24$ | | | 165 | MHz |
| f_{PLL1} | PLL input clock | FREF_RANGE = 0 | 1.5 | | 3.0 | MHz |
| | | FREF_RANGE = 1 MX[1:0]='00' or '01' | 3.0 | | 8.25 | MHz |
| | | FREF_RANGE = 1 MX[1:0]='10' or '11' | 3.0 | | 6 | MHz |
| | PLL input clock duty cycle | | 25 | | 75 | % |

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|-----------------------|----------------------------|---|-------|-----|-----|------|
| | | | Min | Typ | Max | |
| f _{FREE1} | PLL free running frequency | FREF_RANGE = 0 MX[1:0]='01' or '11' | | 1 | | MHz |
| | | FREF_RANGE = 0 MX[1:0]='00' or '10' | | 2 | | MHz |
| | | FREF_RANGE = 1 MX[1:0]='01' or '11' | | 2 | | MHz |
| | | FREF_RANGE = 1 MX[1:0]='00' or '10' | | 4 | | MHz |
| t _{LOCK1} | PLL lock time | FREF_RANGE = 0 Stable Input Clock Stable V _{33IOPLL} , V ₁₈ | | | 300 | μs |
| | | FREF_RANGE = 1 Stable Input Clock Stable V _{33IOPLL} , V ₁₈ | | | 600 | μs |
| Δt _{JITTER1} | PLL jitter (peak to peak) | t _{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz) | | 0.7 | 2 | ns |

Table 18. PLL2 Electrical Characteristics

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|-----------------------|---------------------------|---|-------|-----|-----|------|
| | | | Min | Typ | Max | |
| f _{PLLCLK2} | PLL output clock | f _{PLL} x 28 | | | 140 | MHz |
| f _{PLL2} | PLL input clock | FREF_RANGE = 0 | 1.5 | | 3.0 | MHz |
| | | FREF_RANGE = 1 | 3.0 | | 5 | MHz |
| t _{LOCK2} | PLL lock time | FREF_RANGE = 0 Stable Input Clock Stable V _{33IOPLL} , V ₁₈ | | | 300 | μs |
| | | FREF_RANGE = 1 Stable Input Clock Stable V _{33IOPLL} , V ₁₈ | | | 600 | μs |
| Δt _{JITTER2} | PLL jitter (peak to peak) | t _{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz) | | 0.7 | 2 | ns |

2.9 Flash Electrical characteristics

$V_{33} = 3.3 \pm 10\%$, $T_A = -40 / 85 \text{ }^\circ\text{C}$ unless otherwise specified.

Table 19. Flash Program/Erase Characteristics 1

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|-----------|--------------------------|---------------------|-------|--------------|------------------|---------------|
| | | | Typ | Max(C_0) | Max(C_{max}) | |
| t_{PW} | Word Program | | 40 | | | μs |
| t_{PDW} | Double Word Program | | 60 | | | μs |
| t_{PB0} | Bank 0 Program (256K) | Double Word Program | 1.6 | 2.1 | 4.3 | s |
| t_{PB1} | Bank 1 Program (16K) | Double Word Program | 130 | 170 | 300 | ms |
| t_{ES} | Sector Erase (64K) | Not preprogrammed | 2.3 | 4.0 | 4.9 | s |
| | | Preprogrammed | 1.9 | 3.3 | 4.1 | |
| t_{ES} | Sector Erase (8K) | Not preprogrammed | 0.7 | 1.1 | 1.36 | s |
| | | Preprogrammed | 0.6 | 1.0 | 1.26 | |
| t_{ES} | Bank 0 Erase (256K) | Not preprogrammed | 8.0 | 13.7 | 17.2 | s |
| | | Preprogrammed | 6.6 | 11.2 | 14.0 | |
| t_{ES} | Bank 1 Erase (16K) | Not preprogrammed | 0.9 | 1.5 | 1.87 | s |
| | | Preprogrammed | 0.8 | 1.3 | 1.66 | |
| t_{RPD} | Recovery from Power-Down | | | | 20 | μs |
| t_{PSL} | Program Suspend Latency | | | | 10 | μs |
| t_{ESL} | Erase Suspend Latency | | | | 300 | μs |

Note C_0 : $T_A = 85 \text{ }^\circ\text{C}$ after 0 cycles

C_{max} : $T_A = 85 \text{ }^\circ\text{C}$ after max number of cycles

Table 20. Flash Program/Erase Characteristics 2

| Symbol | Parameter | Conditions | Value | | | Unit |
|-----------|---------------------------|--|-------|-----|-----|---------|
| | | | Min | Typ | Max | |
| | Endurance | | 10 | | | kcycles |
| | Endurance (Bank1 sectors) | | 100 | | | kcycles |
| | Data Retention | | 20 | | | Years |
| t_{ESR} | Erase Suspend Rate | Min time from Erase Resume to next Erase Suspend | 20 | | | ms |

2.10 External Memory Bus Timing

$V_{33} = 3.3 \pm 10\%$, $T_A = -40 / 85 \text{ }^\circ\text{C}$ unless otherwise specified.

The tables below use a variable which is derived from the EMI_BCONn registers (described in the STR71x Reference Manual) and represents the special characteristics of the programmed memory cycle.

| Symbol | Parameter | Value |
|-------------------|-------------------------------|---|
| t_{MCLK} | CPU clock period | $1 / f_{\text{MCLK}}$ |
| t_{C} | Memory cycle time wait states | $t_{\text{MCLK}} \times (1 + [\text{C_LENGTH}])$ |

Table 21. EMI Read Operation

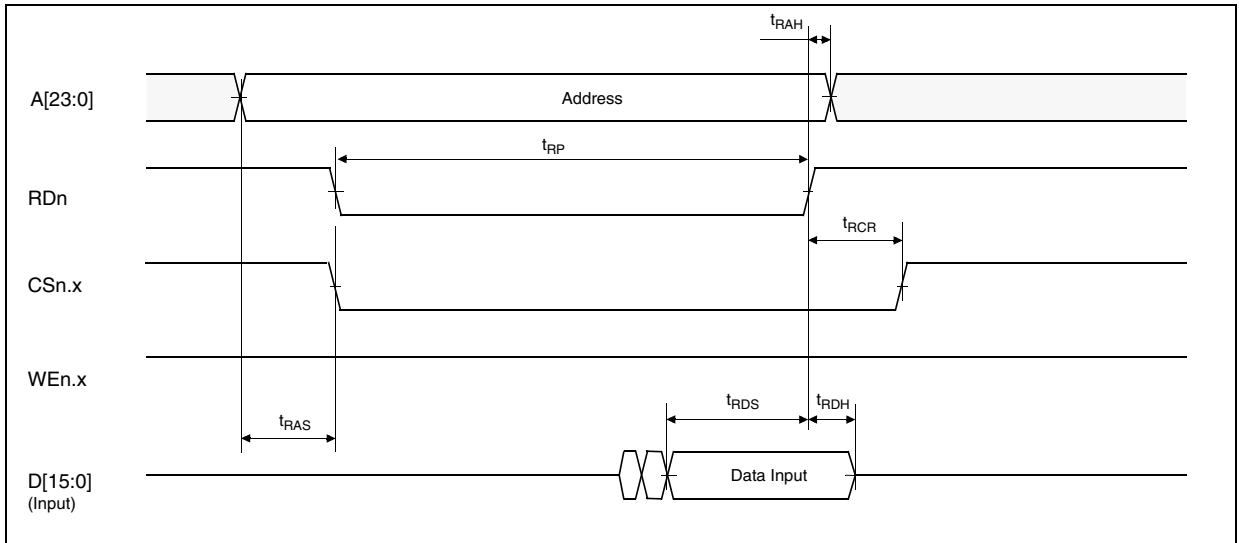
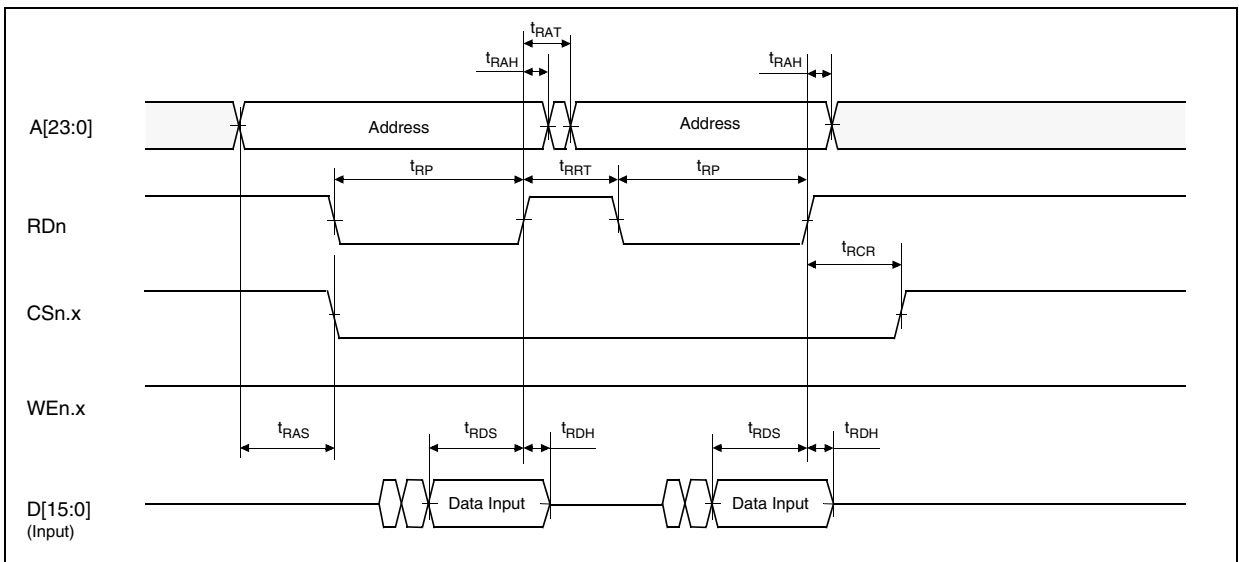
| Symbol | Parameter | Test Conditions | Value | | | Unit |
|------------------|------------------------------|-----------------|-------|-----------------------------|-----|------|
| | | | Min | Typ | Max | |
| t_{RCR} | Read to CSn Removal Time | | | t_{MCLK} | | ns |
| t_{RP} | Read Pulse Time | | | t_{C} | | ns |
| t_{RDS} | Read Data Setup Time | | | 3 | | ns |
| t_{RDH} | Read Data Hold Time | | | 3 | | ns |
| t_{RAS} | Read Address Setup Time | | | $1.3 \cdot t_{\text{MCLK}}$ | | ns |
| t_{RAH} | Read Address Hold Time | | | 3 | | ns |
| t_{RAT} | Read Address Turnaround Time | | | 3 | | ns |
| t_{RRT} | RDn Turnaround Time | | | t_{MCLK} | | ns |

See [Figure 10](#), [Figure 11](#), [Figure 12](#) and [Figure 13](#) for related timing diagrams.

Table 22. EMI Write Operation

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|------------------|-------------------------------|-----------------|-------|-----------------------------|-----|------|
| | | | Min | Typ | Max | |
| t_{WCR} | WEn to CSn Removal Time | | | t_{MCLK} | | ns |
| t_{WP} | Write Pulse Time | | | t_{C} | | ns |
| t_{WDS} | Write Data Setup Time | | | 3 | | ns |
| t_{WDH} | Write Data Hold Time | | | 3 | | ns |
| t_{WAS} | Write Address Setup Time | | | $1.3 \cdot t_{\text{MCLK}}$ | | ns |
| t_{WAH} | Write Address Hold Time | | | 3 | | ns |
| t_{WAT} | Write Address Turnaround Time | | | 3 | | ns |
| t_{WWT} | WEn Turnaround Time | | | t_{MCLK} | | ns |

See [Figure 14](#), [Figure 15](#), [Figure 16](#) and [Figure 17](#) for related timing diagrams.

Figure 10. Read Cycle Timing: 16-bit READ on 16-bit Memory**Figure 11. Read Cycle Timing: 32-bit READ on 16-bit Memory**

See [Table 21](#) for read timing data.

Figure 12. Read Cycle Timing: 16-bit READ on 8-bit Memory

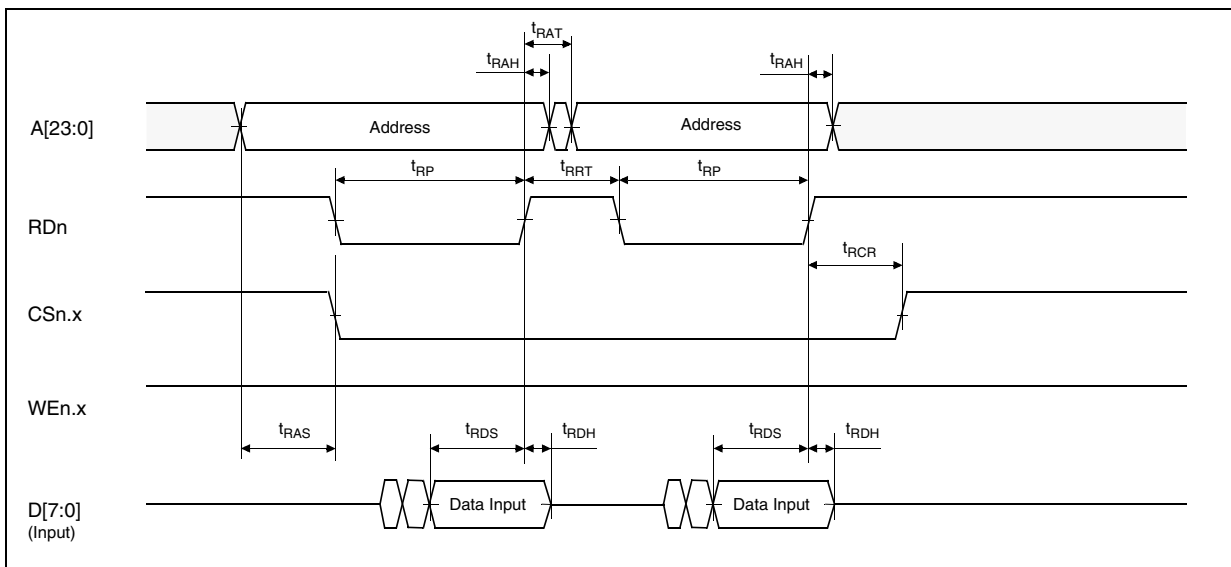
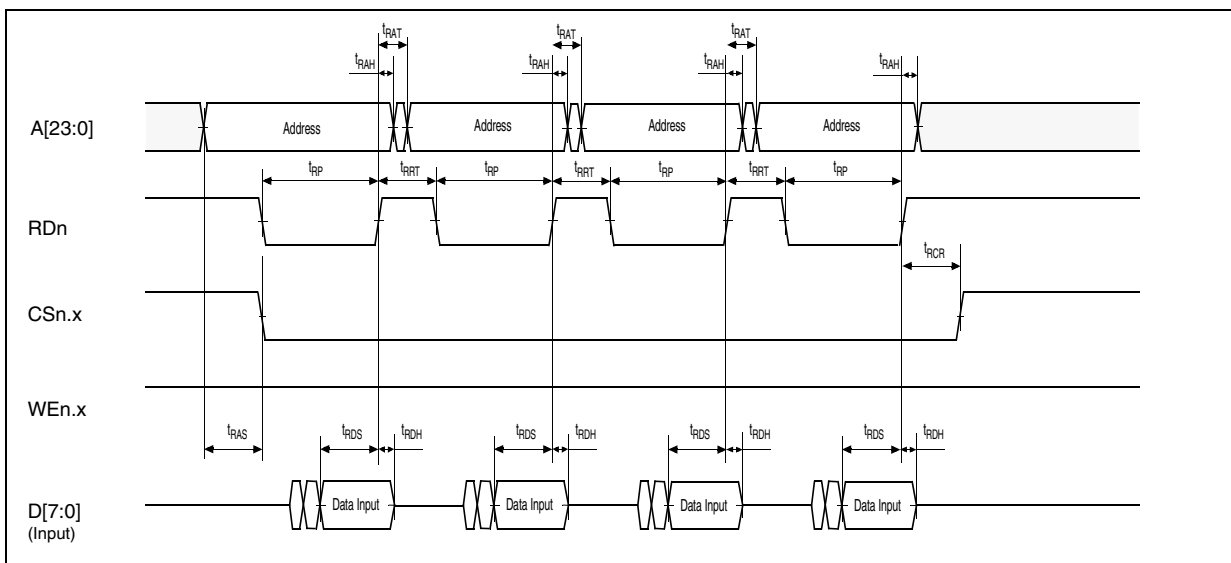


Figure 13. Read Cycle Timing: 32-bit READ on 8-bit Memory



See [Table 21](#) for read timing data.

Figure 14. Write Cycle Timing: 16-bit WRITE on 16-bit Memory

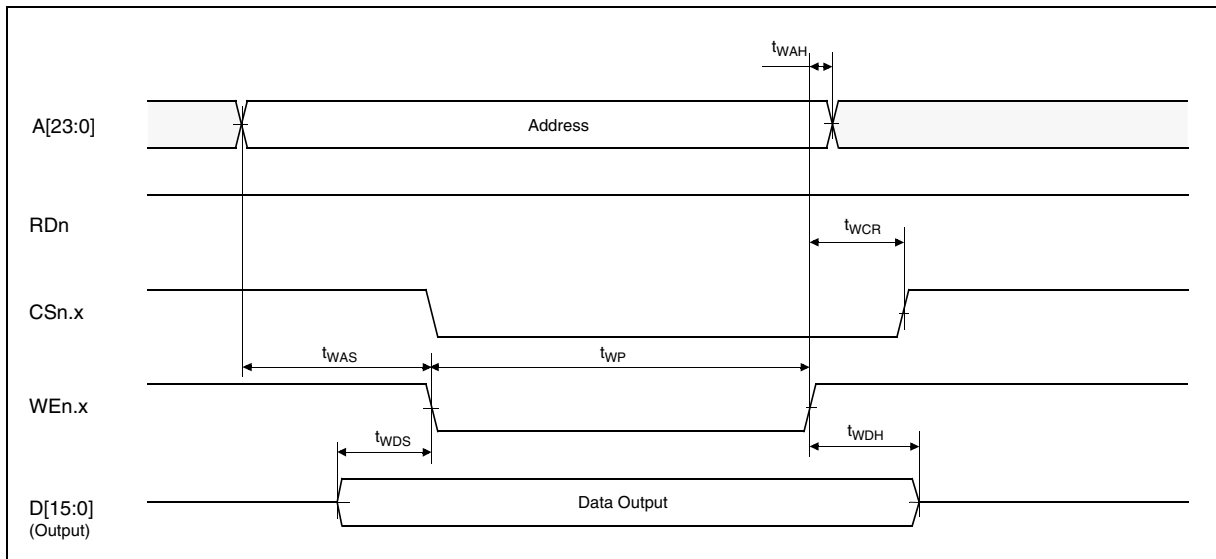
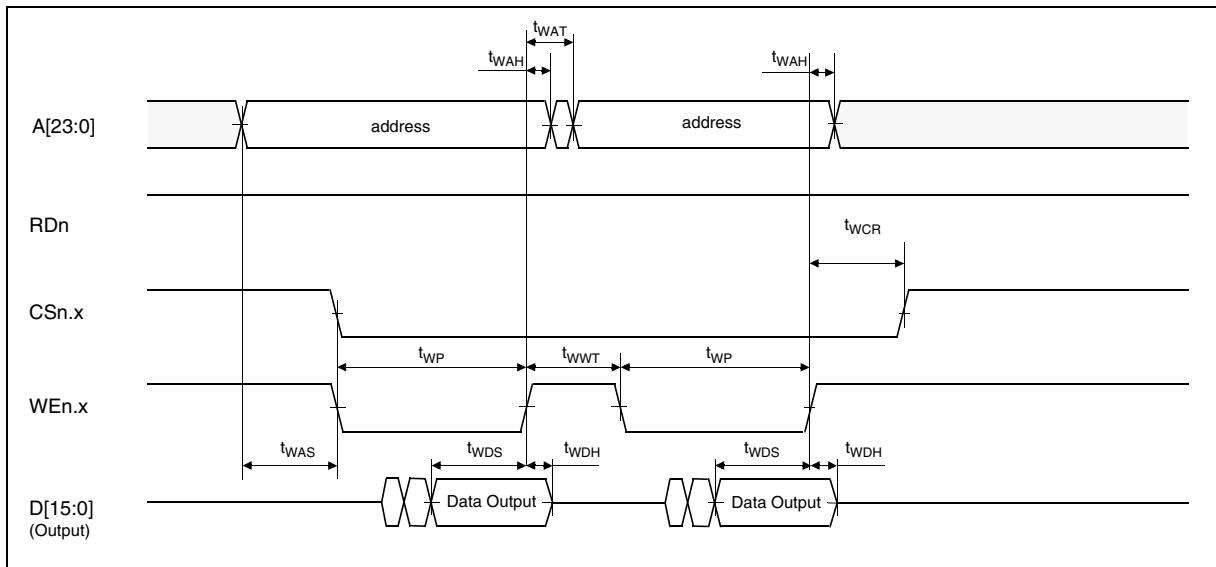


Figure 15. Write Cycle Timing: 32-bit WRITE on 16-bit Memory



See [Table 22](#) for write timing data.

Figure 16. Write Cycle Timing: 16-bit WRITE on 8-bit Memory

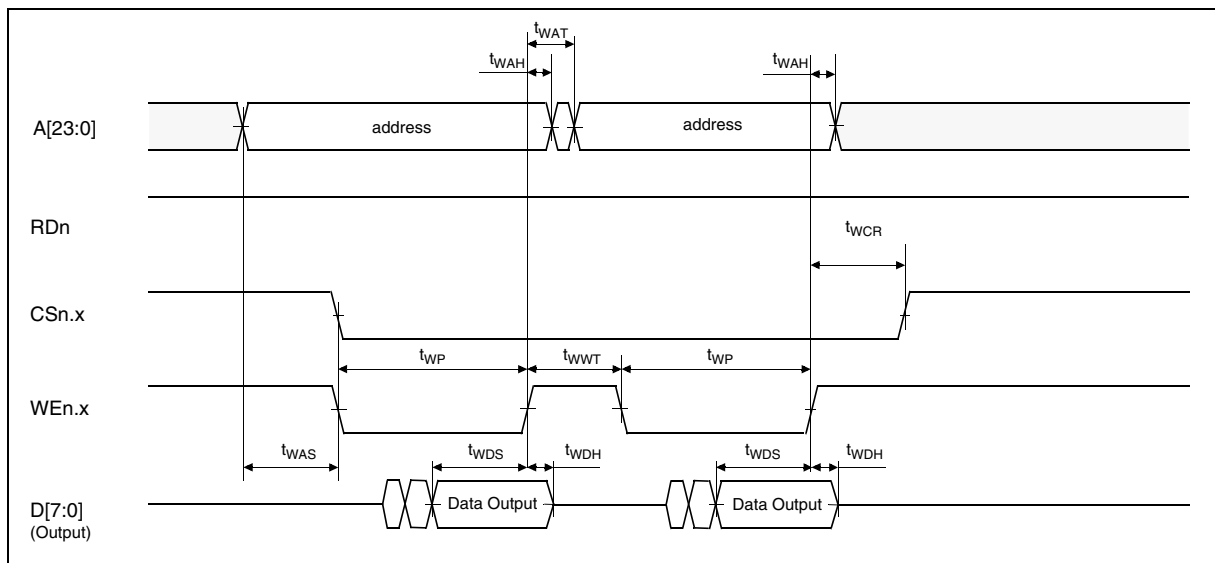
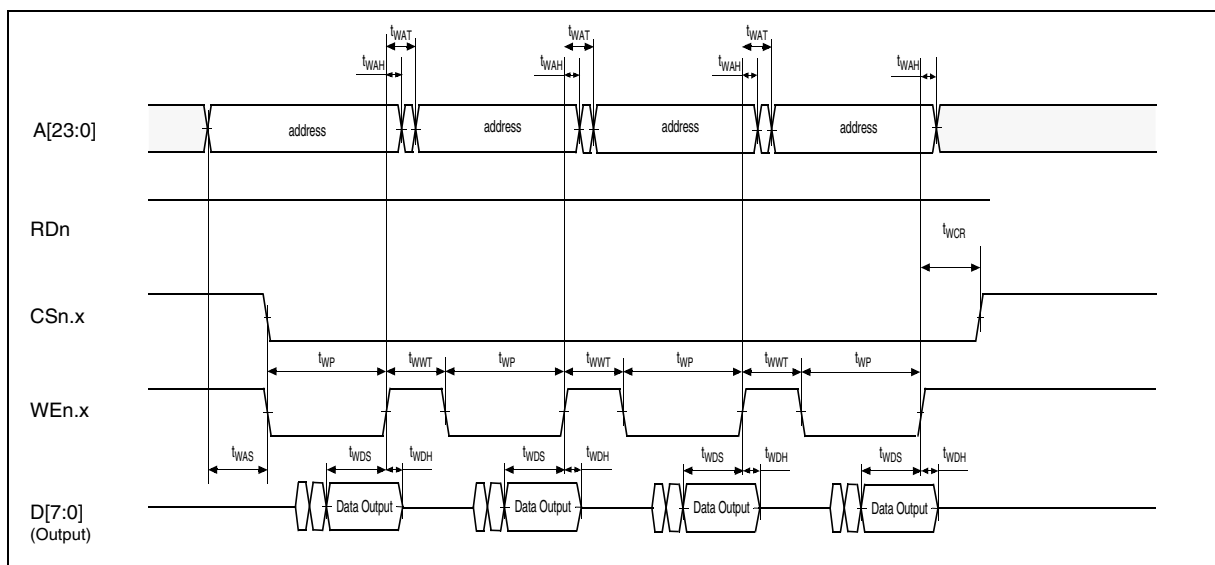


Figure 17. Write Cycle Timing: 32-bit WRITE on 8-bit Memory



See [Table 22](#) for write timing data.

2.11 ADC Electrical Characteristics

$V_{33} = 3.3 \pm 10\%$, $AV_{DD} = 3.3 \pm 10\%$, $T_A = -40 / 85 \text{ }^\circ\text{C}$ unless otherwise specified.

Table 23. ADC Electrical Characteristics

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|-----------------|----------------------------------|---|-------|-----|----------------|---------------|
| | | | Min | Typ | Max | |
| RES | Resolution | Sinewave with ΔV_{IN} amplitude | | 12 | | bits |
| ΔV_{IN} | Input Voltage Range | | 0 | | 2.5 | V |
| f_{MOD} | Modulator Oversampling Frequency | | | | 2.1 | MHz |
| IBW | Input Bandwidth | | | | $f_{MOD}/4096$ | kHz |
| N_{ch} | Number of Input Channels | | | | 4 | n |
| PBR | Passband Ripple | | | | 0.1 | dB |
| SINAD | S/N and Distortion | | 56 | 63 | | dB |
| THD | Total Harmonic Distortion | | 60 | 74 | | dB |
| Z_{IN} | Input Impedance | $f_{MOD} = 2 \text{ MHz}$ | 1 | | | $M\Omega$ |
| C_{IN} | Input Capacitance | | | | 5 | pF |
| I_{ADC} | Power Consumption | $T_A = 27 \text{ }^\circ\text{C}$ | | 2.5 | 3.0 | mA |
| I_{STBY} | Standby Power Consumption | $T_A = 27 \text{ }^\circ\text{C}$ | | | 1 | μA |

3 PACKAGE CHARACTERISTICS

3.1 Package Mechanical Data

Figure 18. 64-Pin Thin Quad Flat Package (10x10)

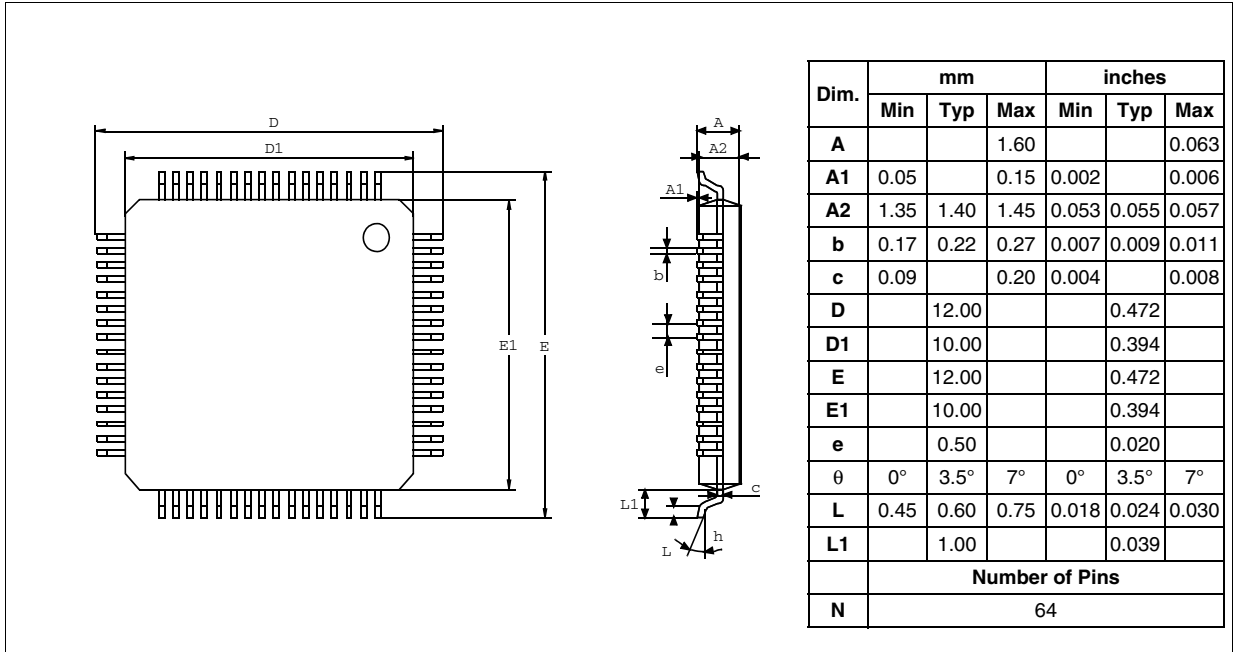


Figure 19. 144-Pin Thin Quad Flat Package

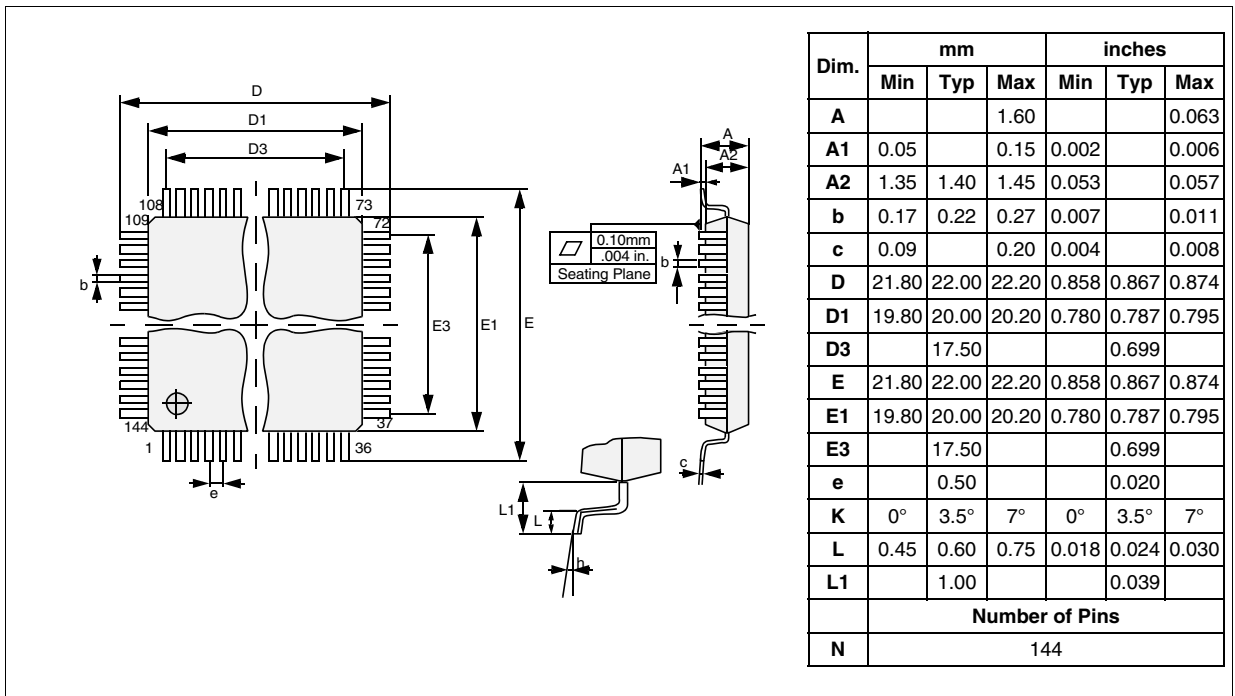


Figure 20. 64-Low Profile Fine Pitch Ball Grid Array Package

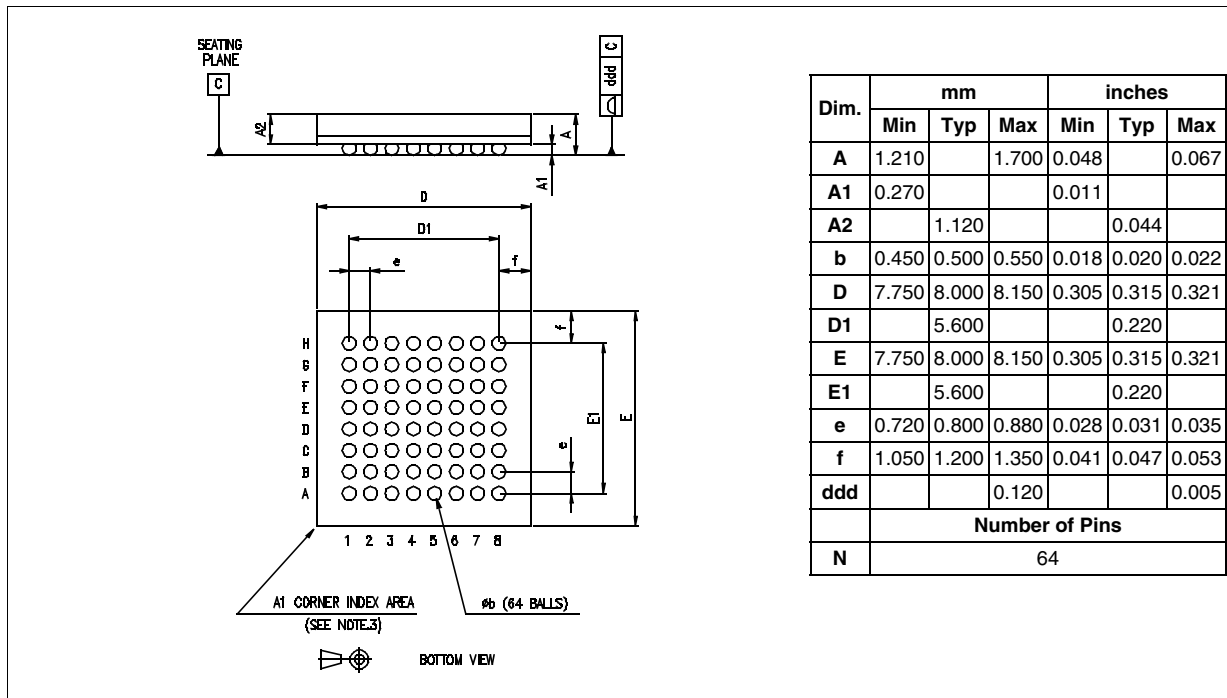
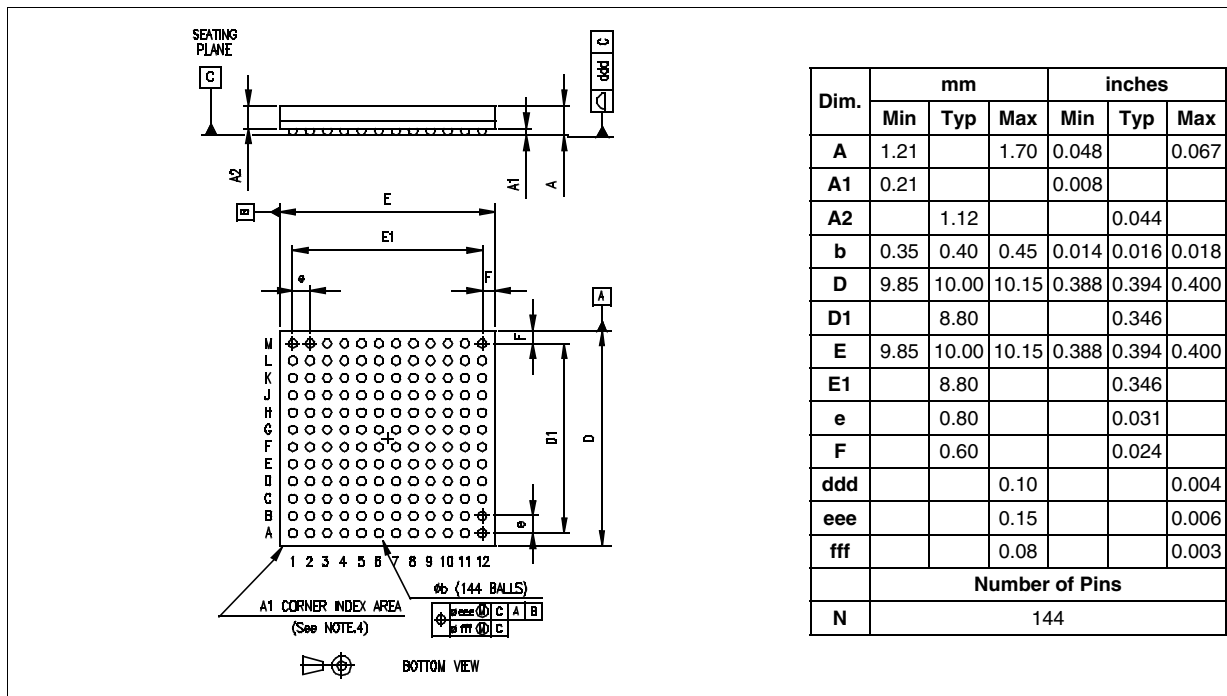


Figure 21. 144-Low Profile Fine Pitch Ball Grid Array Package



3.2 Thermal Characteristics

The average chip-junction temperature, T_J , in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \tag{1}$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the Chip Internal Power.
- $P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273^\circ\text{C}) \tag{2}$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273^\circ\text{C}) + \Theta_{JA} \times P_D^2 \tag{3}$$

where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A .

Table 24. Thermal characteristics

| Symbol | Parameter | Value | Unit |
|---------------|--|-------|------|
| Θ_{JA} | Thermal Resistance Junction-Ambient TQFP 144 - 20 x 20 mm / 0.5 mm pitch | 42 | °C/W |
| Θ_{JA} | Thermal Resistance Junction-Ambient TQFP 64 - 10 x 10 mm / 0.5 mm pitch | 45 | °C/W |
| Θ_{JA} | Thermal Resistance Junction-Ambient LFBGA 64 - 8 x 8 x 1.7mm | TBD | °C/W |
| Θ_{JA} | Thermal Resistance Junction-Ambient LFBGA 144 - 10 x 10 x 1.7mm | TBD | °C/W |

4 ORDER CODES

Table 25. Order Codes

| Partnumber | FLASH Kbytes | RAM Kbytes | EMI | USB | CAN | I/O Ports | Package | Temp. Range |
|-------------|-----------------|---------------|-----|-----|-----|--------------|-------------------|-----------------|
| STR710FZ1T6 | 128+16 | 32 | Yes | Yes | Yes | 48 | TQFP144 20 x 20 | -40 to +85°C |
| STR710FZ2T6 | 256+16 | 64 | | | | | | |
| STR710FZ1H6 | 128+16 | 32 | Yes | Yes | Yes | 48 | LFBGA 10 x 10 1.7 | |
| STR710FZ2H6 | 256+16 | 64 | | | | | | |
| STR711FR0H6 | 64+16 | 16 | No | Yes | No | 30 | LFBGA64 8 x 8 1.7 | |
| STR711FR0T6 | 64+16 | 16 | | | | | TQFP64 10x10 | |
| STR711FR1T6 | 128+16 | 32 | | | | | | |
| STR711FR2T6 | 256+16 | 64 | | | | | | |
| STR712FR0H6 | 64+16 | 16 | | | | | LFBGA64 8 x 8 1.7 | |
| STR712FR0T6 | 64+16 | 16 | | | | | TQFP64 10 x10 | |
| STR712FR1T6 | 128+16 | 32 | | No | Yes | 32 | | |
| STR712FR2T6 | 256+16 | 64 | | | | | | |
| STR715FR0H6 | 64+16 | 16 | | | | | LFBGA64 8 x 8 1.7 | |
| STR715FR0T6 | 64+16 | 16 | | | | | TQFP64 10 x 10 | |
| | | | | | | | | |
| | | | | | | | | |

5 REVISION HISTORY

Table 26. Revision history

| Date | Revision | Description of Changes |
|-------------|----------|---|
| 17-Mar-2004 | 1 | First Release |
| 05-Apr-2004 | 2 | Updated "ELECTRICAL CHARACTERISTICS" on page 30 |
| 08-Apr-2004 | 2.1 | Corrected STR712F Pinout. Pins 43/42 swapped. |
| 15-Apr-2004 | 2.2 | PDF hyperlinks corrected. |
| 7-Jul-2004 | 3 | Corrected description of STDBY, V18, VSS18 V18BKP VSSBKP pins Added IDDrn typical data Updated BSPI max. baudrate. Updated "External Memory Bus Timing" on page 38 |
| 29-Oct-2004 | 4 | Corrected Flash sector B1F0/F1 address in Figure 6 on page 27 Corrected Table 6 on page 21 TQFP64 TEST pin is 16 instead of 17. Added to TQFP64 column: pin 7 BOOTEN, pin 17 V _{33IO-PLL} Changed description of JTCK from 'External pull-down required' to 'External pull-up or pull down required'. |
| 25-Jan-2005 | 5 | Changed "Product Preview" to "Preliminary Data" on page 1 and 3 Renamed 'PU/PD' column to 'Reset state' in Table 6 on page 21 Added reference to STR7 Flash Programming Reference Manual |
| 19-Apr-2005 | 6 | Added STR715F devices and modified RAM size of STR71xF1 devices Added BGA package in Section 3 Updated ordering information in Section 4 . Added PLL duty cycle min and max. in Section 2.8 |

Notes:

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