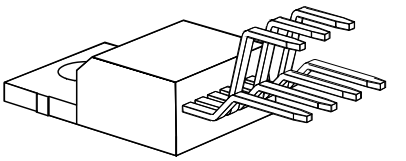
SIEMENS

3-A DC Motor Driver — TLE 5203

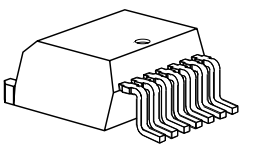
Overview — SPT IC [1)]

Features

- Output current ± 3 A
- I/O error diagnostics
- Short-circuit proof
- Four-quadrant operation
- Integrated free-wheeling diodes
- Wide temperature range
- Open load detection
- Break low, if break high required, the device TLE 5204 will fit



P-TO220-7-1



P-TO220-7-8

Type	Ordering Code	Package
TLE 5203	Q67000-A9096	P-TO220-7-1
TLE 5203 G	Q67006-A9242	P-TO220-7-8

Description

TLE 5203 is an integrated power bridge with DMOS output stages for driving DC motors.

This motor bridge is optimized for driving DC motors in reversible operation. The internal protective circuitry in particular ensures that no crossover currents can occur.

Because the free-wheeling diodes are integrated, the external circuitry that is necessary is reduced to the capacitors on the supply voltage.

The control inputs have TTL/CMOS-compatible levels.

[1)] SIEMENS Power Technology

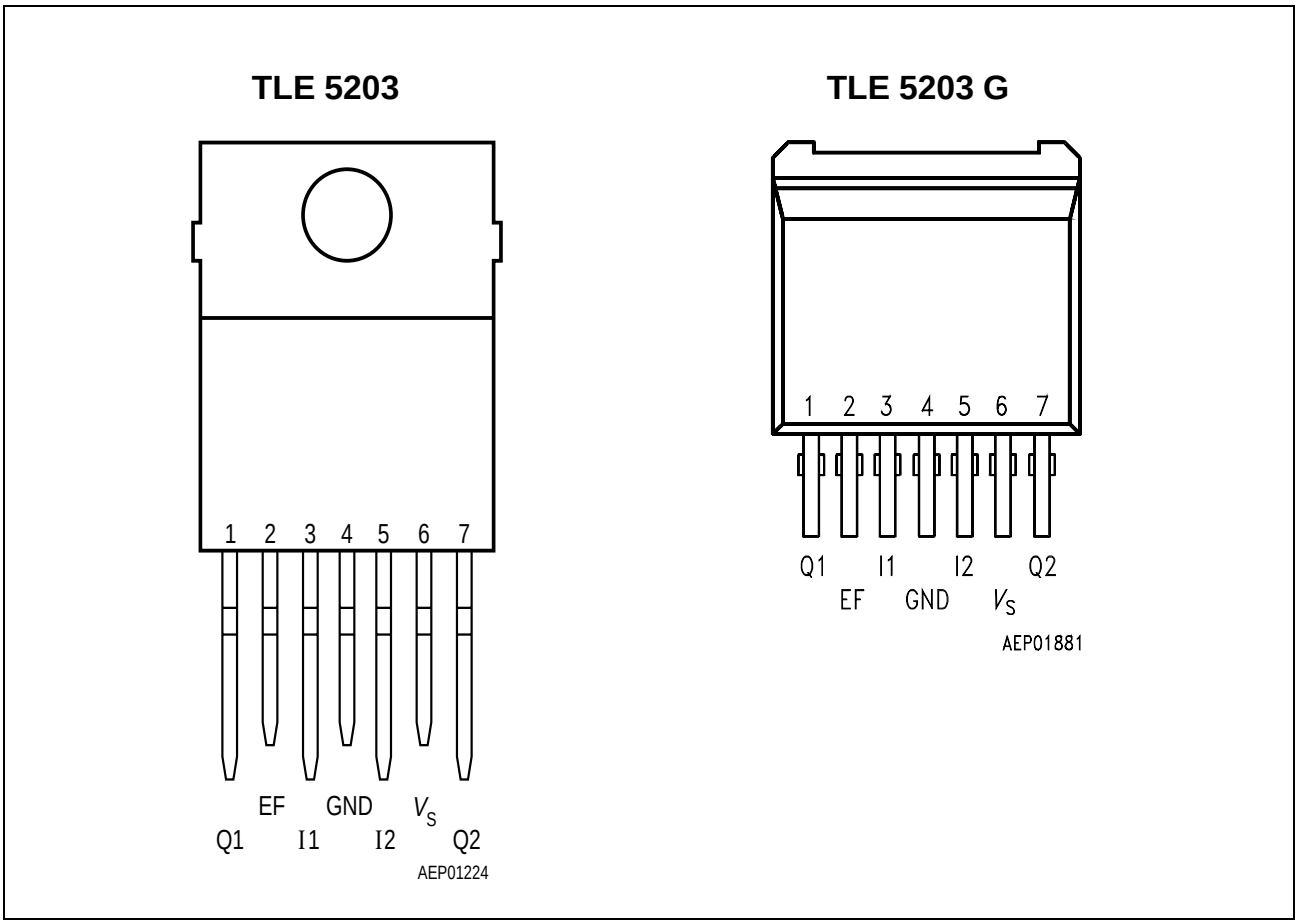


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	Q1	**Output of channel 1;** Short-circuit proof, free-wheeling diodes integrated for inductive loads
2	EF	**Error flag;** TTL/CMOS-compatible output for error detection (open drain)
3	I1	**Control input 1;** TTL/CMOS-compatible
4	GND	**Ground;** connected internally to cooling fin
5	I2	**Control input 2;** TTL/CMOS-compatible
6	V_S	**Supply voltage;** wire with capacitor matching load
7	Q2	**Output of channel 2;** Short-circuit proof, free-wheeling diodes integrated for inductive loads

Circuit Description

Input Circuit

The control inputs consist of TTL/CMOS-compatible Schmitt triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages.

Output Stages

The output stages form a switched H-bridge. Protective circuits make the outputs short-circuit proof to ground and to the supply voltage throughout the operating range. Positive and negative voltage spikes, which occur when switching inductive loads, are clamped by integrated power diodes.

Functional Truth Table

E1	E2	Q1	Q2	Comments
L	L	H	L	Motor turns counterclockwise
L	H	L	H	Motor turns clockwise
H	L	L	L	Brake; both low side transistors turned-ON
H	H	Z	Z	Open circuit detection

Notes for Output Stage

Symbol	Value
L	Low side transistor is turned-ON High side transistor is turned-OFF
H	High side transistor is turned-ON Low side transistor is turned-OFF
Z	High side transistor is turned-OFF Low side transistor is turned-OFF

Monitoring Functions

An internal circuit ensures that all output transistors are turned-OFF if the supply voltage is below the operating range.

A monitoring circuit for each output transistor detects whether the particular transistor is active and in this case prevents the corresponding source transistor (sink transistor) from conducting in sink operation (source operation). Therefore no crossover currents can occur. Pulse-width operation is possible up to a maximum switching frequency of 1 kHz for any load.

Depending on the load current higher frequencies are possible.

Protective Function

Various errors like short-circuit to + V_S, ground or across the load are detected. All faults result in turn-OFF of the output stages after a delay of 40 µs and setting of the error flag EF to ground. Changing the inputs resets the error flag.

Output Shorted to Ground Detection

If a high side transistor is switched on and its output is shorted to ground, the output current is limited to typ 8 A. After a delay of 40 µs all outputs will be switched off and the error flag EF is set to ground.

Output Shorted to + V_S and Overload Detection

An internal circuit detects if the current through the low side transistor is higher than 4 A typ. In this case all outputs are turned off after 40 µs and the error flag EF is set to ground.

At a junction temperature higher than 160 °C the thermal shutdown turns off, all four output stages commonly and the error flag is set without a delay.

Open Load Detection

The output Q1 has a 10 kΩ pull-up resistor and the output Q2 has a 10 kΩ pull-down resistor. If E1 and E2 are high, all output power stages are turned-OFF. In case of no load between Q1 and Q2 the output voltage Q1 is V_S and Q2 is ground. This state will be detected by two comparators and an error flag will be set after a delay time of 40 µs. Changing the inputs resets the error flip flop.

Diagnosis

Input		Output		Diagnosis				EF
E1	**E2**	**Q1**	**Q2**	**Shorted to GND**	**Shorted to V_S**	**Overload**	**Open Load**	
L	L	H	L	Q1	Q2	X	–	L
L	H	L	H	Q2	Q1	X	–	L
H	L	L	L	–	Q1, Q2	–	–	L
H	H	Z	Z	–	–	–	X	L

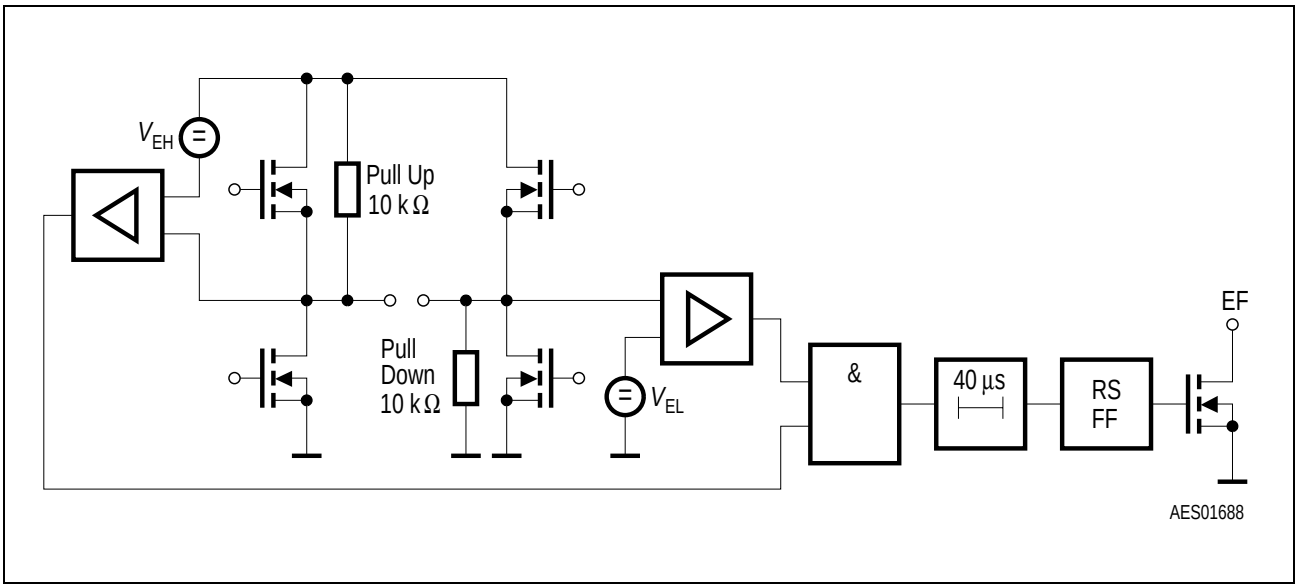


Figure 2 Simplified Schematic for Open Load Detection

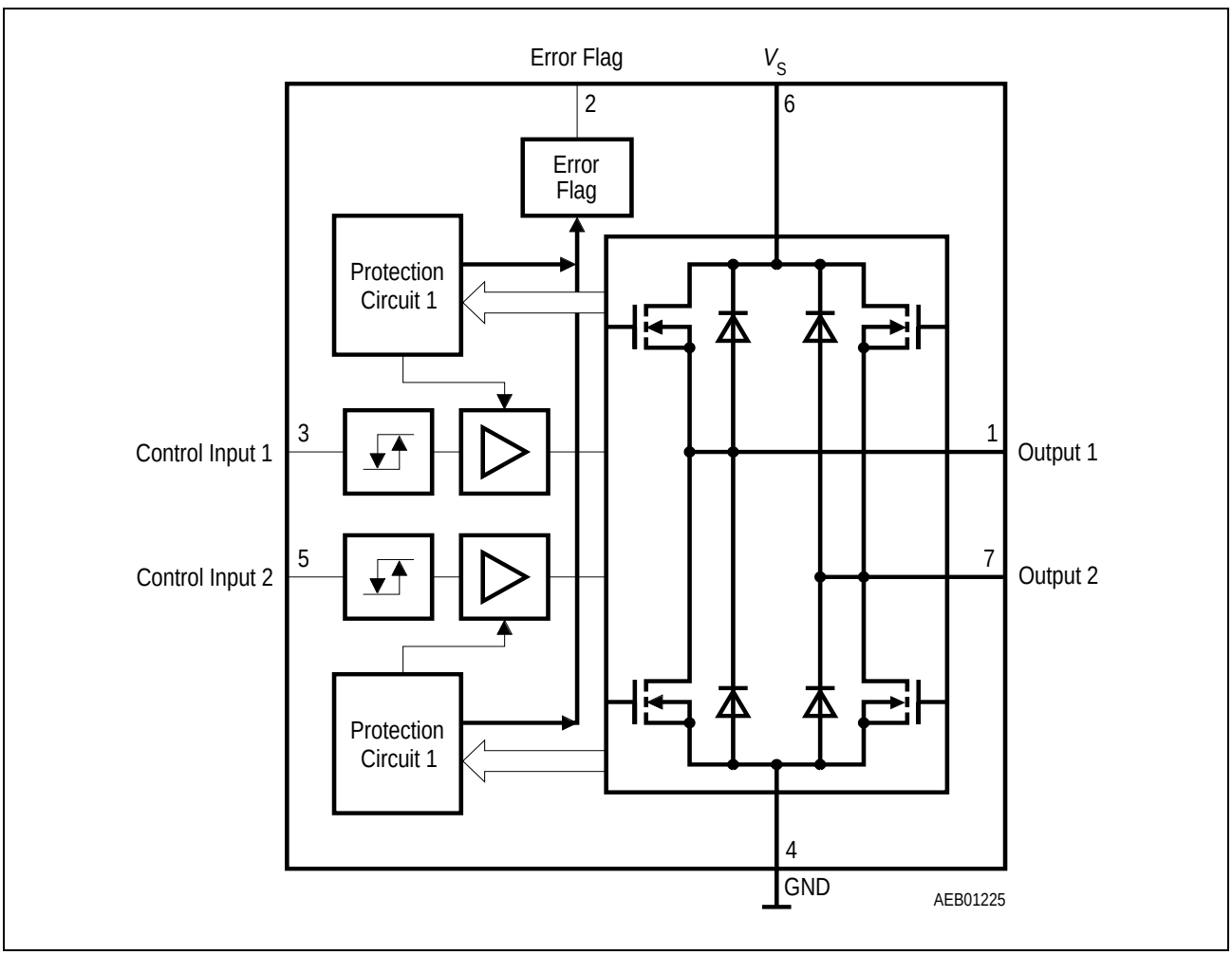


Figure 3 Block Diagram

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltage					
Supply voltage	V_S	– 0.3	40	V	–
Supply voltage	V_S	– 1	–	V	t < 500 ms; I_S < 5 A
Logic input voltage	$V_{I1,2}$	– 0.3	7	V	V_S = 0 – 40 V
Diagnostics output voltage	V_{EF}	– 0.3	7	V	–
Current					
Free-wheeling current	I_F	– 4	4	A	$T_j \leq$ 150 °C
Output current [1]	I_Q	– 4	4	A	–
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Thermal Resistance					
Junction-case	$R_{th\ jC}$	–	4	K/W	–
Junction-ambient	$R_{th\ jA}$	–	65	K/W	–
Operating Range					
Supply voltage	V_S	6	24	V	–
Logic input voltage	$V_{I1,2}$	– 0.3	7	V	–
Switching frequency [2]	f	–	1	kHz	–
Junction temperature	T_j	– 40	150	°C	–

[1] During overload condition currents higher than 4 A can dynamically occur, before the device shuts off, without any damaging the device.

[2] Depending on load higher frequencies are possible.

Electrical Characteristics

V_S = 6 to 18 V; T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General						
Quiescent current	I_q	–	–	10	mA	I_L = 0 A
Turn-ON delay	t_{d1}	–	10	20	µs	Input to output
Turn-OFF delay	t_{d2}	–	–	10	µs	Input to output
Turn-ON time	t_r	–	10	20	µs	I_Q = 2.5 A; cf diagram
Turn-OFF time	t_f	–	–	10	µs	I_Q = 2.5 A; cf diagram
Undervoltage	V_S	–	5.5	5.9	V	$I_{C\ ON}$
Undervoltage	V_S	–	4.5	5.2	V	$I_{C\ OFF}$
Logic						
Control inputs						
H-input voltage	V_{IH}	2.8	–	–	V	–
L-input voltage	V_{IL}	–	–	1.2	V	–
Hysteresis of input voltage	ΔV_I	0.4	0.8	1.2	V	–
H-input current	I_I	– 2	–	2	µA	$V_I = V_{IH}$
L-input current	I_I	– 10	– 4	0	µA	$V_I = V_{IL}$
Diagnosis output						
Delay time	t_d	20	40	60	µs	–
L-output voltage	V_{EF}	–	–	0.4	V	I = 3 mA
Leakage current	I_{RD}	–	–	10	µA	–
Error detection						
Switching threshold U	V_{EH}	2	2.7	3.5	V	Error low
Switching threshold L	V_{EL}	2	2.7	3.5	V	Error high
Overcurrent 1	I_{F1}	3	4	5	A	Error low

Electrical Characteristics (cont'd)

V_S = 6 to 18 V; T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Outputs						
RDSONU	–	–	–	0.4	Ω	V_S > 6 V; T_j = 25 °C 1)
RDSONU	–	–	–	0.65	Ω	V_S > 6 V; T_j = 150 °C 1)
RDSONL	–	–	–	0.4	Ω	V_S > 6 V; T_j = 25 °C 1)
RDSONL	–	–	–	0.65	Ω	V_S > 6 V; T_j = 150 °C 1)
Diode forward voltage	V_{FU}	–	–	1.5	V	I_F = 3 A
Diode forward voltage	V_{FL}	–	–	1.5	V	I_F = 3 A
Pull up/pull down	R	5	10	25	kΩ	–

1) Values for RDSON are for t > 100 µs after applying + V_S.

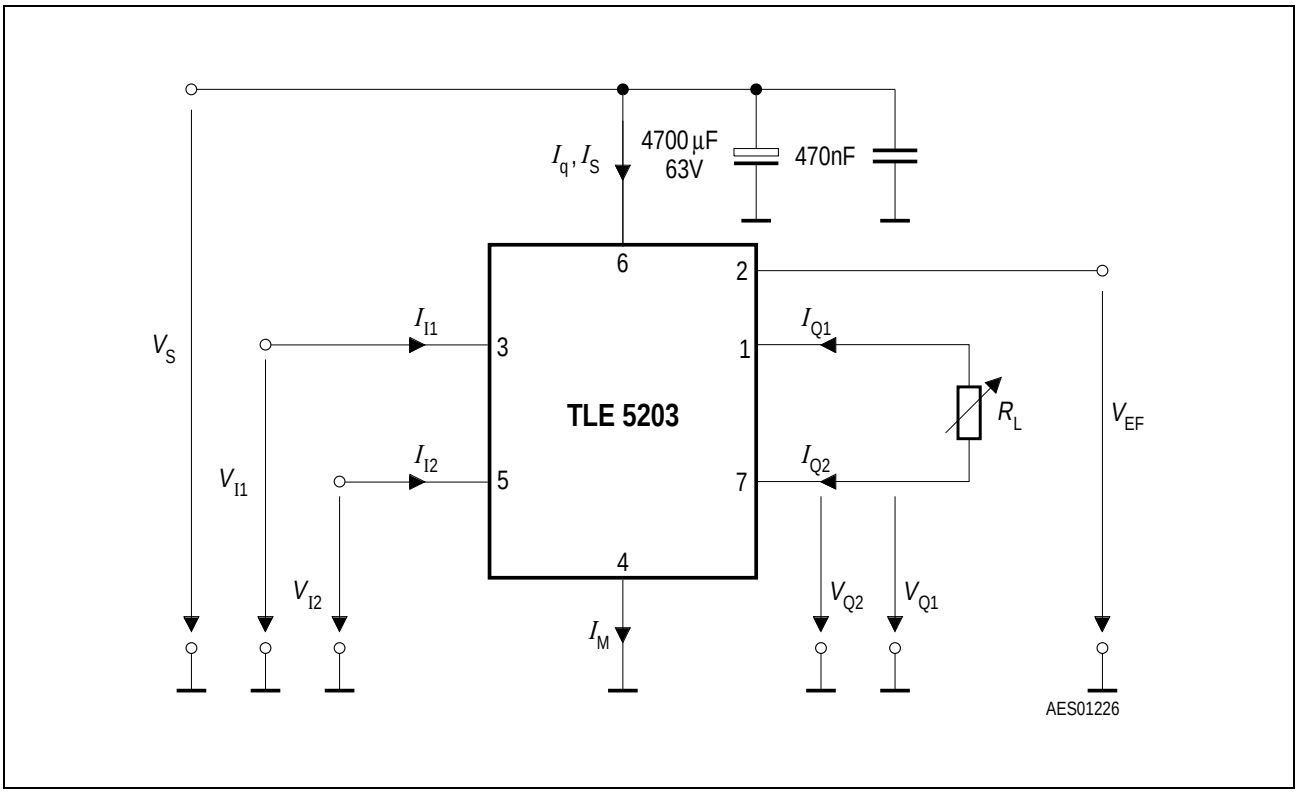


Figure 4 Test Circuit

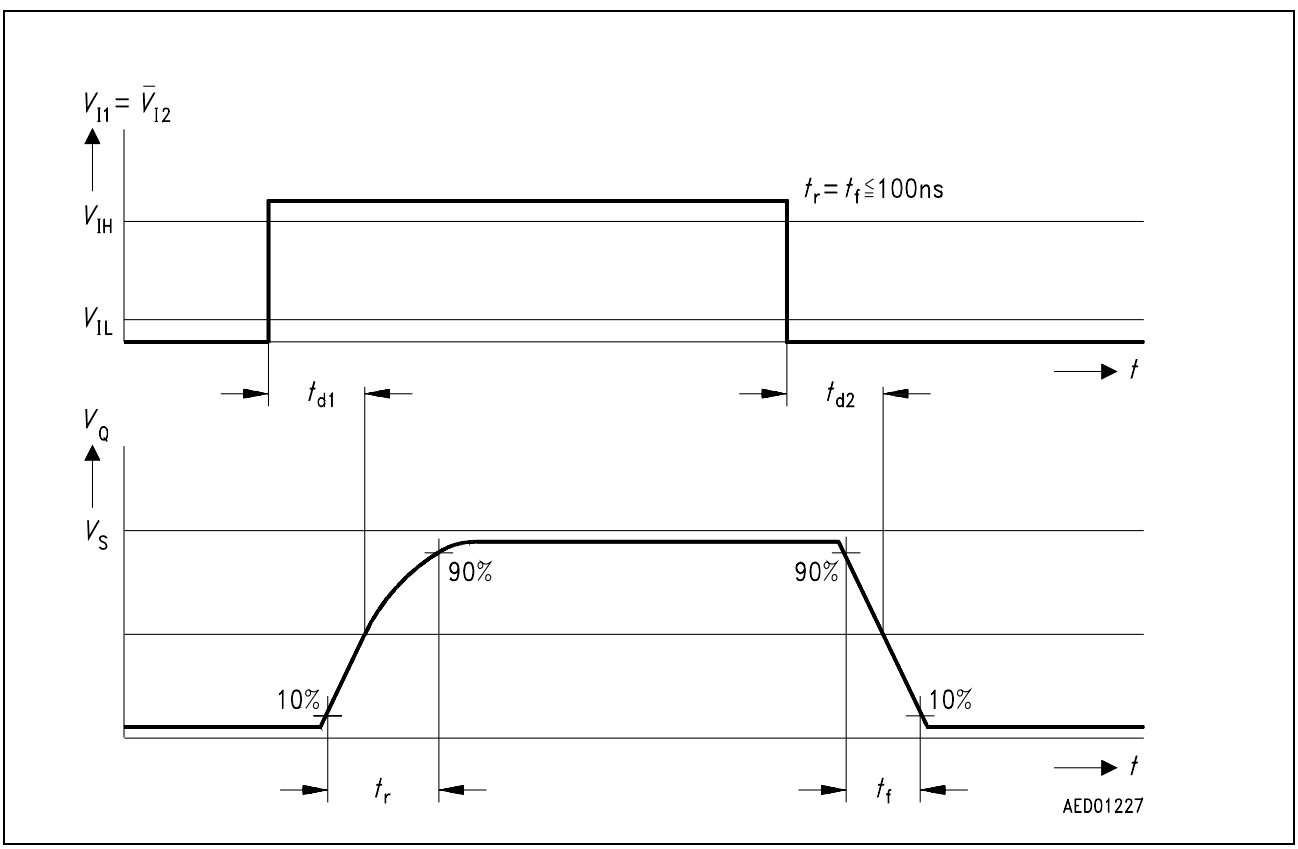
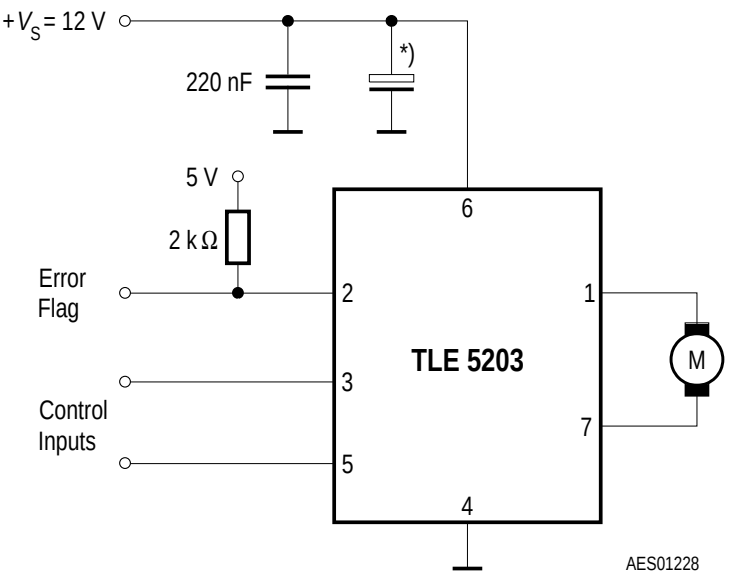


Figure 5 Timing Diagram

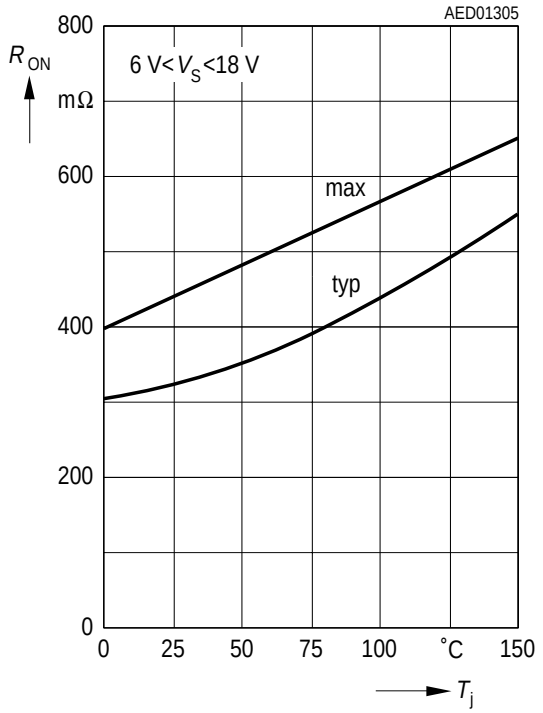


*) Necessary for isolating supply voltage or interruption (e.g. 470 µF).

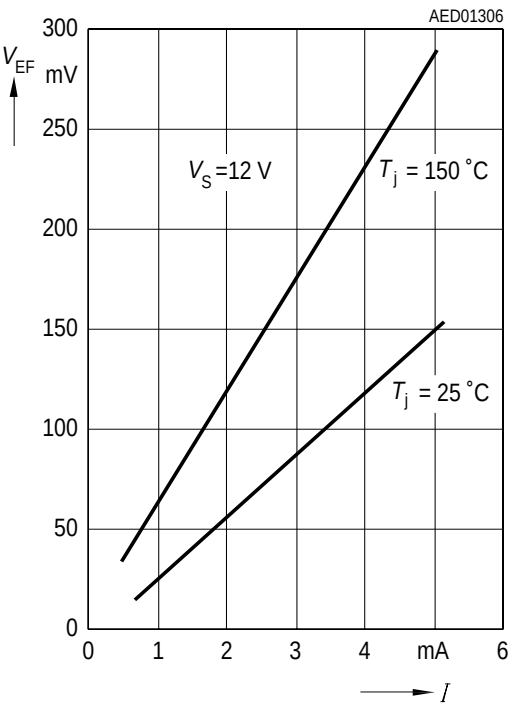
Figure 6 Application Circuit

Diagrams

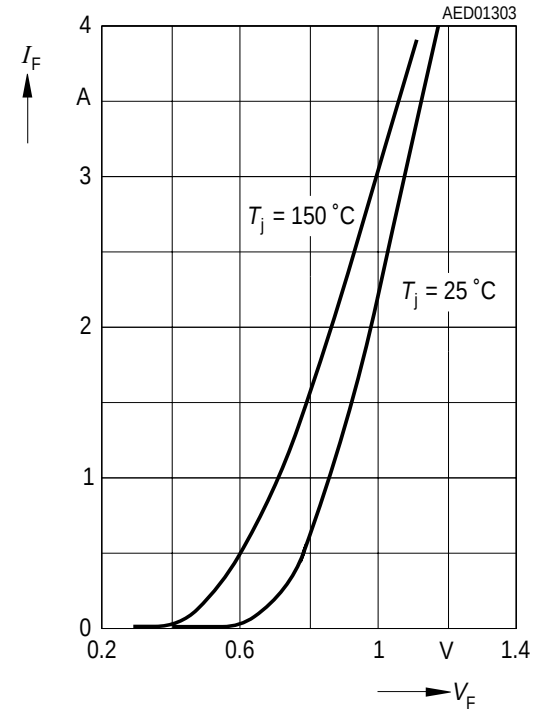
R_{ON} Resistance of Output Stage over Temperature



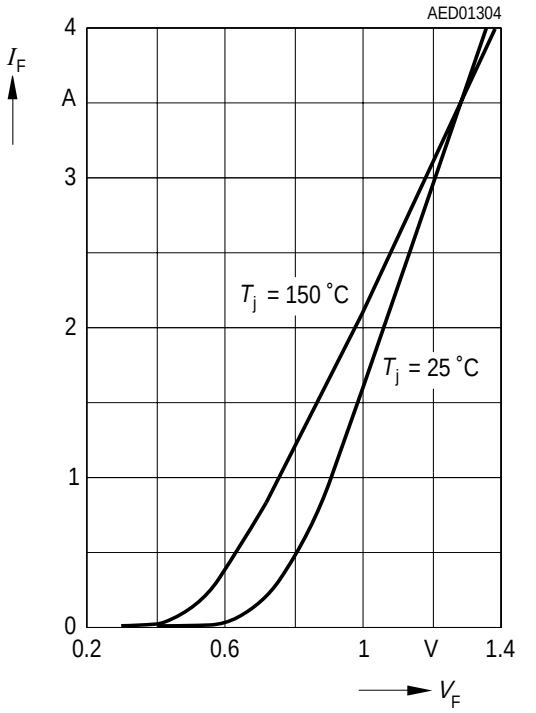
Output Voltage on Diagnostics Output versus Current



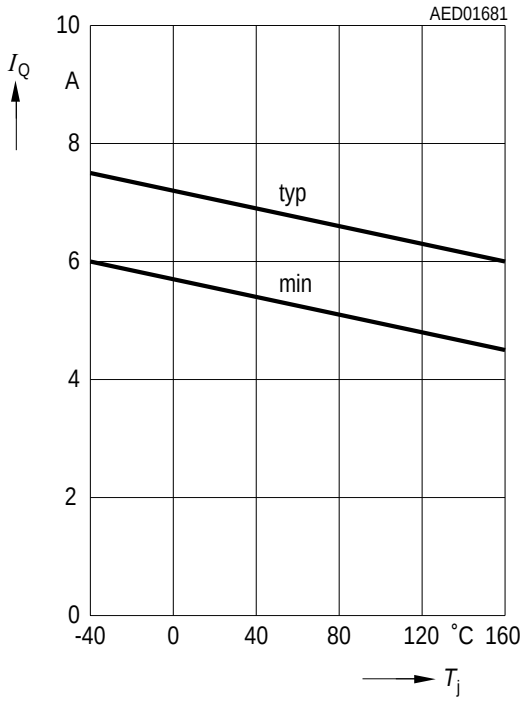
Forward Current of Upper Free-Wheeling Diode versus Voltage



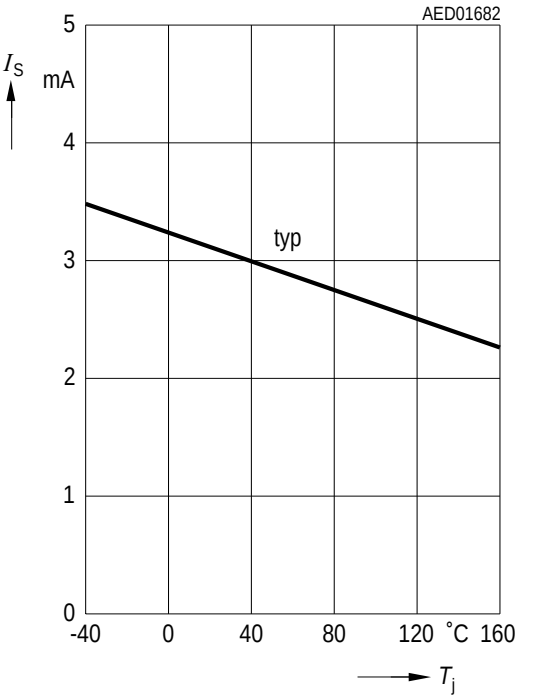
Forward Current of Lower Free-Wheeling Diode versus Voltage



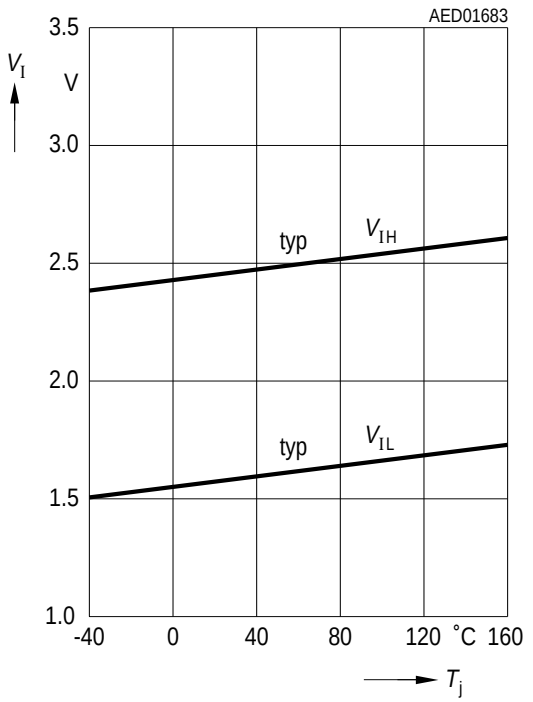
Overcurrent Threshold versus Temperature



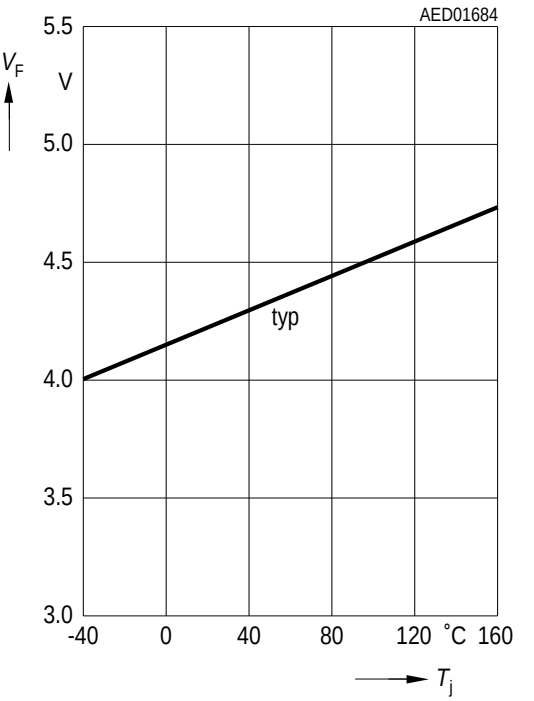
Quiescent Current versus Temperature



Input Threshold versus Temperature



Switching Threshold $V_{EL, EH}$ versus Temperature



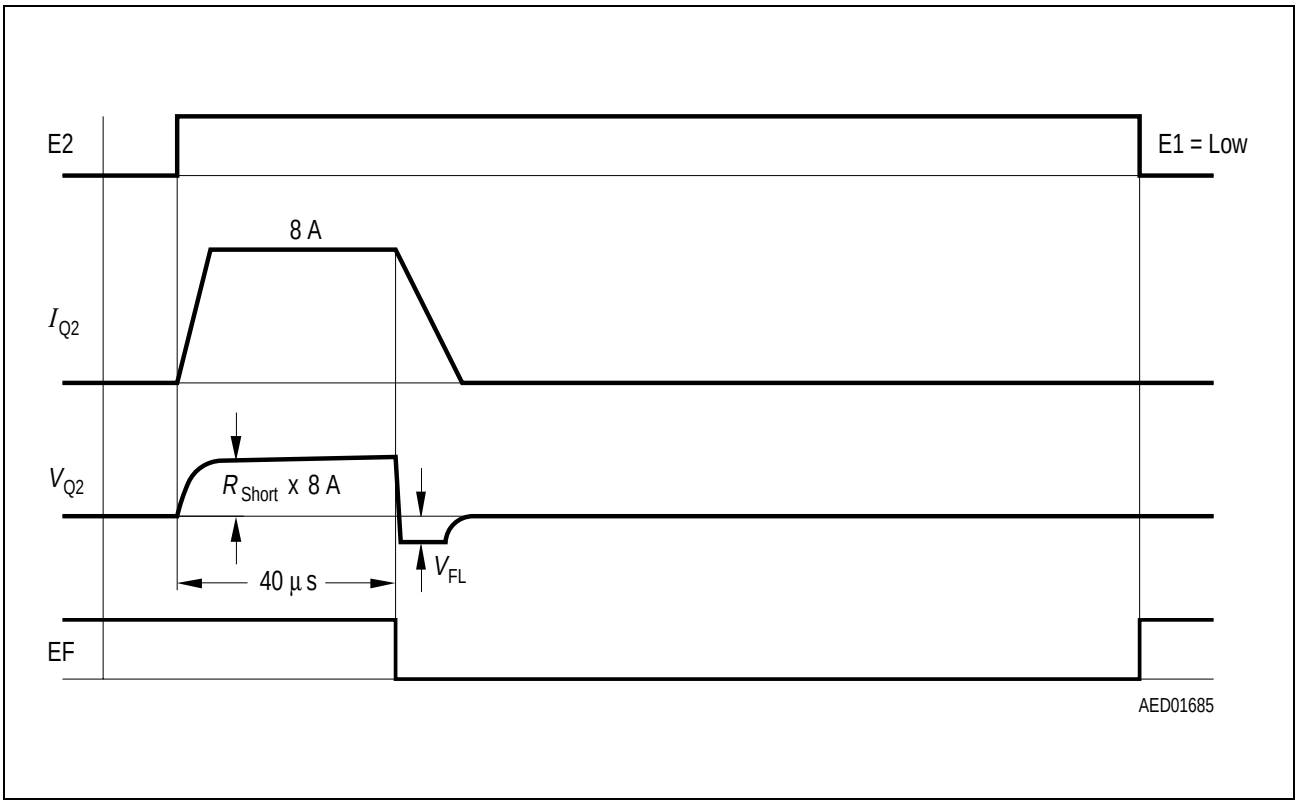


Figure 7 Timing Diagram for Output Shorted to Ground

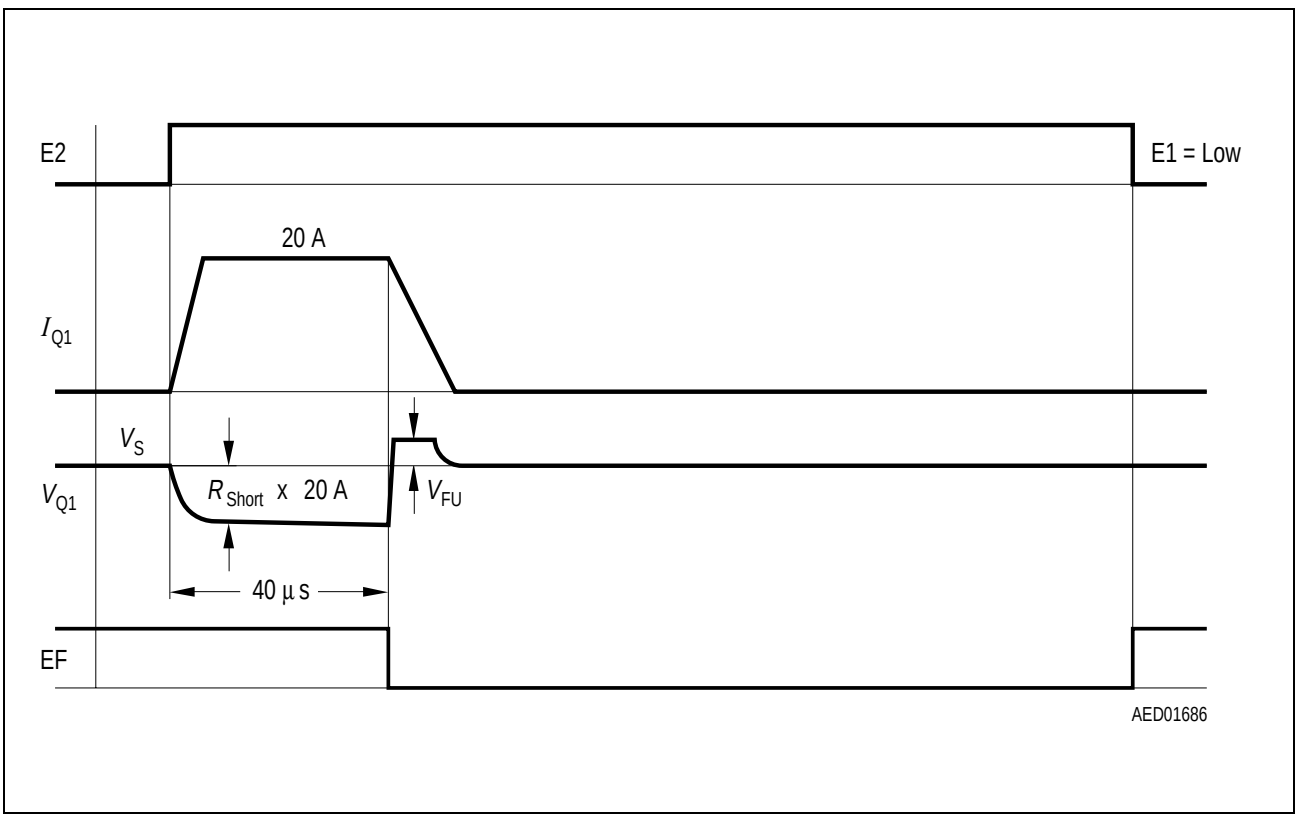


Figure 8 Timing Diagram for Output Shorted to V_S

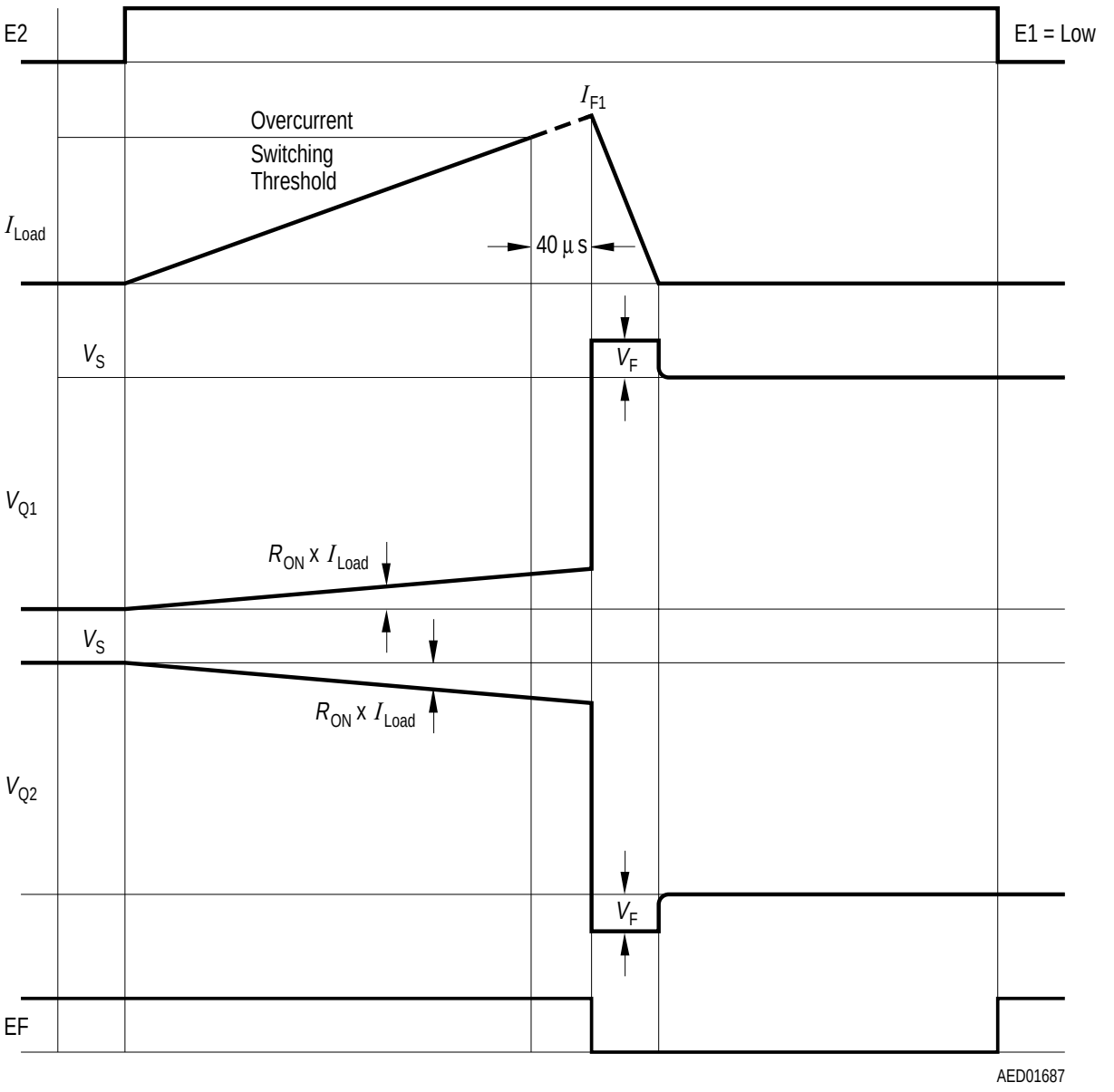


Figure 9 Timing Diagram for Overcurrent

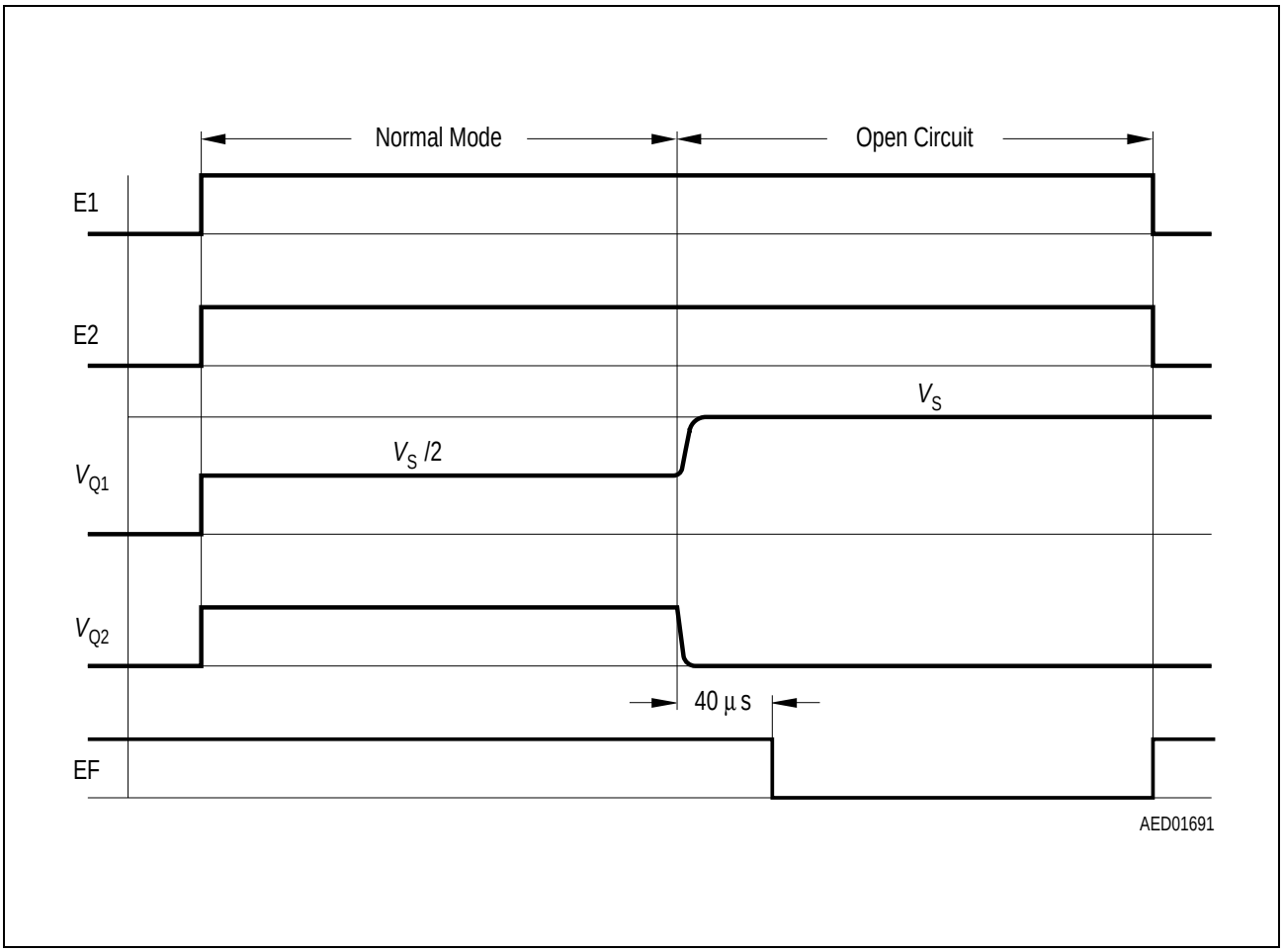
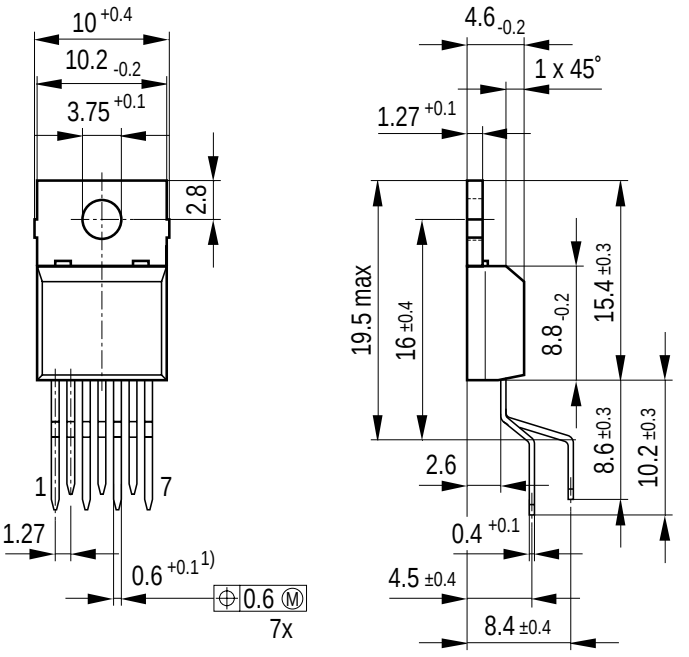


Figure 10 Timing Diagram for Open Load

Package Outlines

P-TO220-7-1
(Plastic Transistor Single Outline)



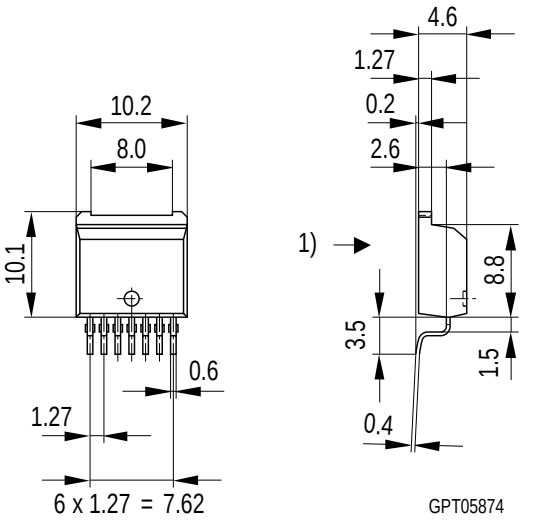
1) 0.75 $_{-0.15}$ at dam bar (max 1.8 from body)
1) 0.75 $_{-0.15}$ im Dichtstegbereich (max 1.8 vom Körper)

GPT05108

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

P-TO220-7-8 (SMD)
(Plastic Transistor Single Outline)



1) shear and punch direction burr free surface

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SMD = Surface Mounted Device

Dimensions in mm