

BIPOLAR DIGITAL INTEGRATED CIRCUIT

μ PB565

1 GHz HIGH SENSITIVITY PRESCALER

The μ PB565 is a general purpose prescaler intended for use in PLL Digital Tuning System. This is operated until 1 GHz by utilizing advanced bipolar process technology. This prescaler provides $\div 64$, $\div 8$, $\div 4$ and $\div 2$ division ratio, and can be used for TV and CATV.

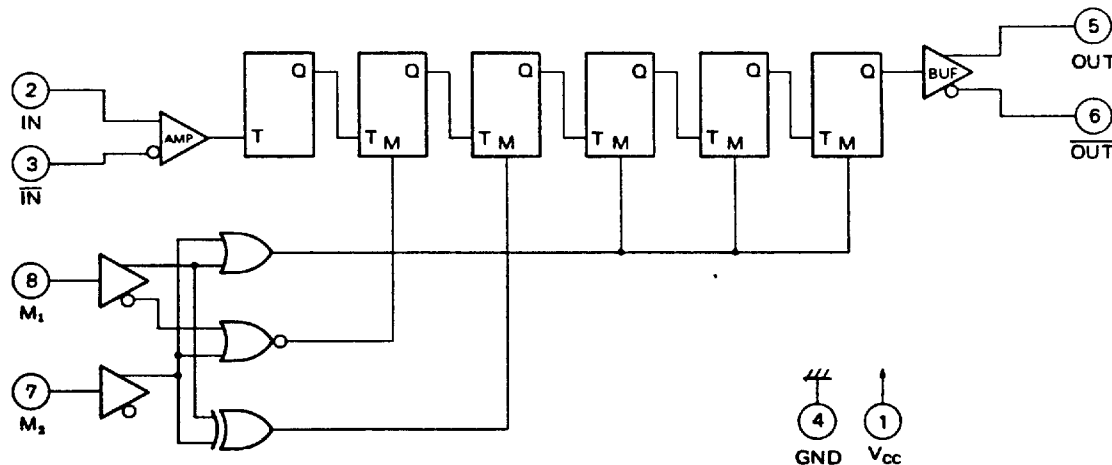
FEATURES

- High frequency operation : ($\div 64$, $\div 8$, $\div 4$) 1 GHz MAX.
 ($\div 2$) 500 MHz MAX.
- High sensitivity : 60 mV_{p.p} MIN.
- Wide band operation : 90 MHz to 1 GHz
- Low radiation
 Low level output (0.6 V_{p.p} TYP.)

ORDERING INFORMATION

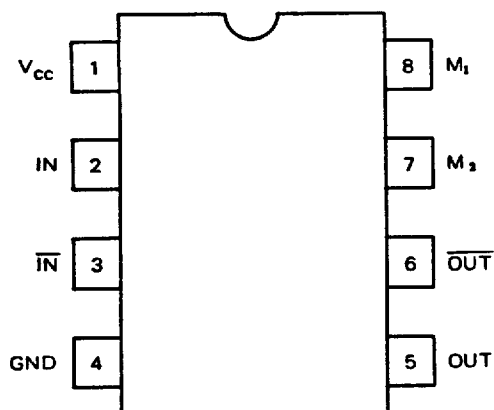
Order Code	Package
μ PB565C	8 pin plastic DIP (300 mil)

BLOCK DIAGRAM



NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

CONNECTION DIAGRAM (Top View)



1. V_{cc} : Power Supply Pin (+5V)
2. IN : Signal Input Pin (Positive Logic)
3. $\overline{\text{IN}}$: Signal Input Pin (Negative Logic)
4. GND : GND Pin
5. OUT : Output Pin (Positive Logic)
6. $\overline{\text{OUT}}$: Output Pin (Negative Logic)
7. M₂ : Division Ratio Control
8. M₁ : Division Ratio Control

DIVISION RATIO CONTROL

M ₁	M ₂	Division Ratio
H	L	÷2
L	H	÷4
H	H	÷8
L	L	÷64

H : V_{cc}

L : OPEN

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^{\circ}\text{C}$)

Supply Voltage	V_{CC}	-0.5 to +6.0	V
Input Voltage	V_I	-0.5 to $+V_{CC} + 0.3$	V
Output Current	I_O	-10	mA
Junction Temperature	T_j	+125	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

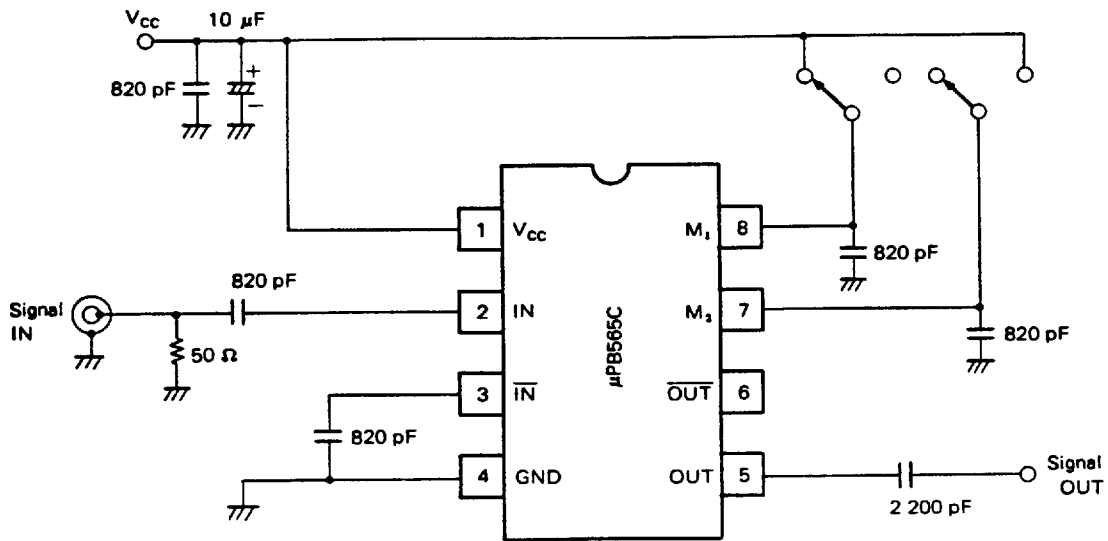
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Load Capacitance	C_L			30	pF
Ambient Temperature	T_a	-30		+75	$^{\circ}\text{C}$

ELECTRIC CHARACTERISTICS ($V_{CC} = 5.0 \pm 0.5\text{ V}$, $T_a = -30$ to $+75^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power Supply Current	I_{CC}		43	53.5	mA	$V_{CC} = 5\text{V}$, $T_a = 25^{\circ}\text{C}$
Output Voltage	V_O	0.4	0.6	0.8	$V_{p.p}$	OUT pin, $C_L = 5\text{ pF}$
High Level Input Voltage	V_{IH}	2.0			V	M1, M2 pin
Low Level Input Voltage	V_{IL}			0.8	V	M1, M2 pin
High Level Input Current	I_{IH}			150	μA	M1, M2 pin, $V_I = V_{CC}$
Low Level Input Current	I_{IL}	50			μA	M1, M2 pin, $V_I = 0$
Input Voltage	V_{in}	60		1500	mV _{p.p}	IN pin
Operating Frequency	f_{in}	90		1000	MHz	$V_{in} = 60\text{ mV}_{p.p} \div 4, \div 8, \div 64$
		90		500	MHz	$V_{in} = 60\text{ mV}_{p.p} \div 2$
		90		1150	MHz	$V_{in} = 120\text{ mV}_{p.p} \div 4, \div 8, \div 64$

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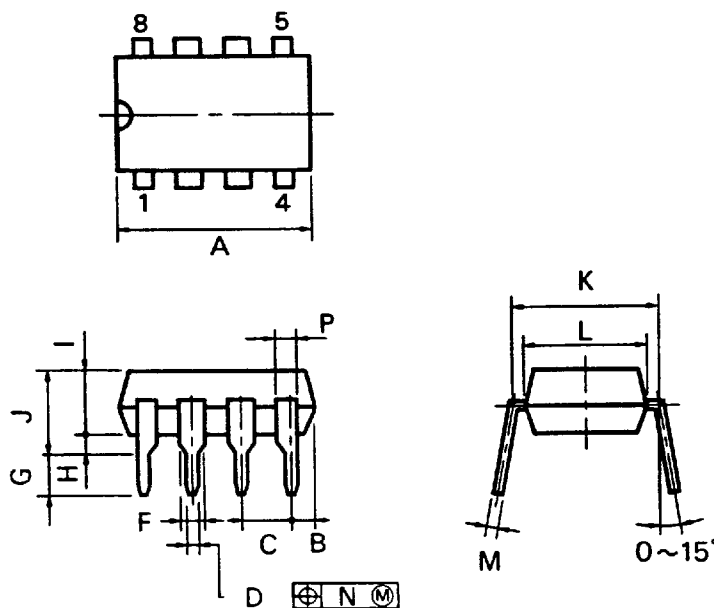
TEST CIRCUIT



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PACKAGE DIMENSIONS

8PIN PLASTIC DIP (300 mil)



P8C-100-300A

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	0.020 ± 0.004
F	1.4 MIN.	0.055 MIN.
G	2.9 ± 0.3	0.114
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 ± 0.10	0.010 ± 0.004
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.