DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD16306B

64-BIT HIGH-VOLTAGE CMOS DRIVER

The μPD16306B is a high voltage CMOS driver for flat display panels such as PDP, VFD and EL. It consists of a 64-bit bidirectional shift register, a 64-bit latch, and a high-voltage CMOS driver. The logic circuit operates on 5 V power supply (CMOS level input), so that it can be connected to a microcomputer. The driver block comprises 80 V, 50 mA MAX. high-voltage output buffer, and both the logic block and driver block consist of CMOS, allowing operation with low power consumption.

FEATURES

- 64-bit bidirectional shift registers
- Data control by transfer clock (external) and latch
- High-speed data transfer ($f_{MAX.}$ = 16 MHz MIN.: in cascade connection)
- Wide operating temperature range (T_A = −40 to +85 °C)
- High-voltage output (80 V, 50 mA MAX.)
- High-voltage Full CMOS process
- Polarities of all drivers can be reversed by using /PC pin.

★ **Remark** /xxx indicates active low signal.

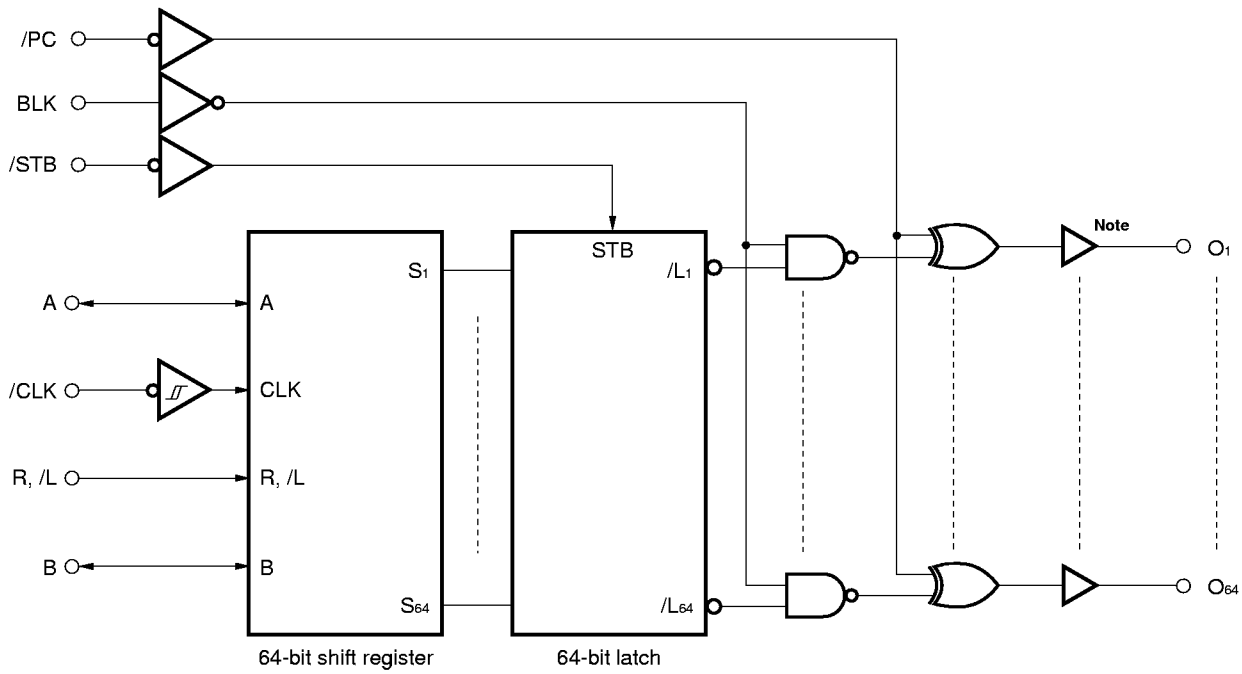
ORDERING INFORMATION

Part Number	Package
μPD16306BGF-3BA	100-pin plastic QFP (14 x 20 mm)
★ μPD16306BGC-9EU	100-pin plastic TQFP (fine pitch) (□ 14 mm)

Document No. S11519EJ3V0DS00 (3rd edition)
Date Published April 1999 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

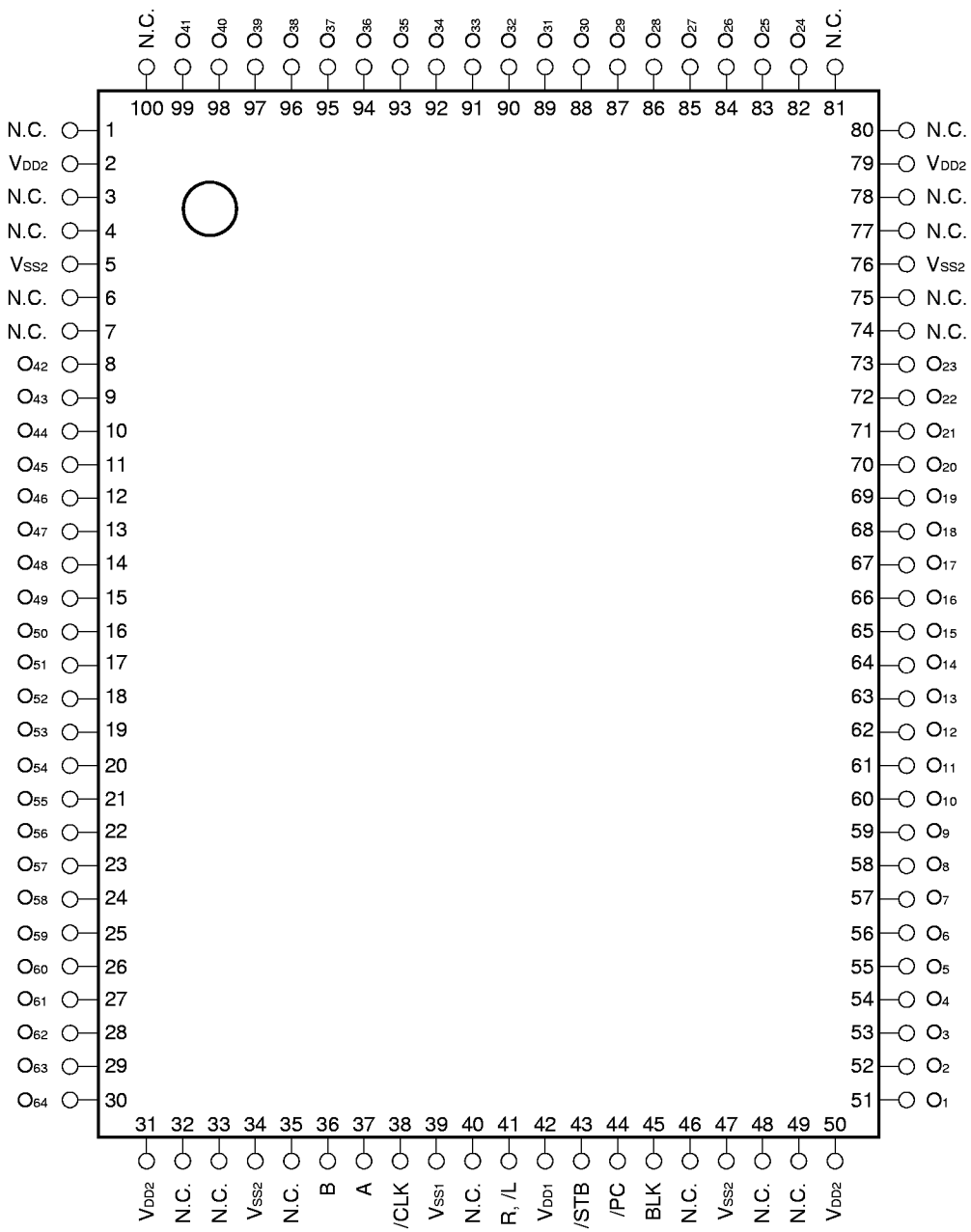
BLOCK DIAGRAM



Note High-voltage CMOS drivers (80 V, ±50 mA MAX.)

PIN CONFIGURATION (Top View)

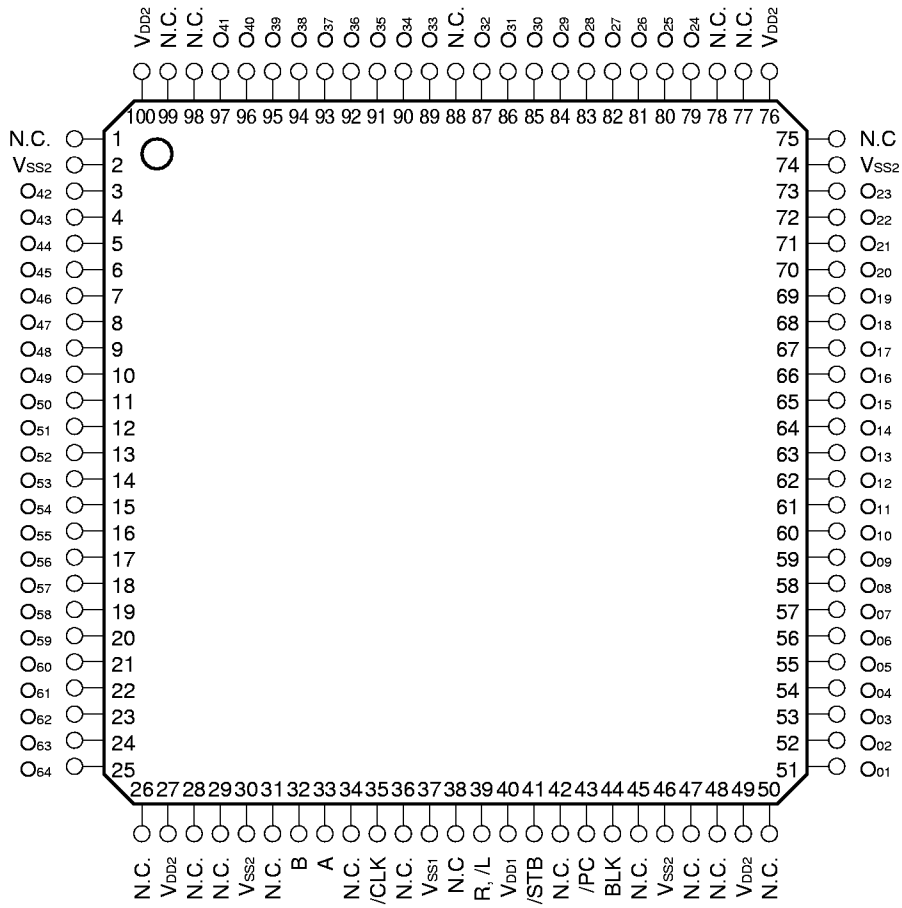
μPD16306BGF-3BA 100-pin plastic QFP (14 x 20 mm)



Cautions

1. **Be sure to leave pin 40 open because it is connected to the lead frame.**
2. **Be sure to use all the V_{DD1}, V_{DD2}, V_{SS1}, and V_{SS2} pins. Keep the V_{SS1} and V_{SS2} pins at the same voltage level.**
3. **Supply power to V_{DD1}, logic inputs, and V_{DD2} in this order to protect the device from destruction due to latch up. Turn off power in the reverse order.**
   Observe these power sequences even during a transition period.
4. **Since μPD16306B have a CMOS structure, be careful about electrical static destruction.**

★ **μPD16306BGC-9EU 100-pin plastic TQFP (fine pitch) (□ 14 mm)**



Cautions

1. **Be sure to use all the V_{DD1}, V_{DD2}, V_{SS1}, and V_{SS2} pins. Keep the V_{SS1} and V_{SS2} pins at the same voltage level.**
2. **Supply power to V_{DD1}, logic inputs, and V_{DD2} in this order to protect the device from destruction due to latch up. Turn off power in the reverse order.**
   Observe these power sequences even during a transition period.
3. **Since μPD16306B have a CMOS structure, be careful about electrical static destruction.**

PIN FUNCTIONS

Pin Symbol	Pin Name	Remark
/PC	Polarity reverse input	/PC = L: Reverses polarities of all outputs
BLK	Blank input	BLK = H: All outputs = H or L
/STB	Latch strobe input	Through at L, holds data at H
A	RIGHT data I/O	R, /L = H: A input, B output
B	LEFT data I/O	R, /L = L: B input, A output
/CLK	Clock input	Executes shift at falling edge
R, /L	Shift direction control input	Right shift mode at H A → O_1...O_{64} →B Left shift mode at L B → O_{64}...O_1 → A
O_1 to O_{64}	High-voltage output	80 V, 50 mA MAX.
V_{DD1}	Logic power supply	5 V ± 10 %
V_{DD2}	Driver power supply	10 to 70 V
V_{SS1}	Logic ground	Connected to GND of system
V_{SS2}	Power ground	Connected to GND of system
N.C.	Non connection	No connection. Be sure to leave pin 40 open.

TRUTH TABLE 1 (SHIFT REGISTER)

Input		I/O		Shift Register
R, /L	/CLK	A	B	
H	↓	Input	Output[Notes 1]	Right shift
H	H or L		Output	Hold
L	↓	Output[Notes 2]	Input	Left shift
L	H or L	Output		Hold

Notes 1. S_{63} is shifted to the position of S_{64} and output from B at the falling edge of the clock.

2. S_2 is shifted to the position of S_1 and output from A at the falling edge of the clock.

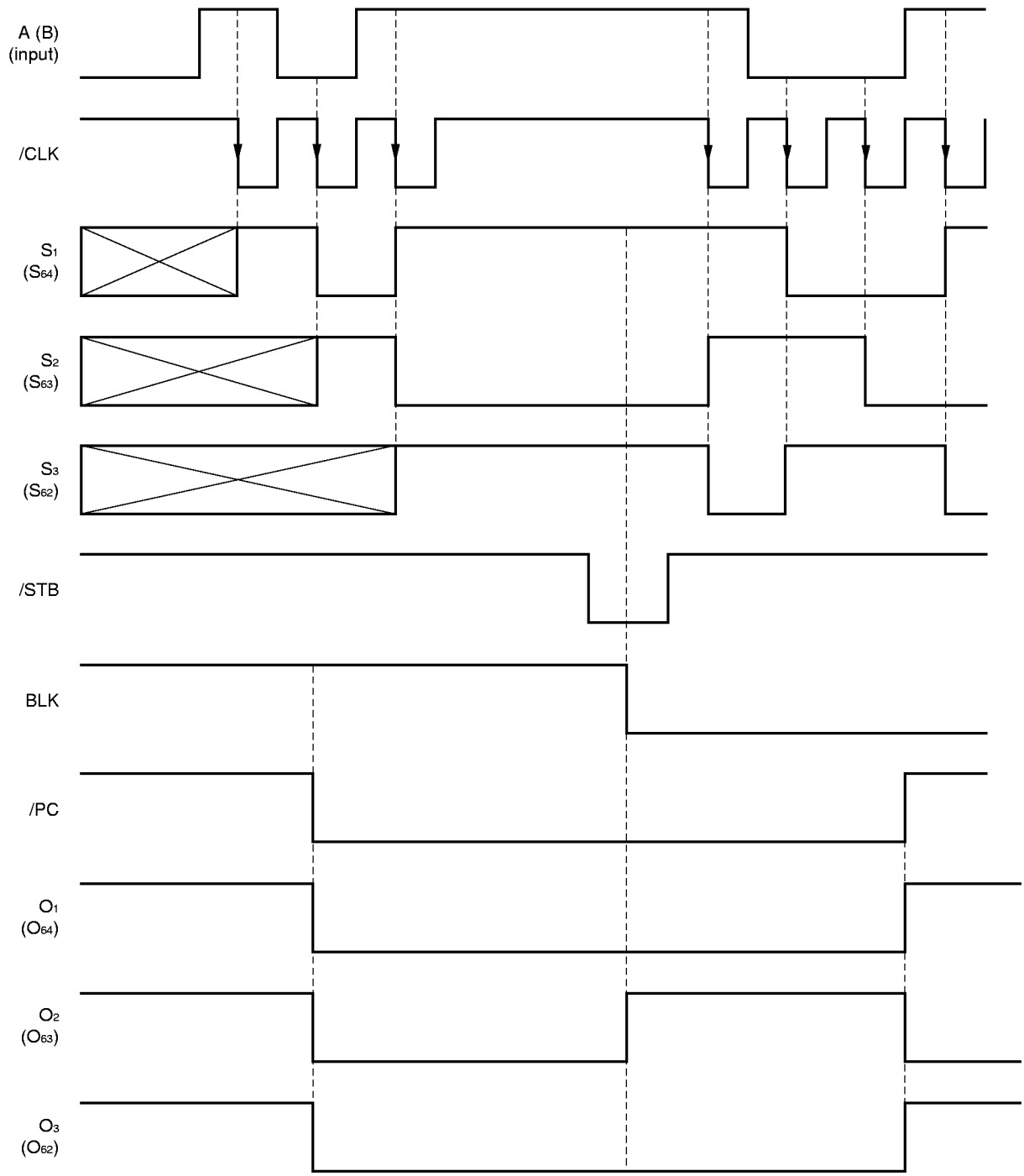
TRUTH TABLE 2 (LATCH AND DRIVER)

Input				Driver Output Stage
A (B)	/STB	BLK	/PC	
X	X	H	H	H (All driver outputs are H.)
X	X	H	L	L (All driver outputs are L.)
H	L	L	H	H
H	L	L	L	L
L	L	L	H	L
L	L	L	L	H
X	H	L	H	Outputs data immediately before /STB goes to H
X	H	L	L	Reverses and outputs data immediately before /STB goes to H

Remark X = H or L, H = high level, L = low level

TIMING CHART

( ): For R, /L = L



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating		Unit
Logic supply voltage	V_{DD1}	−0.5 to +7.0		V
Logic input voltage	V_I	−0.5 to V_{DD1} + 0.5		V
Logic output voltage	V_{O1}	−0.5 to V_{DD1} + 0.5		V
Driver supply voltage	V_{DD2}	−0.5 to +80		V
Driver output voltage	V_{O2}	−0.5 to V_{DD2} + 0.5		V
Driver output current	I_{O2}	±50		mA
★ Power dissipation	P_D	μPD16306BGF-3BA	1000	mW
		μPD16306BGC-9EU	800	
Operating ambient temperature	T_A	−40 to +85		°C
Storage temperature	T_{stg}	−65 to +150		°C

★ **Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.**

Recommended Operating Range (T_A = −40 to +85 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}	4.5	5.0	5.5	V
High-level input voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low-level input voltage	V_{IL}	0		0.2 V_{DD1}	V
Driver supply voltage	V_{DD2}	10		70	V
Driver output current	I_{OL2}			+40	mA
	I_{OH2}			−40	mA

Electrical Characteristics (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH1}	Logic I_{OH1} = –1.0 mA	0.9 V_{DD1}			V
Low-level output voltage	V_{OL1}	Logic I_{OL1} = 1.0 mA			0.1 V_{DD1}	V
High-level output voltage	V_{OH21}	O_1 to O_{64}, I_{OH2} = –1.0 mA	69			V
	V_{OH22}	O_1 to O_{64}, I_{OH2} = –10.0 mA	65			V
Low-level output voltage	V_{OL21}	O_1 to O_{64}, I_{OL2} = 5.0 mA			1.0	V
	V_{OL22}	O_1 to O_{64}, I_{OL2} = 40.0 mA			10	V
High-level input current	I_{IH}	V_I = V_{DD1}			1.0	μA
Low-level input current	I_{IL}	V_I = 0 V			–1.0	μA
High-level input voltage	V_{IH}	Logic	0.7 V_{DD1}			V
Low-level input voltage	V_{IL}	Logic			0.2 V_{DD1}	V
Static current dissipation	I_{DD11}	Logic, T_A = 25 °C			10	μA
	I_{DD12}	Logic, T_A = –40 to +85 °C			100	μA
	I_{DD21}	Driver, T_A = 25 °C			100	μA
	I_{DD22}	Driver, T_A = –40 to +85 °C			1000	μA

Switching Characteristics

(T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V, logic C_L = 15 pF, driver C_L = 50 pF)

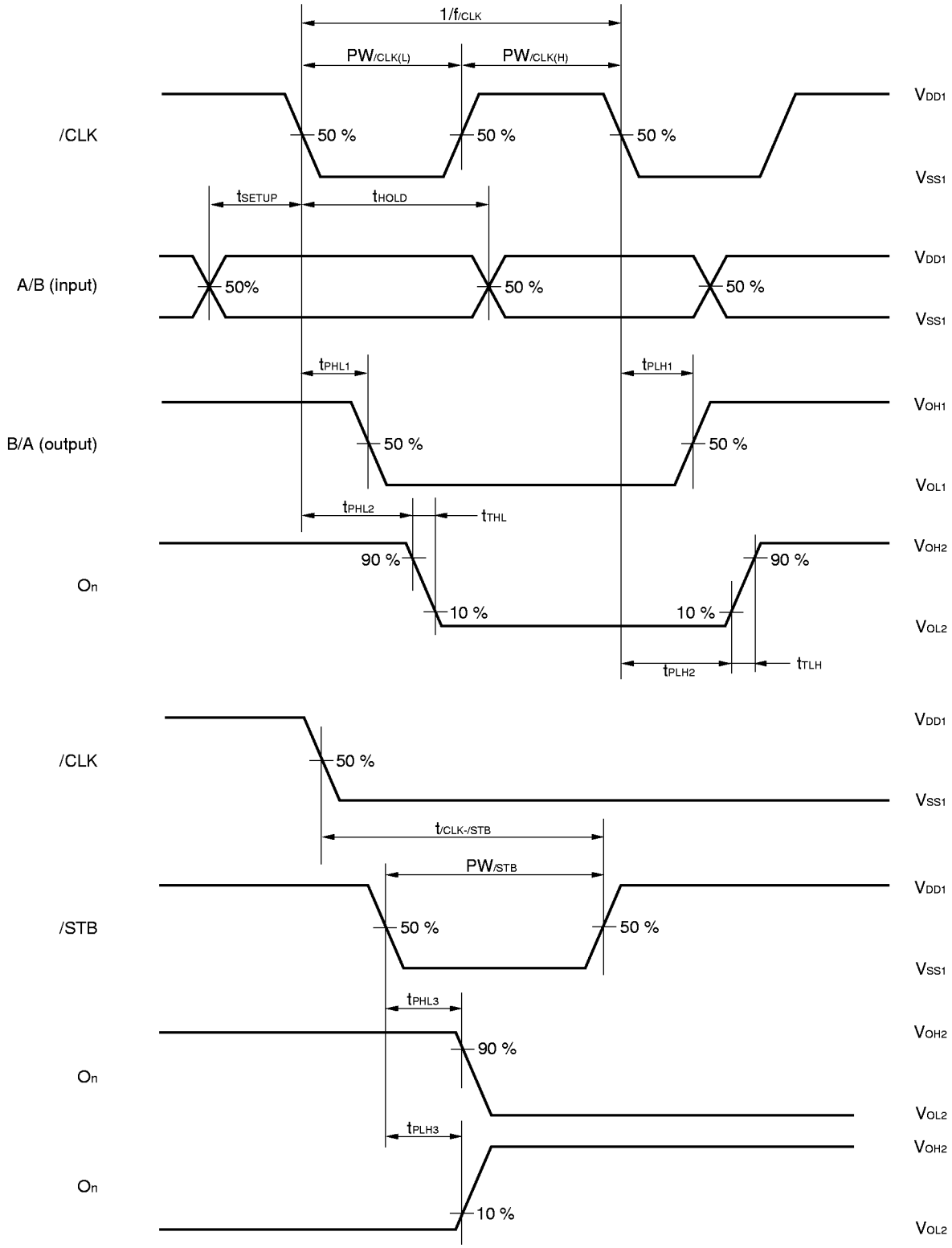
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Propagation delay time	t_{PHL1}	/CLK → A/B			50	ns
	t_{PLH1}				50	ns
	t_{PHL2}	/CLK → O_1 to O_{64}			160	ns
	t_{PLH2}				160	ns
	t_{PHL3}	/STB → O_1 to O_{64}			150	ns
	t_{PLH3}				150	ns
	t_{PHL4}	BLK → O_1 to O_{64}			145	ns
	t_{PLH4}				145	ns
	t_{PHL5}	/PC → O_1 to O_{64}			140	ns
	t_{PLH5}				140	ns
Rise time	t_{TLH}	O_1 to O_{64}			100	ns
Fall time	t_{THL}	O_1 to O_{64}			100	ns
Maximum clock frequency	$f_{MAX.}$	Duty = 50 %, data loading	20			MHz
		In cascade connection	16			MHz
Input capacitance	C_I				20	pF

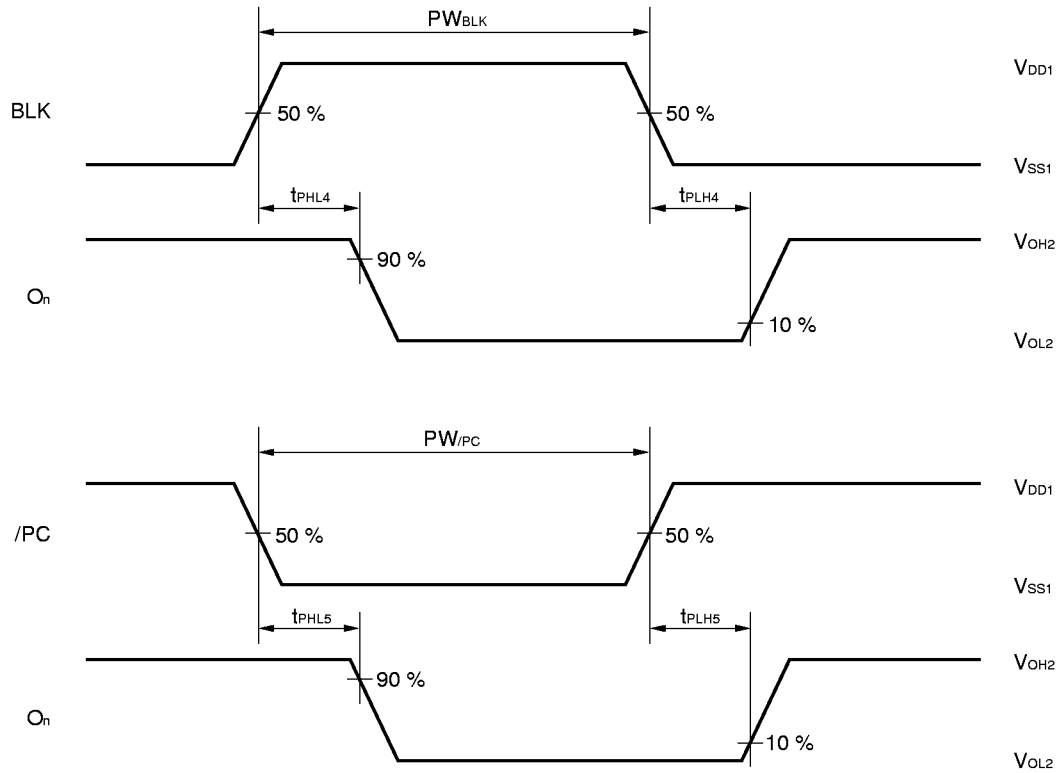
Timing Requirements (T_A = –40 to +85 °C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock pulse width	$PW_{/CLK\ (L),\ (H)}$		20			ns
Strobe pulse width	$PW_{/STB}$		20			ns
Blank pulse width	PW_{BLK}		200			ns
/PC pulse width	$PW_{/PC}$		200			ns
Data setup time	t_{SETUP}		10			ns
Data hold time	t_{HOLD}		10			ns
Clock-strobe time	$t_{/CLK-/STB}$	/CLK ↓ → /STB ↑	50			ns

Switching Characteristics Waveforms

Unless otherwise specified, $V_{IH} = V_{IL} = 0.5\ V_{DD1}$.

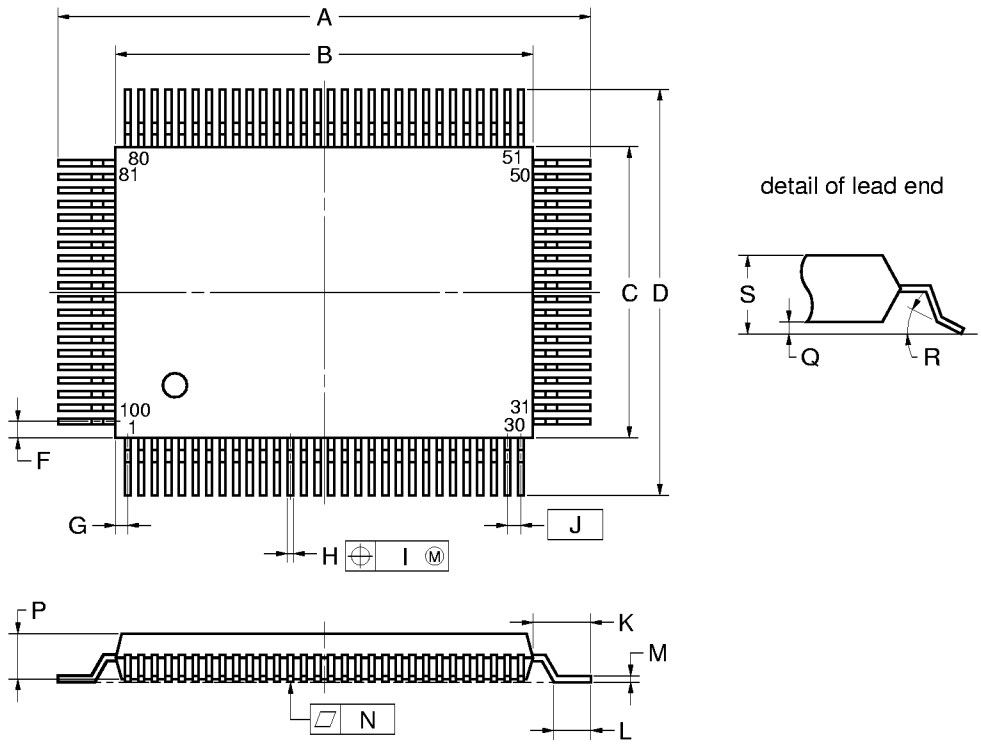



PWBLK
BLK
50 %
50 %
VDD1
VSS1
tPHL4
tPLH4
VOH2
90 %
On
10 %
VOL2
PW/PC
/PC
50 %
50 %
VDD1
VSS1
tPHL5
tPLH5
VOH2
90 %
On
10 %
VOL2

PACKAGE DRAWING

μPD16306BGF-3BA

100 PIN PLASTIC QFP (14×20)



NOTE

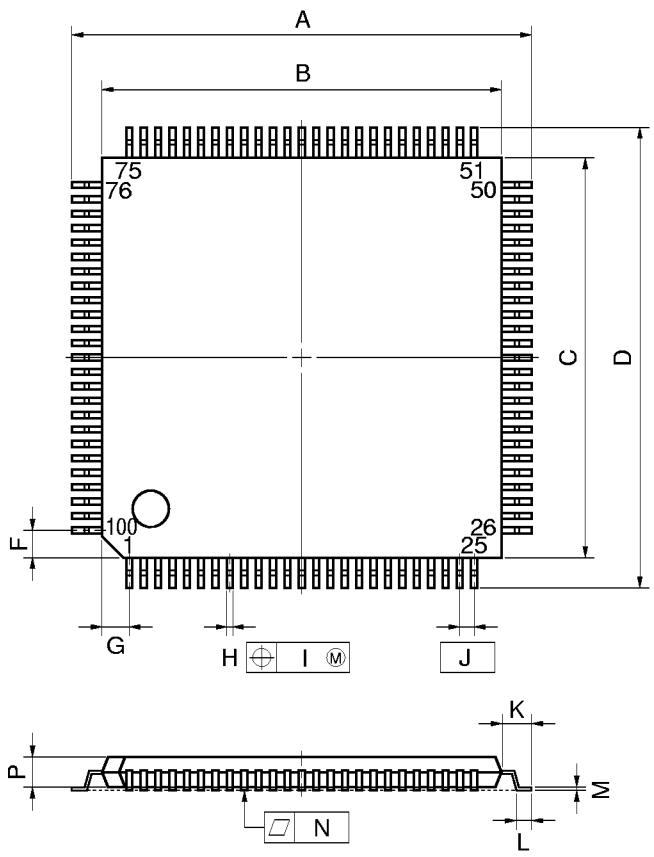
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

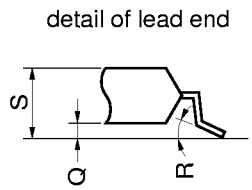
ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA-3

★ **μPD16306BGC-9EU**

100 PIN PLASTIC TQFP (FINE PITCH) (□14)





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.0±0.1	$0.039^{+0.005}_{-0.004}$
Q	0.1±0.05	0.004±0.002
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.27 MAX.	0.050 MAX.

S100GC-50-9EU-1

RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16306B.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Type of Surface Mount Device

μPD16306BGF-3BA: 100-pin plastic QFP (14 x 20 mm)

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 3	IR35-00-3
VPS	Peak temperature of package surface: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 1	VP15-00-1
Partial heating method	Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per one side of the device).	–

μPD16306BGC-9EU: 100-pin plastic TQFP (fine pitch) (□ 14 mm)

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak temperature of package suface: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 3 days (10 hours pre-baking is required at 125 °C afterwards)	IR35-103-2
VPS	Peak temperature of package surface: 215 °C or below, Reflow time: 25-40 seconds (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 3 days (10 hours pre-baking is required at 125 °C afterwards)	VP15-103-2
Partial heating method	Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per one side of the device).	–

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65% or less.

Caution Do not apply more than one soldering method at any one time, except for the partial heating method.

References

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)
Quality Grades on NEC Semiconductor Devices (C11531E)
Semiconductor Device Mounting Technology Manual (C10535E)