DATA SHEET

BLV100
UHF power transistor

Product specification

March 1993

Philips Semiconductors

PHILIPS

UHF power transistor BLV100

FEATURES

- Internal input matching to achieve high power gain
- Ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

DESCRIPTION

NPN silicon planar epitaxial transistor in a SOT171 envelope, intended for common emitter, class-AB operation in radio transmitters for the 960 MHz communications band. The transistor has a 6-lead flange envelope with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT171

PIN	DESCRIPTION
1	emitter
2	emitter
3	base
4	collector
5	emitter
6	emitter

PIN CONFIGURATION

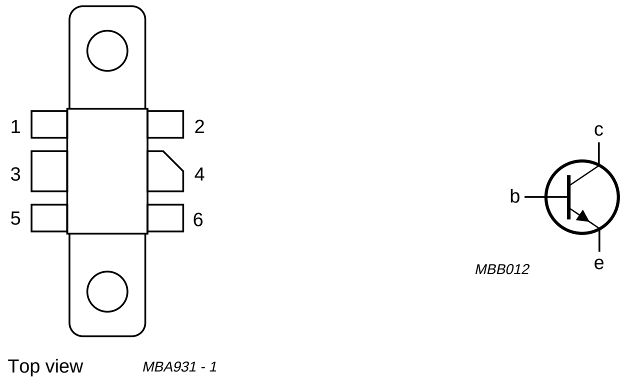


Fig.1 Simplified outline and symbol.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

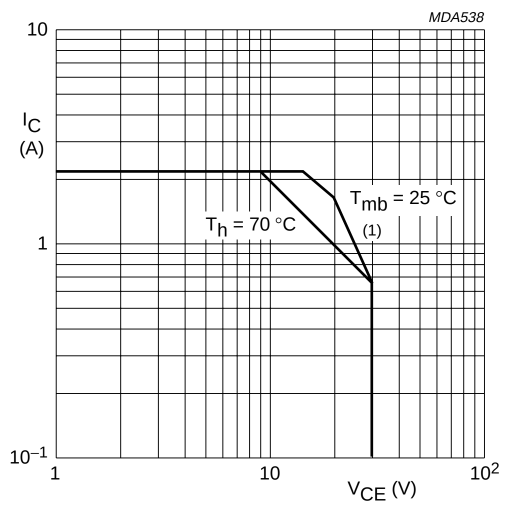
RF performance up to T_h = 25 °C in a common emitter class-AB test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_P (dB)	η_c (%)
c.w. class-AB	960	24	8	> 8	> 50

LIMITING VALUES

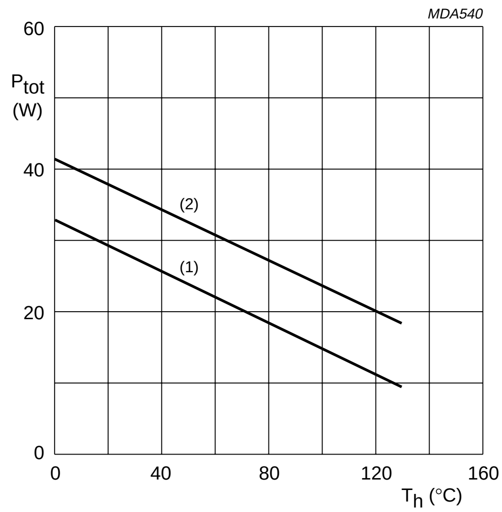
In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	collector-emitter voltage	peak value; $V_{BE} = 0$	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	4	V
I_C	collector current	DC or average value	–	2.25	A
I_{CM}	collector current	peak value f > 1 MHz	–	3.5	A
P_{tot}	total power dissipation	f > 1 MHz; T_{mb} = 25 °C	–	31	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction operating temperature		–	200	°C



(1) Second breakdown limit (temperature independent).

Fig.2 DC SOAR.



(1) RF operation.

(2) Short time operation during mismatch.

Fig.3 Power/temperature derating curve.

THERMAL RESISTANCE

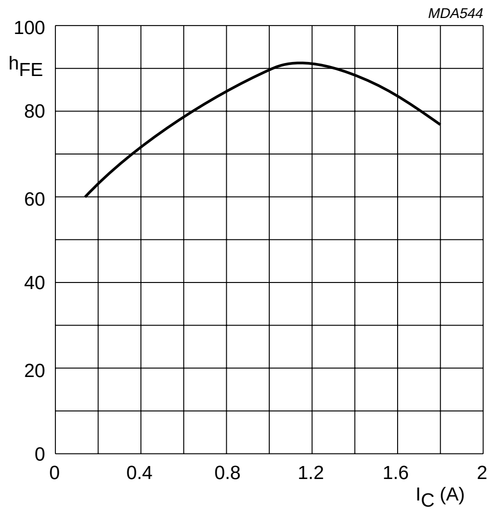
Dissipation = 31 W; T_{mb} = 25 °C.

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}mb(RF)}$	from junction to mounting base	5.6	K/W
$R_{th\ mb\text{-}h}$	from mounting base to heatsink	0.4	K/W

CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CES}$	collector-emitter breakdown voltage	V_{BE} = 0; I_C = 8 mA	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 60 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 4 mA	4	–	–	V
I_{CES}	collector-emitter leakage current	V_{BE} = 0; V_{CE} = 30 V	–	–	2	mA
h_{FE}	DC current gain	V_{CE} = 25 V; I_C = 0.6 A	20	75	–	‘
C_c	collector capacitance	V_{CB} = 25 V; $I_E = I_e$ = 0; f = 1 MHz	–	13.5	–	pF
C_{re}	feedback capacitance	V_{CE} = 25 V; I_C = 40 mA; f =1 MHz	–	8.4	–	pF
C_{c-f}	collector-flange capacitance		–	2	–	pF



V_{CE} = 25 V.

Fig.4 DC current gain as a function of collector current, typical values.

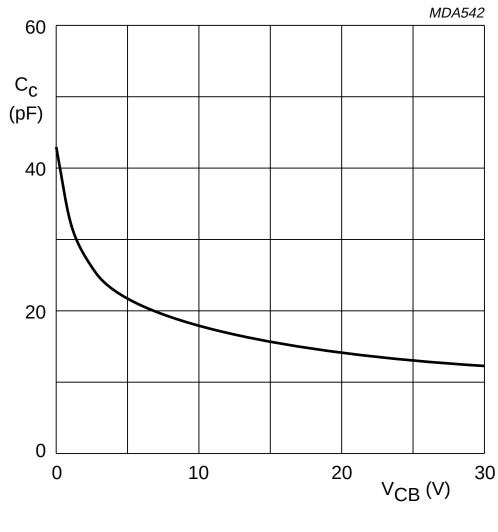


Fig.5 Output capacitance as a function of collector-base voltage, typical values.

APPLICATION INFORMATION

RF performance in a class-AB circuit; T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_P (dB)	η_c (%)
c.w. class-AB	960	24	20	8	> 8 typ. 9	> 50 typ. 55

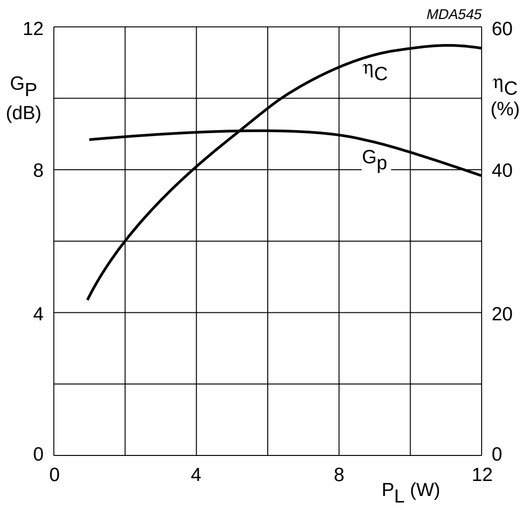


Fig.6 Gain and efficiency as functions of load power, typical values.

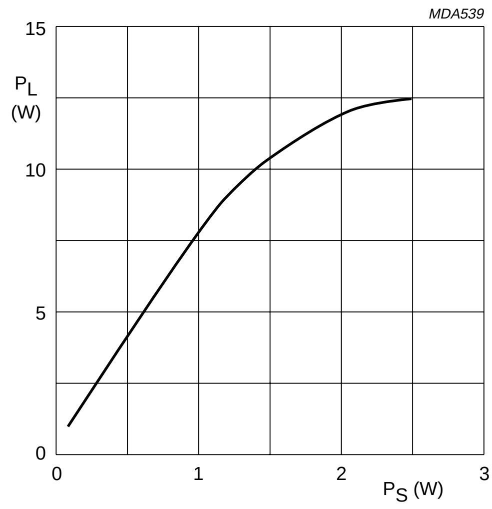


Fig.7 Load power as a function of drive power, typical values.

Ruggedness in class-AB operation

The BLV100 is capable of withstanding a load mismatch corresponding to VSWR = 10:1 through all phases, under the following conditions:

V_{CE} = 24 V, f = 960 MHz, and rated output power.

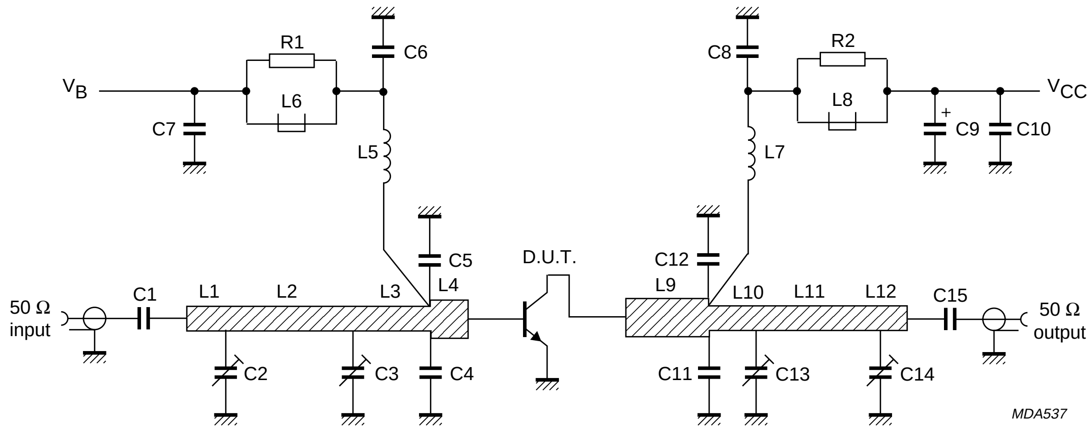


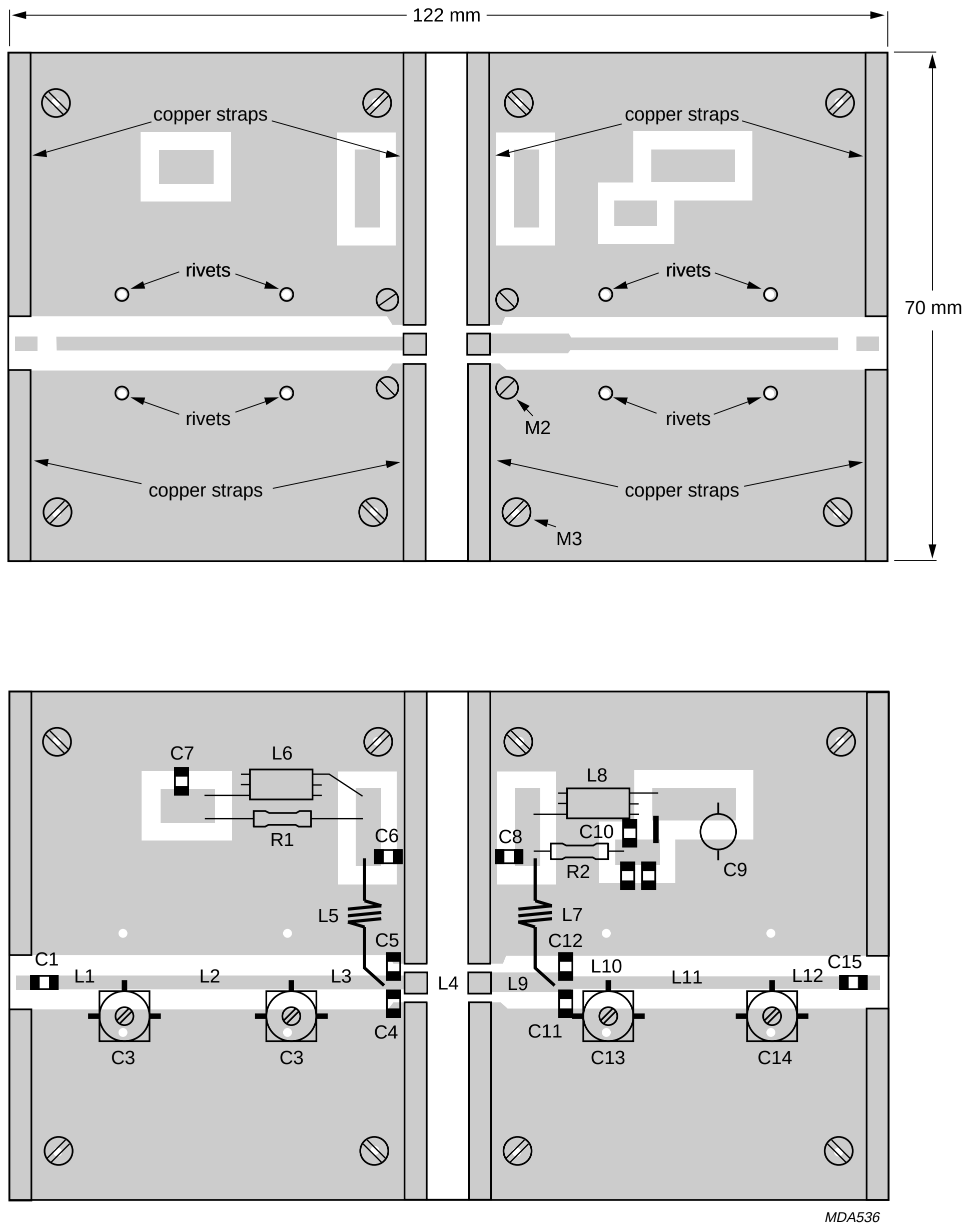
Fig.8 Class-AB test circuit at f = 960 MHz.

List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6, C7, C8, C15	multilayer ceramic chip capacitor	330 pF		
C2, C3, C13, C14	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C4, C5	multilayer ceramic chip capacitor (note 1)	5.1 pF		
C9	35 V solid aluminium capacitor	2.2 μF		2222 128 50228
C10	multilayer ceramic chip capacitor	3 × 100 pF in parallel		
C11, C12	multilayer ceramic chip capacitor (note 2)	6.2 pF		
L1, L12	microstrip (note 3)	50 Ω	9 × 2.4 mm	
L2, L11	microstrip (note 3)	50 Ω	23 × 2.4 mm	
L3	microstrip (note 3)	50 Ω	16 × 2.4 mm	
L4	microstrip (note 3)	43 Ω	3 × 3 mm	
L5	3 turns enamelled 0.8 mm copper wire		int. dia. 3 mm; length 5 mm; leads 2 × 5 mm	
L6, L8	grade 3B Ferroxcube wideband RF choke			4312 020 36642
L7	4 turns enamelled 0.8 mm copper wire		int. dia. 4 mm; length 5 mm; leads 2 × 5 mm	
L9	microstrip (note 3)	43 Ω	14.5 mm × 3 mm;	
L10	microstrip (note 3)	50 Ω	4.5 mm × 2.4 mm;	
R1, R2	0.4 W metal film resistor	10 Ω		2322 151 71009

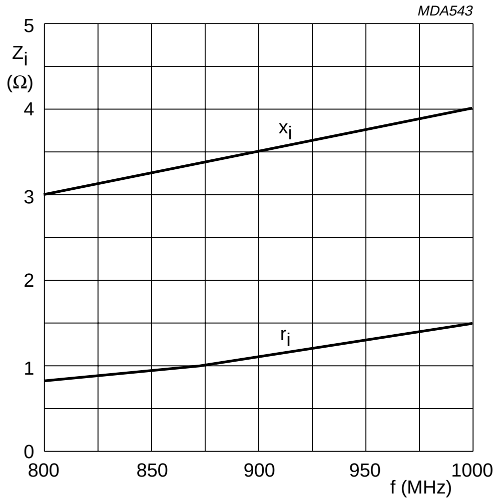
Notes

1. American Technical Ceramics capacitor type 100A, or capacitor of the same quality.
2. American Technical Ceramics capacitor type 100B, or capacitor of the same quality.
3. The microstrips are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness $^1\!/_{32}$ inch.



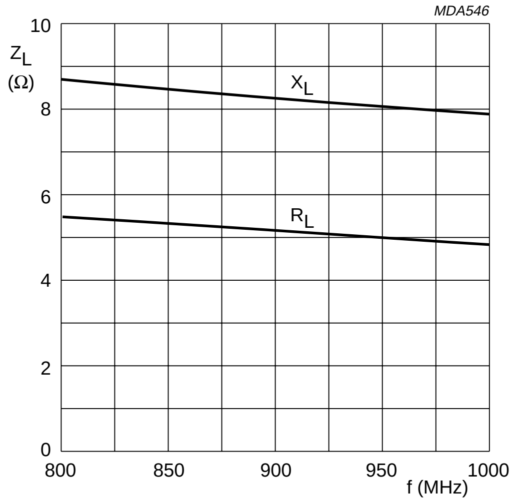
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by means of fixing screws, hollow rivets and straps around the board and under the emitters, to provide a direct contact between the component ground plane.

Fig.9 Component layout for 960 MHz test circuit.



V_{CE} = 24 V; I_{CQ} = 20 mA; P_L = 8 W.

Fig.10 Input impedance (series components) as a function of frequency, typical values.



V_{CE} = 24 V; I_{CQ} = 20 mA; P_L = 8 W.

Fig.11 Load impedance (series components) as a function of frequency, typical values.

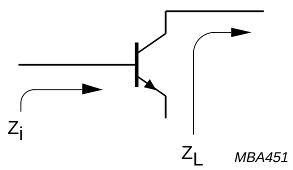
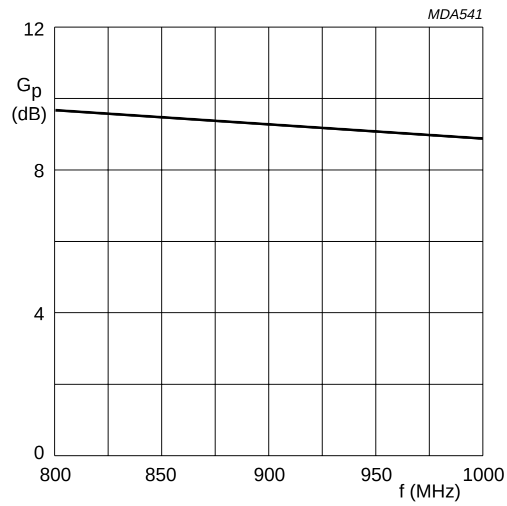


Fig.12 Definition of transistor impedance.

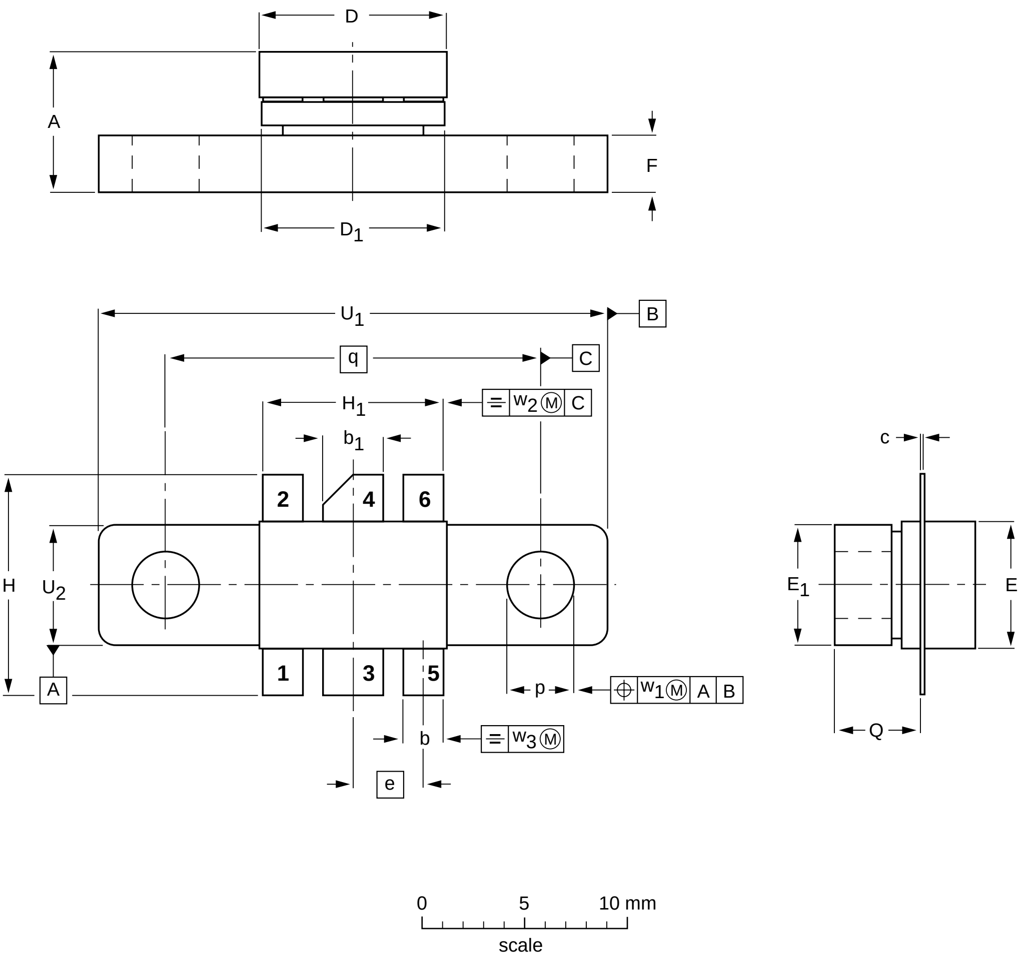


V_{CE} = 24 V; I_{CQ} = 20 mA; P_L = 8 W.

Fig.13 Power gain as a function of frequency, typical values.

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 6 leads **SOT171A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	6.81 6.07	2.15 1.85	3.20 2.89	0.16 0.07	9.25 9.04	9.30 8.99	5.95 5.74	6.00 5.70	3.58	3.05 2.54	11.31 10.54	9.27 9.01	3.43 3.17	4.32 4.11	18.42	24.90 24.63	6.00 5.70	0.51	1.02	0.26
inches	0.268 0.239	0.085 0.073	0.126 0.114	0.006 0.003	0.364 0.356	0.366 0.354	0.234 0.226	0.236 0.224	0.140	0.120 0.100	0.445 0.415	0.365 0.355	0.135 0.125	0.170 0.162	0.725	0.980 0.970	0.236 0.224	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT171A						97-06-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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