SONY

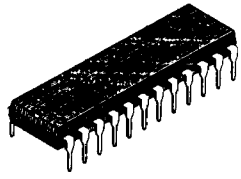
CXA1008P/1009P

High-speed Sample and Hold Amplifiers

Description

CXA1008P/1009P are bipolar IC's developed for the purpose of sample holding video signals and other signals at high-speed.

24pin DIP(Plastic)



Features

- Maximum sampling frequency
  - CXA1008P 35 MHz
  - CXA1009P 18 MHz
- Linearity 0.08% (Typ.)
- Clock input level ECL compatible
- Low power consumption
  - CXA1008P 680 mW (Typ.)
  - CXA1009P 420 mW (Typ.)

Structure

Bipolar silicon monolithic IC.

Function

High-speed hold circuit, wide band 6 dB amplifier, A/D reference power supply, A/D clock output circuit.

Applications

- A/D converter and other analog signal processing
- Other general applications.

Block Diagram

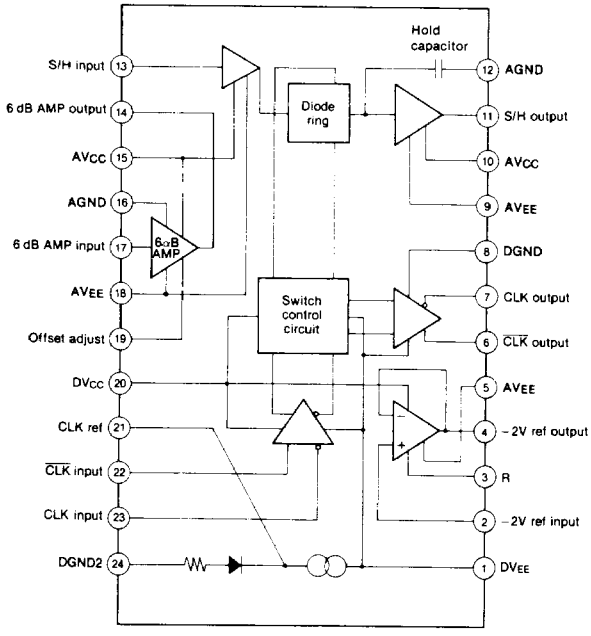


Fig. 1

E89641-HP

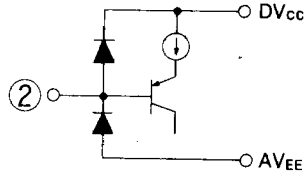
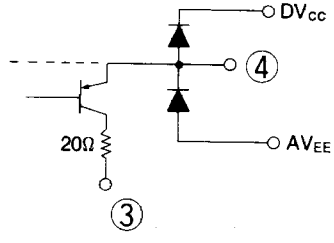
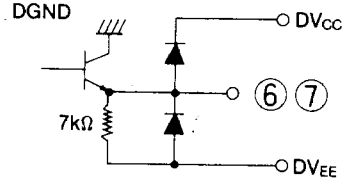
Absolute Maximum Ratings ($T_a = 25°C$)

•Supply voltage	V_{CC}	+5.5	V
	V_{EE}	−6.0	V
•Operating temperature	T_{opr}	−20 to +75	°C
•Storage temperature	T_{stg}	−55 to +150	°C
•Allowable power dissipation	P_D	1.2	W

Recommended Operating Conditions

•Supply voltage	V_{CC}	+4.75 to 5.25V
	V_{EE}	−4.75 to −5.45V

Pin Description

No.	Symbol	Equivalent circuit	Description
1	DV_{EE}		Digital V_{EE} (−5V)
2	−2V ref input		reference voltage input for A/D converter
3	R		Pulldown terminal for external R (30Ω typically)
4	−2V ref output		reference voltage output for A/D converter
5	AV_{EE}		Analog V_{EE} (−5V)
6	CLK output		CLK output for A/D converter
7	$\overline{CLK}$ output		$\overline{CLK}$ output for A/D converter
8	DGND		Digital GND
9	AV_{EE}		Analog V_{EE} (−5V)
10	AV_{CC}		Analog V_{CC} (+5V)

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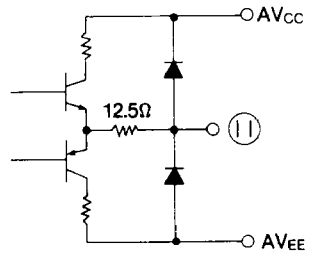
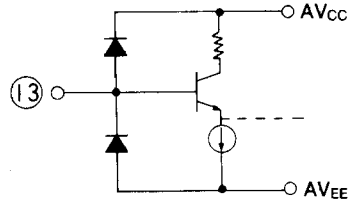
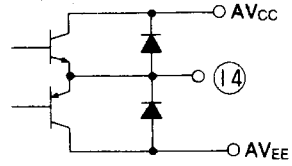
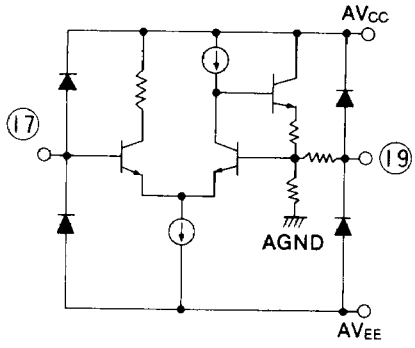
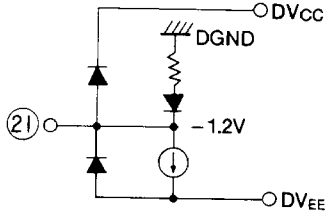
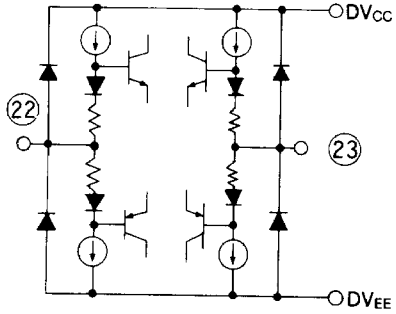
No.	Symbol	Equivalent circuit	Description
11	S/H output		S/H output
12	AGND		Analog GND
13	S/H input		S/H input
14	6dB AMP output		Olutput terminal of 6dB amplifier
15	AVCC		Analog VCC (+5V)
16	AGND		Analog GND

No.	Symbol	Equivalent circuit	Description
17	6dB AMP input		6dB AMP input
18	AV_{EE}		Analog V_{EE} (−5V)
19	offset adjust		6dB AMP DC offset adjust terminal
20	DV_{CC}		Digital V_{CC} (+5V)
21	CLK ref		CLK reference output
22	CLK input		CLK input (Note: connect to (21) PIN or input ECL CLK signal)
23	$\overline{CLK}$ input		$\overline{CLK}$ input (Note: input ECL $\overline{CLK}$ signal)
24	DGND		Digital GND

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CXA1008P

Electrical Characteristics ($Ta = 25°C$, $V_{CC} = +5V$, $V_{EE} = -5V$)
S/H section (see Fig. 3)

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Digital input voltage		V_{IH}	−0.9	−0.8		V
		V_{IL}		−1.6	−1.5	V
CLK Reference voltage (pin 21)		V_{CLKREF}	−1.3	−1.2	−1.1	V
Analog input voltage range	$\triangle V < 1.2V$ *1	V_{INS}	−3		3	V
Output voltage range		V_{outs}	−3		3	V
Power Supply		I_{CC}	48	60	78	mA
	without −2V ref.	I_{EE1}	48	60	78	mA
	with −2V ref. $R_{LI} = 50\Omega$ *2	I_{EE2}	80	100	125	mA
Input bias current	$-2V < V_{in} < 2V$	I_{Biass}		15	30	μA
Output impedance		Z_{OS}		20	40	Ω
Voltage gain ratio		G_{VS}	0.99	1.0	1.01	
Full power bandwidth	$V_{in} = 2V_{p\text{-}p}$ (−3dB)	BW		12		MHz
Power supply rejection ratio		SVR_s		−40		dB
Hold mode feed through	fin = 4MHz Vin = 1 Vp-p, CLK open	HMTH		−50	−40	dB
Clock leak	$V_{in} = 0V$	CL_{LEAK}		10	50	mV
Linearity	fin = 19.53kHz (10/512MHz) f_{CLK} = 10MHz *3	Lin		0.08	0.15	%
Hold mode droop	input voltage range, 0 to −2V	HMDR		2	20	mV/μs
Acquisition time	$\triangle V = 1.2V$	Taq		8	12	ns
Settling time	Settle to ±0.2% of F.S. see the Timing Chart	T_{set}		25		ns
DC offset voltage	$f_{CLK} = 5MHz$	V_{offset}		±15	±100	mV
Maximum sampling frequency		f_{CLKH}	35			MHz
Minimum sampling frequency		f_{CLKL}			5	MHz
Differential gain (D.G.)	Vin = NTSC 40 IRE mode ramp. f_{CLK} = 20MHz	DG		0.5	1.0	%
Differential phase (D.P.)		DP		0.5	1.0	deg

($R_{LI} = 50\Omega$. see Fig. 3)

CXA1009P

Electrical Characteristics ($Ta = 25°C$, $V_{CC} = +5V$, $V_{EE} = -5V$)
S/H section (see Fig. 3)

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Digital input voltage		V_{IH}	−0.9	−0.8		V
		V_{IL}		−1.6	−1.5	V
CLK Reference voltage (pin 21)		V_{CLKREF}	−1.3	−1.2	−1.1	V
Analog input voltage range	$\triangle V < 1.2V$ *1	V_{INS}	−3		3	V
Output voltage range		V_{outs}	−3		3	V
Power supply		I_{CC}	25	35	45	mA
	without −2V ref.	I_{EE1}	25	35	45	mA
	with −2V ref. $R_{LI} = 50\Omega$ *2	I_{EE2}	60	75	98	mA
Input bias current	$-2V < Vin < 2V$	I_{Biass}		9	18	μA
Output impedance		Zos		20	40	Ω
Voltage gain ratio		G_{vs}	0.99	1.0	1.01	
Full power bandwidth	$Vin = 2V_{p-p}$ (−3dB)	BW		6		MHz
Power supply rejection ratio		SVR_S		−40		dB
Hold mode feed through	fin = 4MHz Vin = 1 Vp-p, CLK open	HMTH		−50	−40	dB
Clock leak	Vin = 0V	CL_{LEAK}		10	50	mV
Linearity	fin = 19.53kHz (10/512MHz) f_{CLK} = 10MHz *3	Lin		0.08	0.15	%
Hold mode droop	input voltage range, 0 to −2V	HMDR		2	10	mV/μs
Acquisition time	$\triangle V = 1.2V$	Taq		12	20	ns
Settling time	Settle to ±0.2% of F.S. see the Timing Chart	T_{set}		36		ns
DC offset voltage	f_{CLK} = 5MHz	V_{offset}		±15	±100	mV
Maximum sampling frequency		f_{CLKH}	18			MHz
Minimum sampling frequency		f_{CLKL}			2	MHz
Differential gain (D.G.)	Vin = NTSC 40 IRE more ramp f_{CLK} = 15MHz	DG		0.5	1.0	%
Differential phase (D.P.)		DP		0.5	1.0	deg

*1 $\triangle V$ is voltage change during one sampling period.
*2 Power consumption is $I_{CC} \times 5V + I_{EE1} \times 5V + 40mA \times 1.8V$.
*3 Input voltage waveform

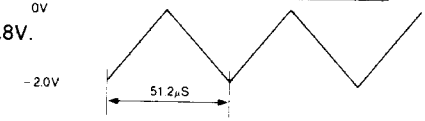

Fig. 2

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6dB amp section (see Fig. 3)

Item	Condition	Symbol	CXA1008P			CXA1009P			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Intput voltage range	*3	V_{INA}	−1.3		+0.8	−1.3		+0.8	V
Band width (−3dB)	V_{in} = IV_{pp}	W	45	55		15	25		MHz
Input bias current	−1V < V_{in} < 1V	$I_{Bias\ A}$		9	20		5	10	μA
Output impedance		Z_{OA}		4	10		4	10	Ω
Voltage gain	*4	G_{VA}	5.1	6.0	6.9	5.1	6.0	6.9	dB
Power supply rejection ratio		SVR_A		−40			−40		dB

*3 2ndary harmonic: −40dB f_{in} = 3.58MHz
*4 f_{in} = 3.58MHz V_{in} = $1V_{p\text{-}p}$

CLK OUT section (see Fig. 3)

Item		Condition	Symbol	CXA1008P			CXA1009P			Unit
				Min.	Typ.	Max.	Min	Typ.	Max.	
Output voltage	Amplitude	R_{L2} = 1.5 KΩ see Fig. 3	V_{CLK}	0.2	0.3	0.4	0.2	0.3	0.4	V
	Low level		V_{CLKL}	−1.2	−1.1	−0.9	−1.2	−1.1	−0.9	V
Rise time			tr		7	10		7	10	ns
Fall time			tf		5	8		5	8	ns
CLK Delay 1			τ_{D1}	20	28	34	36	38	45	ns
CLK Delay 2			τ_{D2}	14	22	28	24	26	33	ns

$-2V_{ref}$ amp section (see Fig. 3)

Item	Condition	Symbol	CXA1008P			CXA1009P			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Voltage gain ratio	V_{ref} = −2V R_{LI} = 50Ω	G_{VR}	0.9	1.0	1.1	0.9	1.0	1.1	
Input bias current	−3V < V_{in} < 0V	$I_{Bias\ R}$		5	10		5	10	μA
Output impedance		Z_{OR}		2	10		2	10	Ω

Electrical Characteristics Test Circuit

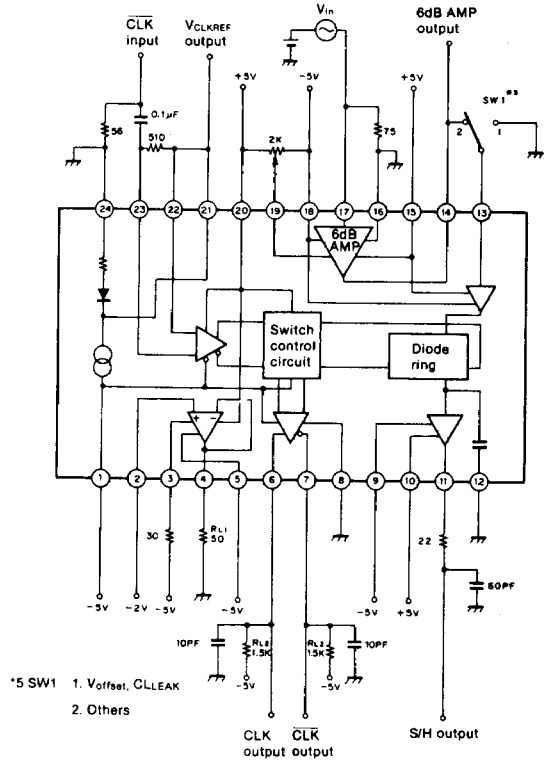


Fig. 3

Timing Chart

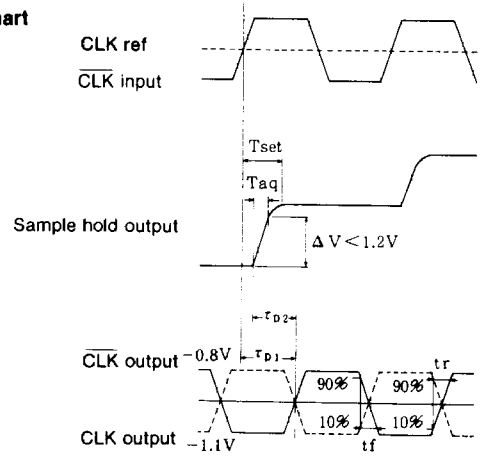


Fig. 4

Description of Functions

CXA1008P/1009P are the monolithic ICs incorporating a high-speed sample hold circuit, a wide band 6 dB amp, reference power supply for A/D converter, and a clock output section, and operate up to a sampling frequency of 35/18 MHz.

CXA1008P/1009P can compose in 20/15 MS/s A/D converter system in combination with a CX20052A. CXA1008P/1009P form, with the input of a single phase or 2-phase ECL clock input, a new sampling signal. For this reason, the sampling period remain unchanged even when the frequency or duty of the input sampling CLK signal changes.

•Wide band 6 dB AMP.

In-phase amp with a band width over 45/15 MHz amplifies ordinary TV signal (1Vp-p) to a 2Vp-p signal which gives the highest accuracy when processed in CX20052A.

•CLK output section

When used in combination with an A/D converter such as CX20052A, the CLK timing between the S/H circuit and the A/D converter needs to be adjusted, and up to 20/15 MHz, CXA1008P/1009P generate CLK timing signals for driving the A/D converter, and output 2-phase CLK at 300 mVp-p from pins 6 and 7. With this output, no separate CLK is required to combine with an A/D converter.

•CXA1008P/1009P incorporate a buffer amp to provide a reference voltage for the A/D converter.

Application Circuit

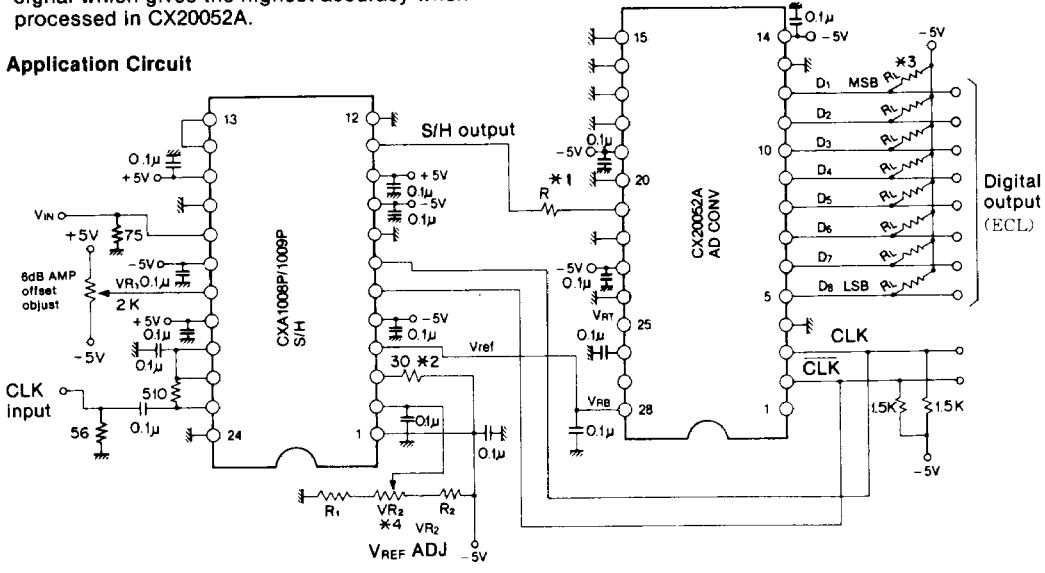


Fig. 5 Connection of CXA 1008P/1008P with CX20052A (1)

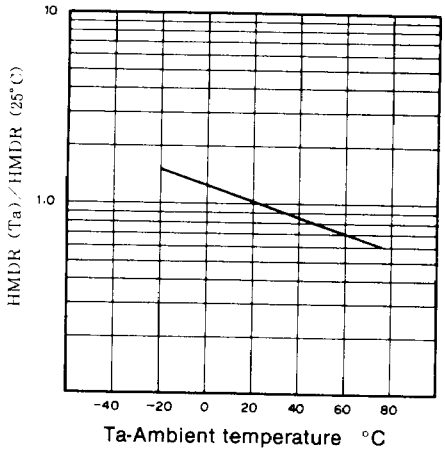
*1 R is a ringing preventing resistor. Select between 10 to 50Ω
*2 Pulldown R for V_{ref}
*3 R_L = 4.3kΩ
*4 R_1 = 1kΩ, VR_2 = 2kΩ, R_2 = 2kΩ

Notes on Application

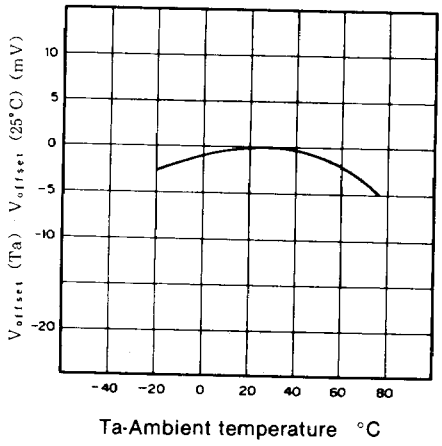
1. Unless sufficiently stable power supply and GND voltage in the high-frequency range are used, the device characteristics deteriorates. For this reason, bring the power supply bypass capacitor as near to this IC as possible, and make the pattern to the power supply and to the earth terminal as wide as feasible.
2. To reduce CLK leak, use waveforms similar to sine waves as far as possible, up to the CLK input. For satisfactory operation, a CLK input ampritude of around 300mV is enough.
3. When the S/H input deviates over 1.2V during one sampling period, the output may contain errors.

Changes in Characteristics with Temperature

Hold Mode Droop Rate

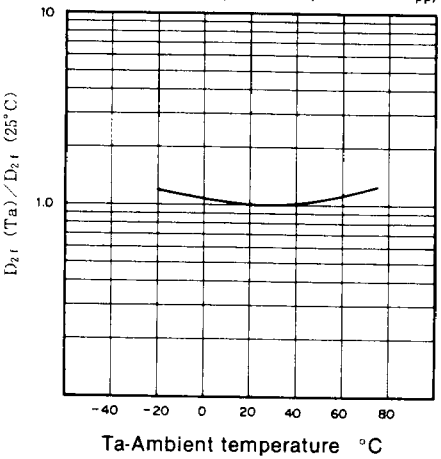


Offset Voltage Between S/H Input & Output

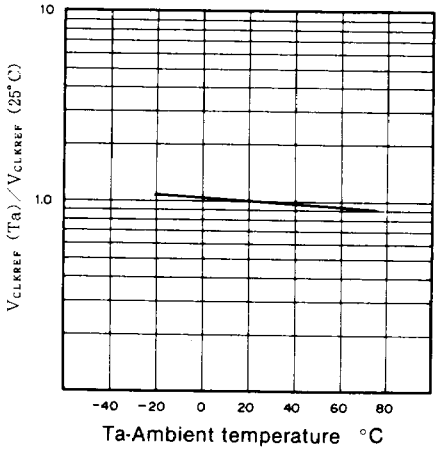


6dB AMP 2ndary Harmonic Level

(3.58MHz, Vin = $1V_{pp}$)



CLK Ref Voltage



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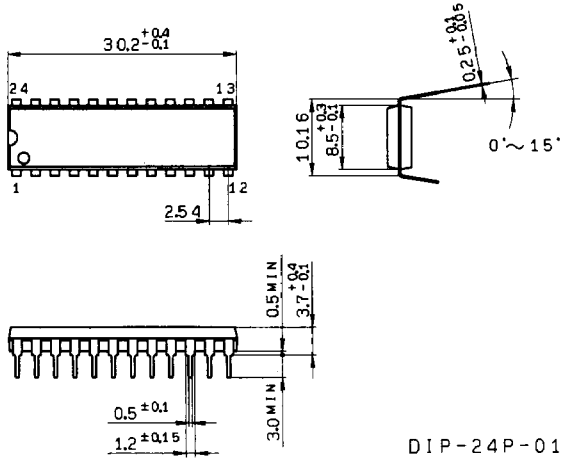
Package Outline Unit : mm

24pin DIP(Plastic) 400mil 2.0g



DIP-24P-01

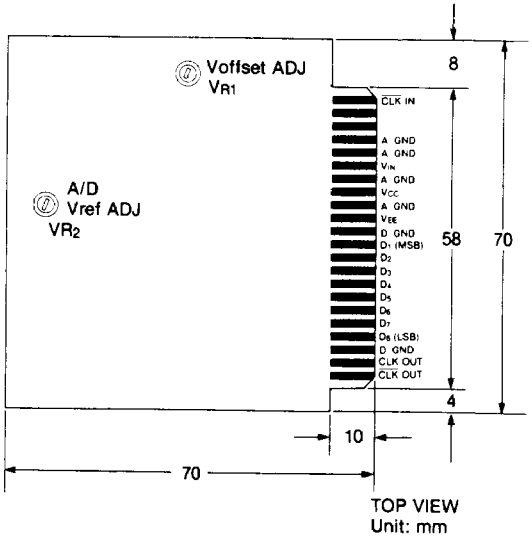
8bit, 20/15MHz A/D Converter Evaluation Board with CXA1008P/CXA1009P S/H.

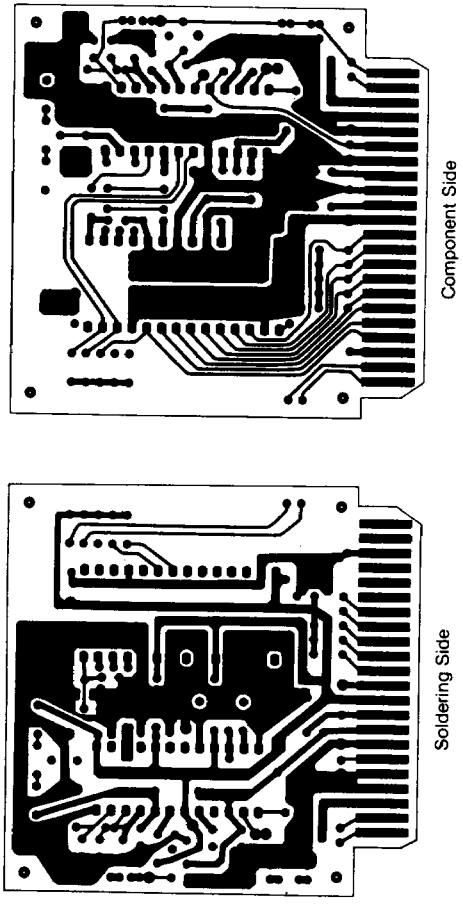
Description

CX20052A PCB-3A/3B is an 8 bit A/D converter board for video signal processing. A high speed S/H IC CXA1008P/1009P and a high speed 8 bit A/D converter CX20052A are assembled on single small printed circuit board.
CX20052A PCB-3A with CXA1008P mounted, operates up to 20 MHz of conversion rate, and CX20052A PCB-3B with CXA1009P mounted, operates up to 15 MHz of conversion rate.

Features

•Resolution	8 bit ± 1/2 LSB
•Conversion rate	20 MHz CX20052A PCB-3A
	15 MHz CX20052A PCB-3B
•Analog input level	1Vp-p
•Digital output level	ECL level
•Power supply	±5V





CX20052A PCB-3A/3B Pattern

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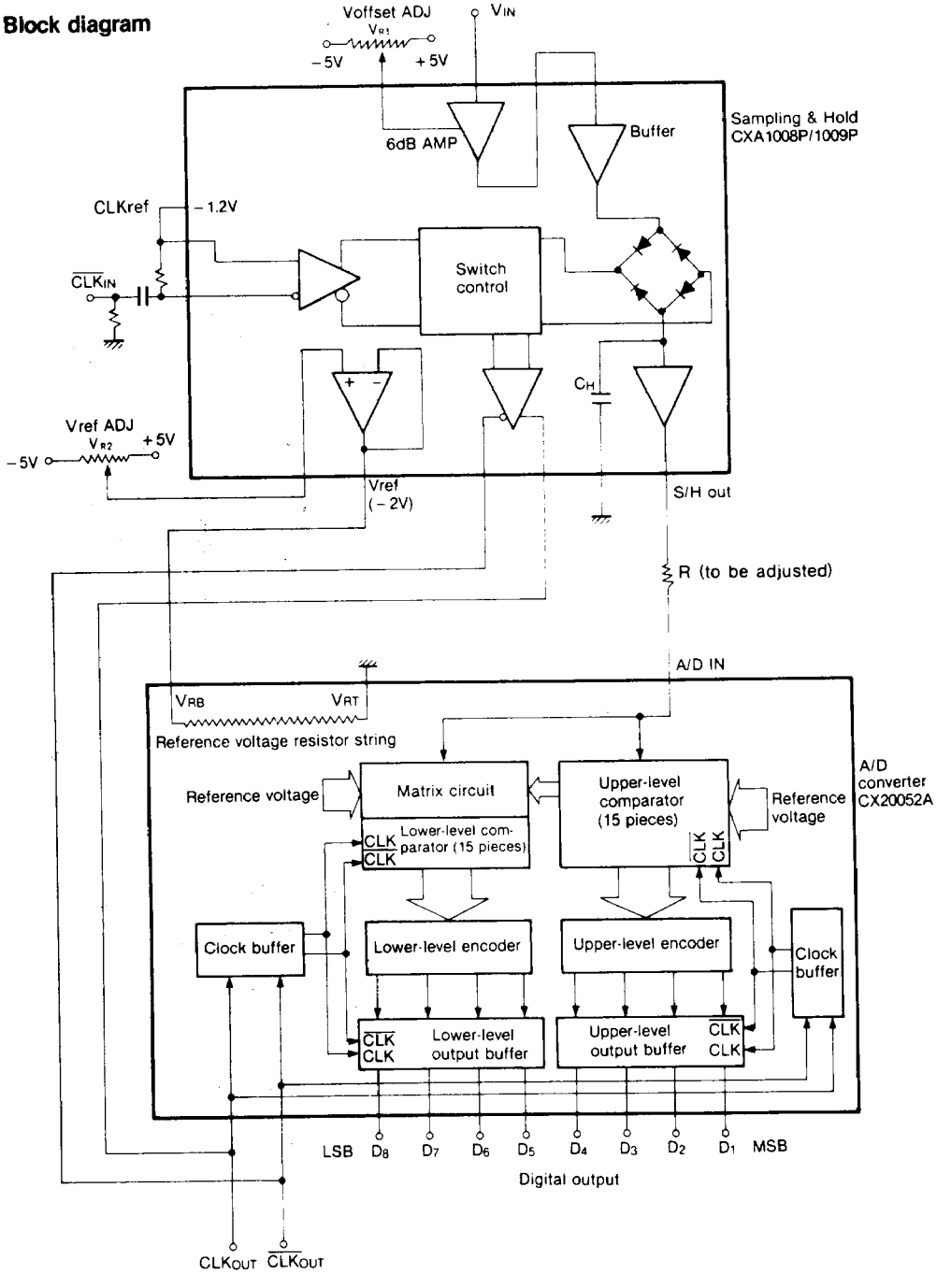
1. Block diagram



2. Characteristics

1. Supply Voltage

($Ta = 25°C$, $V_{EE} = -5V$, $V_{CC} = 5V$)

Item			Symbol	Min	Typ	Max	Unit
V_{CC}	+5V	CX20052A	I_{CC}		70	80	mA
V_{EE}	−5V	PCB-3A	I_{EE}		220	240	mA
		CX20052A	I_{CC}		50	60	mA
		PCB-3B	I_{EE}		200	220	mA

2. Analog Input (V_{IN})

Item	Symbol	Min	Typ	Max	Unit
AC Input Voltage Amplitude	V_{IN}			1	V
Offset Adjustable Range		±1.5	±2.0		V
Input Impedance	Z_{in}				
CX20052APCB-3A			75		Ω
CX20052APCB-3B			75		Ω

3. Digital Input ($\overline{CLK}$ IN)

Item	Symbol	Min	Typ	Max	Unit
Input Voltage (p-p)	V_{CLK}	0.3	0.8	4	V
Input Impedance	Z_{INCL}		50		Ω

4. Digital Output (D1 ~ D8) (1.5kΩ to V_{EE})

Item	Symbol	Min	Typ	Max	Unit
Output Voltage	V_{OH}	−0.90	−0.75		V
	V_{OL}		−1.50	−1.35	V

5. Clock Output (CLK_{OUT}, $\overline{CLK}_{OUT}$) (See timing chart)

Item		Symbol	CX20052A PCB-3A			CX20052A PCB-3B			Unit
			Min	Typ	Max	Min	Typ	Max	
Output voltage	Amplitude	V_{CLK}	0.2	0.3	0.4	0.2	0.3	0.4	V
	Low Level	V_{CLKL}	−1.2	−1.1	−0.9	−1.2	−1.1	−0.9	V
Rise time		tr		6	10		6	10	ns
Fall time		tf		12	15		12	15	ns
CLK Delay		τ_F	20	28	34	36	38	45	ns

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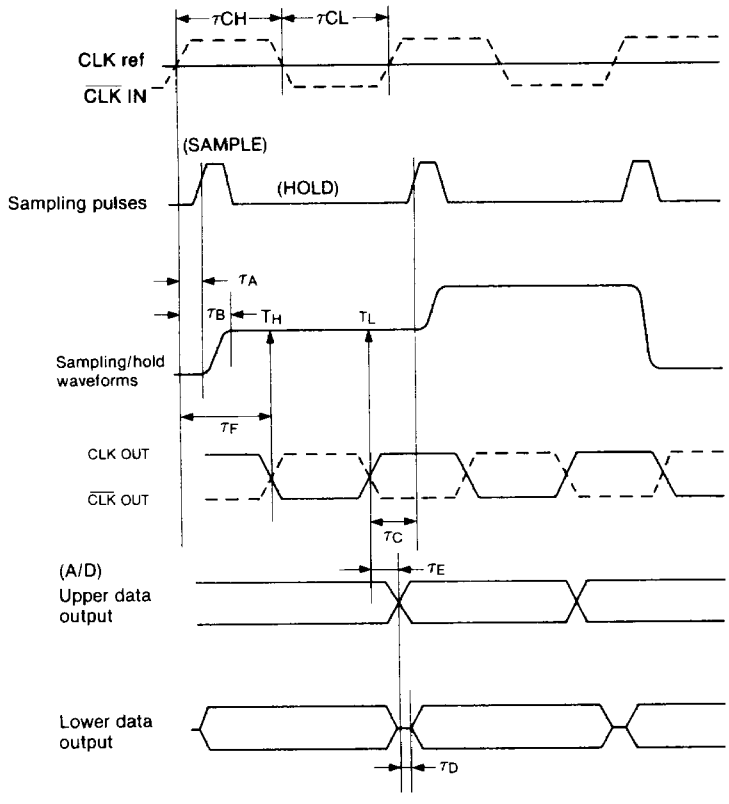
3. Timing Chart



T_H shows a timing when the A/D latches upper 4 bits.
T_L shows a timing when the A/D latches lower 4 bits.

Item	Symbol	CX20052A PCB-3A			CX20052A PCB-3B			
		Min	Typ	Max	Min	Typ	Max	Unit
Clock in	τCH		25			33		ns
	τCL		25			33		ns
Sampling delay	τA		6			12		ns
	τB		25			36		ns
Clock out	τF	20	28	34	36	38	45	ns
Data delay	τE			8			8	ns
	τD			4			4	ns

4. Adjustment

(1) Offset Voltage (Voffset ADJ)
VR_1 should be adjusted so that the S/H output meets the input voltage range of the A/D (0 to −2V).
(2) A/D reference voltage (Vref ADJ).
The reference voltage of the A/D (TP5) is to be −2V. VR_2 should be adjusted.

5. Output Data Format

The input of the A/D converter IC (S/H out) is quantized in 8 bit within the reference voltage range of V_{RT} and V_{RB}. The V_{RT} and V_{RB} are set at 0V and −2V respectively on the printed circuit board.

Step	A/D input signal voltage		Digital output code
			MSB LSB
	over	0. 0 0 0 0 V	1 1 1 1 1 1 1 1
0 0 0		0. 0 0 0 0 V (V_{RT})	1 1 1 1 1 1 1 1
.		.	.
.		.	.
.		.	.
1 2 7		−0. 9 9 6 1 V	1 0 0 0 0 0 0 0
1 2 9		−1. 0 0 3 9 V	0 1 1 1 1 1 1 1
.		.	.
.		.	.
.		.	.
2 5 5		−2. 0 0 0 0 V (V_{RB})	0 0 0 0 0 0 0 0
	under	−2. 0 0 0 0 V	0 0 0 0 0 0 0 0

6. Note on application

(1) Although the pull down resistors (RL: 4.3kΩ) are mounted on the PCB, additional pull down is recommended in an external circuit. The output current at the A/D output terminal should not exceed 10 mA.
(2) Digital output data should be latched by an external circuit to achieve a rated performance. Output data can be latched at a rising edge of CLK_{OUT}.
CLK_{OUT} AND $\overline{CLK}_{OUT}$ should be reshaped by an ECL line receiver such as MC10116 in an external circuit.
(3) The reference voltage is derived from the V_{EE} by a simple resistor dividing network. The power supply (±5V) should be stabilized to reduce voltage drift of the reference voltage.
(4) To reduce CLK leak, use waveforms similar to sine waves as far as possible up to the CLK input. For satisfactory operation, a CLK input amplitude of around 300m V_{PP} is enough.
(5) When the S/H input deviates over 1.2V during one sampling period, the output may contain errors.

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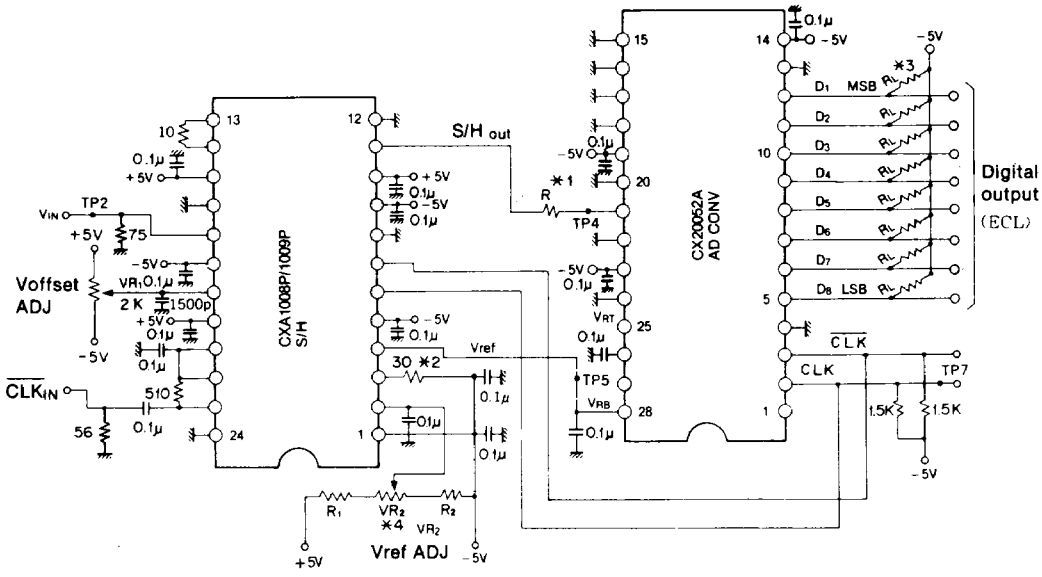
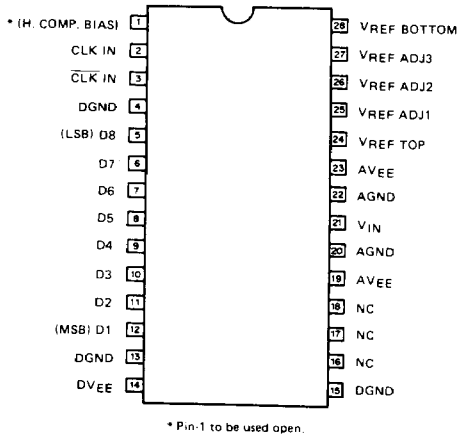
CX20052A PCB-3A/3B Circuit



*1. R is a ringing preventing resistor. Select between 10 to 50Ω according to pattern length.
*2. Pulldown R for Vref.
*3. $R_L = 4.3k\Omega$
*4. $R_1 = 2k\Omega, VR_2 = 2k\Omega, R_2 = 1k\Omega$

Additional Information on CX20052A

Pin Configuration (Top View)

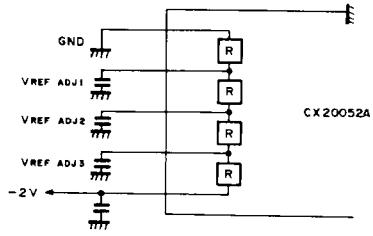


* Pin-1 to be used open.

Pin Description

No.	Symbol	Description
1	H-COMP BIAS	Pin connected to internal comparator. It should not be connected to outer circuit.
2	CLK IN	CLOCK input pin.
3	$\overline{\text{CLK IN}}$	$\overline{\text{CLOCK}}$ input pin.
4	DGND	Ground pin of digital circuit.
15	DGND	Ground pin of digital circuit.
17	NC	Non-connection.
18	NC	
24	$V_{REF\ (T)}$	Reference voltage pin. (0V)
25	$V_{REF\ ADJ1}$	Reference voltage adjusting pin. (Usually it should be connected to GND through 0.047 μF capacitor.)
26	$V_{REF\ ADJ2}$	
27	$V_{REF\ ADJ3}$	
28	$V_{REF\ (B)}$	Reference voltage pin. (−2.0V)

(*) Reference resistors have adjusting pins as shown below. Usually these pins are connected to GND through 0.047 μF capacitors. When an adjustment is required, they should be connected to GND or $V_{REF\ (B)}$ through resistors.



Output Coding

Step	Input signal voltage	Output digital code
		MSB LSB
000	0.0000V	11111111
.	.	.
.	.	.
.	.	.
127	−0.9961V	10000000
128	−1.0039V	01111111
129	−1.0118V	01111110
.	.	.
.	.	.
.	.	.
255	−2.0000V	00000000

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