KS0641

6 BIT 300 / 309 CHANNEL TFT-LCD SOURCE DRIVER

November. 1999.

Ver. 0.1

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KS0641 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Aug.1999
0.1	The content of page 21 has been modified	Nov.1999

CONTENTS

INTRODUCTION

The KS0641 is a 300 channel or 309 channel output, TFT-LCD source driver for 64 gray scale displays. Data input is based on digital input consisting of 6 bits by 3 dots, which can realize a full-color display of 260,000 colors by output of 64 values gamma-corrected.

This device has an internal D/A (Digital-to-Analog) converter for each output and 9 or 11 external power supplies.

KS0641 can be adopted to larger panel, and SHL (Shift Direction Selection) pin makes use of the LCD panel connection conveniently. Maximum operation clock frequency is 55 MHz at a 3.3 V logic operation. It can be applied to the TFT-LCD panel of SVGA, XGA standards.

FEATURES

- TFT active matrix LCD source driver LSI
- 64 gray scale is possible through 9 or 11 external power supply and D/A converter
- Line inversion display is possible
- CMOS level input
- Compatible with gamma-correction
- Logic supply voltage: 3.0 - 5.5 V
- LCD driver supply voltage: 3.0 - 5.5 V
- Output dynamic range: 2.6 - 5.1 Vp-p
- Maximum operating frequency: fMAX = 55 MHz (internal data transmission rate at 3.3 V operation)
- Output: 300 / 309 outputs
- TCP

BLOCK DIAGRAM

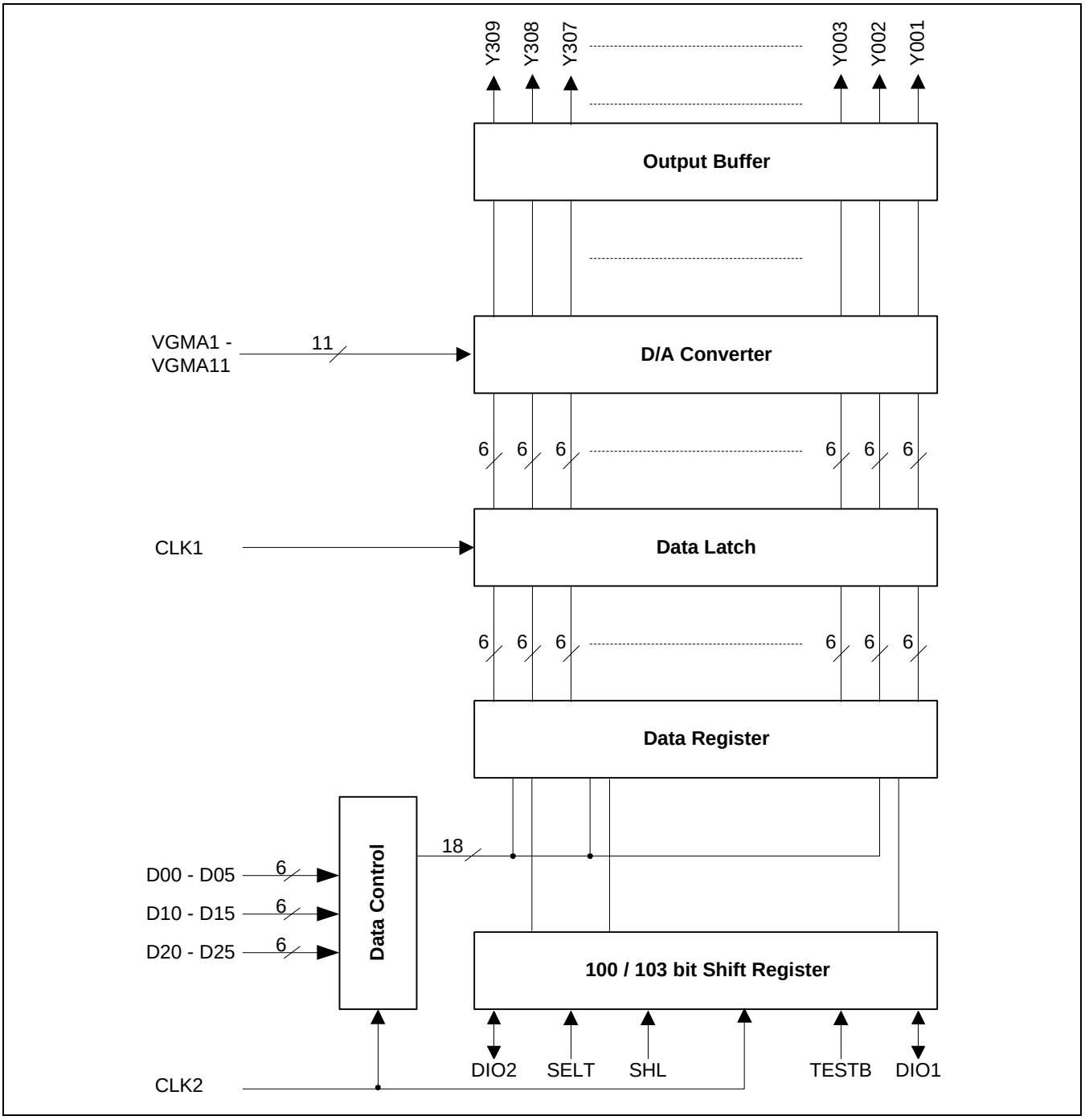

Figure 1. KS0641 Block Diagram

PIN ASSIGNMENTS

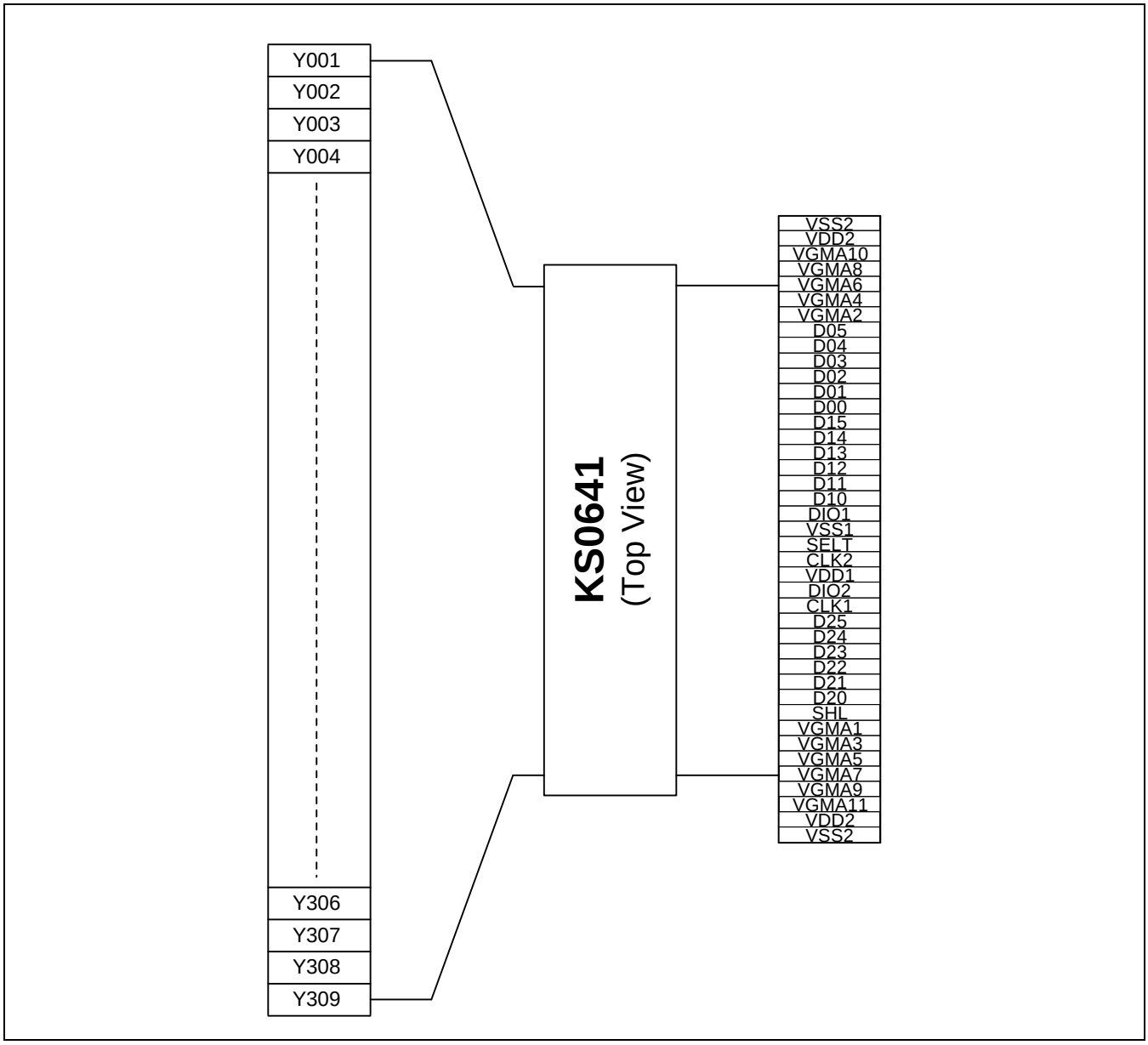

Figure 2. KS0641 Pin Assignments

PIN DESCRIPTIONS

Symbol	Pin Name	Description
VDD1	Logic power supply	3.0- 5.5 V
VDD2	Driver power supply	3.0 - 5.5 V
VSS1	Logic ground	Ground (0 V)
VSS2	Driver ground	Ground (0 V)
Y1 – Y309	Driver outputs	The D/A converted 64 gray scale analog voltage is output.
D0<0:5> - D2<0:5>	Display data input	The display data is input with a width of 18 bits, gray-scale data (6 bits) by 3 dots (R,G,B) DX0: LSB, DX5: MSB
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. The shift direction of the shift registers is as follows. SHL = H: DIO1 input, Y1 → Y309, DIO2 output SHL = L: DIO2 input, Y309 → Y1, DIO1 output
DIO1	Start pulse input / output	SHL = H: Used as the start pulse input pin. SHL = L: Used as the start pulse output pin.
DIO2	Start pulse input / output	SHL = H: Used as the start pulse output pin. SHL = L: Used as the start pulse input pin.
CLK2	Shift clock input	Refer to the shift register's shift clock input. the display data is loaded to the data register at the rising edge of CLK2.
CLK1	Latch input	Latches the contents of the data register at rising edge and transfers them to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the "Relationships between CLK1 start pulse (DIO1, DIO2) and blanking period" of the switching characteristic waveform.
SELT	300 / 309CH output control input	This pin controls 300CH or 309CH output. SELT = H: 309CH output → Y151 to Y159 are useless. SELT = L: 300CH output. → Y151 to Y159 are useless. This pin is internally pulled-up.(Rpu = 30 kΩ)
VGMA1 – VGMA11	Gamma corrected power supplies	Input the gamma corrected power supplies from external source. VDD2 ≥ VGMA1 > VGMA2 > …… > VGMA10 > VGMA11 ≥ VSS2 Keep gray-scale power supply unchanged during the gray-scale voltage output.
TESTB	Test input	TESTB = H: Normal operation mode TESTB = L: Test mode (OP AMP CUT-OFF) This pin is internally pulled-up.(Rpu = 30kΩ)

OPERATION DESCRIPTION

DISPLAY DATA TRANSFER

When DIO1 (or DIO2) pulse is loaded into internal latch on the rising edge of CLK2, DIO1 (or DIO2) pulse enables the operation of data transfer, so display data is valid on the next rising edge of CLK2. Once all the data of 300 / 309 channels are loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the next rising edge of CLK2 after the falling edge of DIO1 (or DIO2).

EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

(1) SHL = "L"
Connect DIO1 pin of previous stage to the DIO2 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

(2) SHL = "H"
Connect DIO2 pin of previous stage to the DIO1 pin of next stage and all the input pins except DIO2 and DIO1 are connected together in each device.

RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE

The LCD drive output voltages are determined by the input data and 11 gamma corrected power supplies (VGMA1 - VGMA11).

SHL = H

OUTPUT	Y1	Y2	Y3	.....	Y307	Y308	Y309
-	First			→	Last		
DATA	D00 - D05	D10 - D15	D20 - D25	.....	D00 - D05	D10 - D15	D20 - D25

SHL = L

OUTPUT	Y1	Y2	Y3	.....	Y307	Y308	Y309
-	Last			←	First		
DATA	D00 - D05	D10 - D15	D20 - D25	.....	D00 - D05	D10 - D15	D20 - D25

Figure 3. Relationship between Shift Direction and Output Data

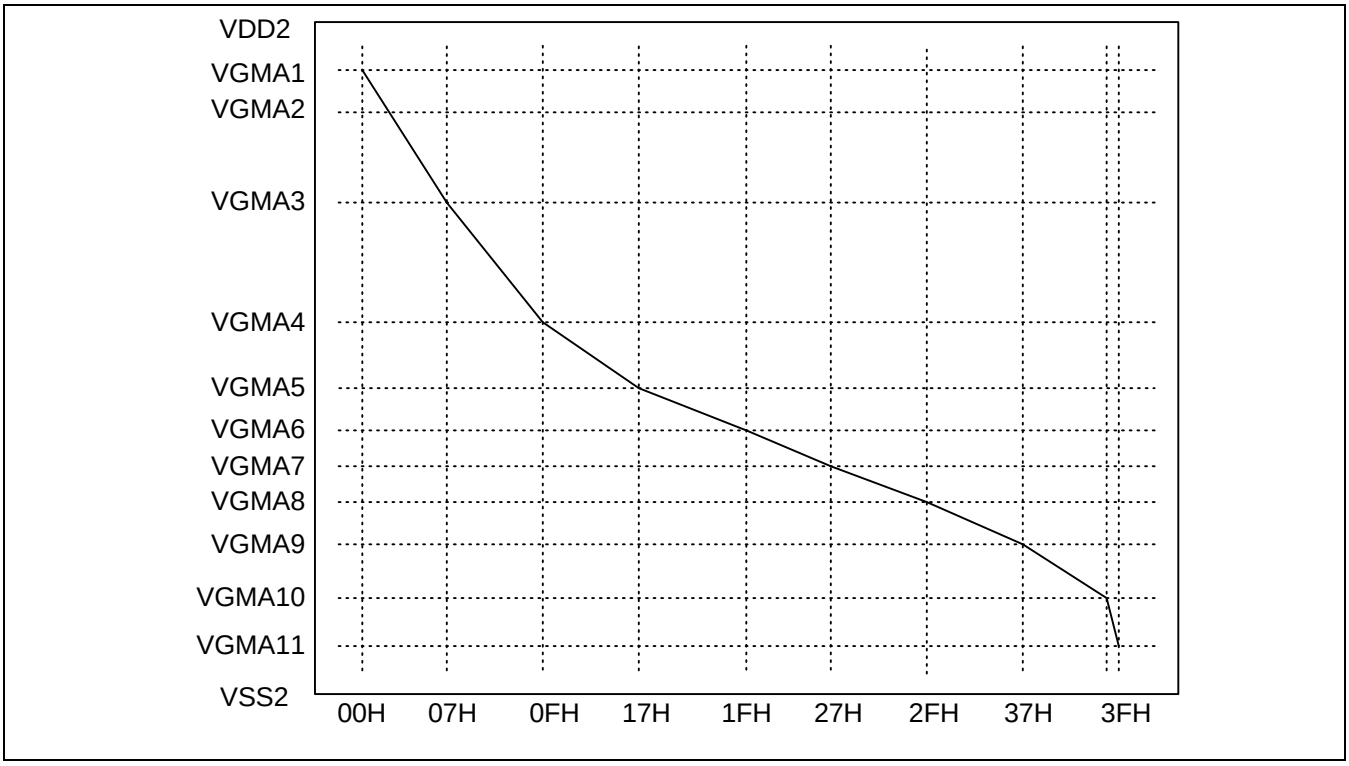

Figure 4. Gamma Correction Curve

Table 2. Relationship between Input Data and Output Voltage Value:
In case of using 11 levels of Gamma-corrected power supplies (VGMA1 to VGMA11)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	VH0	VGMA1
01H	0	0	0	0	0	1	VH1	VGMA3 + (VGMA2 – VGMA3) × 6/7
02H	0	0	0	0	1	0	VH2	VGMA3 + (VGMA2 – VGMA3) × 5/7
03H	0	0	0	0	1	1	VH3	VGMA3 + (VGMA2 – VGMA3) × 4/7
04H	0	0	0	1	0	0	VH4	VGMA3 + (VGMA2 – VGMA3) × 3/7
05H	0	0	0	1	0	1	VH5	VGMA3 + (VGMA2 – VGMA3) × 2/7
06H	0	0	0	1	1	0	VH6	VGMA3 + (VGMA2 – VGMA3) × 1/7
07H	0	0	0	1	1	1	VH7	VGMA3
08H	0	0	1	0	0	0	VH8	VGMA4 + (VGMA3 – VGMA4) × 7/8
09H	0	0	1	0	0	1	VH9	VGMA4 + (VGMA3 – VGMA4) × 6/8
0AH	0	0	1	0	1	0	VH10	VGMA4 + (VGMA3 – VGMA4) × 5/8
0BH	0	0	1	0	1	1	VH11	VGMA4 + (VGMA3 – VGMA4) × 4/8
0CH	0	0	1	1	0	0	VH12	VGMA4 + (VGMA3 – VGMA4) × 3/8
0DH	0	0	1	1	0	1	VH13	VGMA4 + (VGMA3 – VGMA4) × 2/8
0EH	0	0	1	1	1	0	VH14	VGMA4 + (VGMA3 – VGMA4) × 1/8
0FH	0	0	1	1	1	1	VH15	VGMA4
10H	0	1	0	0	0	0	VH16	VGMA5 + (VGMA4 – VGMA5) × 7/8
11H	0	1	0	0	0	1	VH17	VGMA5 + (VGMA4 – VGMA5) × 6/8
12H	0	1	0	0	1	0	VH18	VGMA5 + (VGMA4 – VGMA5) × 5/8
13H	0	1	0	0	1	1	VH19	VGMA5 + (VGMA4 – VGMA5) × 4/8
14H	0	1	0	1	0	0	VH20	VGMA5 + (VGMA4 – VGMA5) × 3/8
15H	0	1	0	1	0	1	VH21	VGMA5 + (VGMA4 – VGMA5) × 2/8
16H	0	1	0	1	1	0	VH22	VGMA5 + (VGMA4 – VGMA5) × 1/8
17H	0	1	0	1	1	1	VH23	VGMA5
18H	0	1	1	0	0	0	VH24	VGMA6 + (VGMA5 – VGMA6) × 7/8
19H	0	1	1	0	0	1	VH25	VGMA6 + (VGMA5 – VGMA6) × 6/8
1AH	0	1	1	0	1	0	VH26	VGMA6 + (VGMA5 – VGMA6) × 5/8
1BH	0	1	1	0	1	1	VH27	VGMA6 + (VGMA5 – VGMA6) × 4/8
1CH	0	1	1	1	0	0	VH28	VGMA6 + (VGMA5 – VGMA6) × 3/8
1DH	0	1	1	1	0	1	VH29	VGMA6 + (VGMA5 – VGMA6) × 2/8
1EH	0	1	1	1	1	0	VH30	VGMA6 + (VGMA5 – VGMA6) × 1/8
1FH	0	1	1	1	1	1	VH31	VGMA6

NOTE: VDD2≥VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6>VGMA7>VGMA8>VGMA9>VGMA10>VGMA11≥ VSS2

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
20H	1	0	0	0	0	0	VH32	VGMA7 + (VGMA6 – VGMA7) × 7/8
21H	1	0	0	0	0	1	VH33	VGMA7 + (VGMA6 – VGMA7) × 7/8
22H	1	0	0	0	1	0	VH34	VGMA7 + (VGMA6 – VGMA7) × 7/8
23H	1	0	0	0	1	1	VH35	VGMA7 + (VGMA6 – VGMA7) × 7/8
24H	1	0	0	1	0	0	VH36	VGMA7 + (VGMA6 – VGMA7) × 7/8
25H	1	0	0	1	0	1	VH37	VGMA7 + (VGMA6 – VGMA7) × 7/8
26H	1	0	0	1	1	0	VH38	VGMA7 + (VGMA6 – VGMA7) × 7/8
27H	1	0	0	1	1	1	VH39	VGMA7
28H	1	0	1	0	0	0	VH40	VGMA8 + (VGMA7 – VGMA8) × 7/8
29H	1	0	1	0	0	1	VH41	VGMA8 + (VGMA7 – VGMA8) × 6/8
2AH	1	0	1	0	1	0	VH42	VGMA8 + (VGMA7 – VGMA8) × 5/8
2BH	1	0	1	0	1	1	VH43	VGMA8 + (VGMA7 – VGMA8) × 4/8
2CH	1	0	1	1	0	0	VH44	VGMA8 + (VGMA7 – VGMA8) × 3/8
2DH	1	0	1	1	0	1	VH45	VGMA8 + (VGMA7 – VGMA8) × 2/8
2EH	1	0	1	1	1	0	VH46	VGMA8 + (VGMA7 – VGMA8) × 1/8
2FH	1	0	1	1	1	1	VH47	VGMA8
30H	1	1	0	0	0	0	VH48	VGMA9 + (VGMA8 – VGMA9) × 7/8
31H	1	1	0	0	0	1	VH49	VGMA9 + (VGMA8 – VGMA9) × 6/8
32H	1	1	0	0	1	0	VH50	VGMA9 + (VGMA8 – VGMA9) × 5/8
33H	1	1	0	0	1	1	VH51	VGMA9 + (VGMA8 – VGMA9) × 4/8
34H	1	1	0	1	0	0	VH52	VGMA9 + (VGMA8 – VGMA9) × 3/8
35H	1	1	0	1	0	1	VH53	VGMA9 + (VGMA8 – VGMA9) × 2/8
36H	1	1	0	1	1	0	VH54	VGMA9 + (VGMA8 – VGMA9) × 1/8
37H	1	1	0	1	1	1	VH55	VGMA9
38H	1	1	1	0	0	0	VH56	VGMA10 + (VGMA9 – VGMA10) × 6/7
39H	1	1	1	0	0	1	VH57	VGMA10 + (VGMA9 – VGMA10) × 5/7
3AH	1	1	1	0	1	0	VH58	VGMA10 + (VGMA9 – VGMA10) × 4/7
3BH	1	1	1	0	1	1	VH59	VGMA10 + (VGMA9 – VGMA10) × 3/7
3CH	1	1	1	1	0	0	VH60	VGMA10 + (VGMA9 – VGMA10) × 2/7
3DH	1	1	1	1	0	1	VH61	VGMA10 + (VGMA9 – VGMA10) × 1/7
3EH	1	1	1	1	1	0	VH62	VGMA10
3FH	1	1	1	1	1	1	VH63	VGMA11

RGMA (Gamma-Corrected Resistance) Ratio. (if the RGMA1 equals 1)

RGMA1	1.00	RGMA6	0.84
RGMA2	2.00	RGMA7	0.66
RGMA3	2.77	RGMA8	0.84
RGMA4	1.50	RGMA9	1.42
RGMA5	0.90	RGMA10	1.05

RGMA1 = 2.31 kΩ

Table 3. Relationship between Input Data and Output Voltage Value:
In case of using 10 levels of Gamma-corrected power supplies (VGMA1 = OPEN)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	VH0	VGMA2
01H	0	0	0	0	0	1	VH1	VGMA3 + (VGMA2 – VGMA3) × 6/7
02H	0	0	0	0	1	0	VH2	VGMA3 + (VGMA2 – VGMA3) × 5/7
03H	0	0	0	0	1	1	VH3	VGMA3 + (VGMA2 – VGMA3) × 4/7
04H	0	0	0	1	0	0	VH4	VGMA3 + (VGMA2 – VGMA3) × 3/7
05H	0	0	0	1	0	1	VH5	VGMA3 + (VGMA2 – VGMA3) × 2/7
06H	0	0	0	1	1	0	VH6	VGMA3 + (VGMA2 – VGMA3) × 1/7
07H	0	0	0	1	1	1	VH7	VGMA3
08H	0	0	1	0	0	0	VH8	VGMA4 + (VGMA3 – VGMA4) × 7/8
09H	0	0	1	0	0	1	VH9	VGMA4 + (VGMA3 – VGMA4) × 6/8
0AH	0	0	1	0	1	0	VH10	VGMA4 + (VGMA3 – VGMA4) × 5/8
0BH	0	0	1	0	1	1	VH11	VGMA4 + (VGMA3 – VGMA4) × 4/8
0CH	0	0	1	1	0	0	VH12	VGMA4 + (VGMA3 – VGMA4) × 3/8
0DH	0	0	1	1	0	1	VH13	VGMA4 + (VGMA3 – VGMA4) × 2/8
0EH	0	0	1	1	1	0	VH14	VGMA4 + (VGMA3 – VGMA4) × 1/8
0FH	0	0	1	1	1	1	VH15	VGMA4
10H	0	1	0	0	0	0	VH16	VGMA5 + (VGMA4 – VGMA5) × 7/8
11H	0	1	0	0	0	1	VH17	VGMA5 + (VGMA4 – VGMA5) × 6/8
12H	0	1	0	0	1	0	VH18	VGMA5 + (VGMA4 – VGMA5) × 5/8
13H	0	1	0	0	1	1	VH19	VGMA5 + (VGMA4 – VGMA5) × 4/8
14H	0	1	0	1	0	0	VH20	VGMA5 + (VGMA4 – VGMA5) × 3/8
15H	0	1	0	1	0	1	VH21	VGMA5 + (VGMA4 – VGMA5) × 2/8
16H	0	1	0	1	1	0	VH22	VGMA5 + (VGMA4 – VGMA5) × 1/8
17H	0	1	0	1	1	1	VH23	VGMA5
18H	0	1	1	0	0	0	VH24	VGMA6 + (VGMA5 – VGMA6) × 7/8
19H	0	1	1	0	0	1	VH25	VGMA6 + (VGMA5 – VGMA6) × 6/8
1AH	0	1	1	0	1	0	VH26	VGMA6 + (VGMA5 – VGMA6) × 5/8
1BH	0	1	1	0	1	1	VH27	VGMA6 + (VGMA5 – VGMA6) × 4/8
1CH	0	1	1	1	0	0	VH28	VGMA6 + (VGMA5 – VGMA6) × 3/8
1DH	0	1	1	1	0	1	VH29	VGMA6 + (VGMA5 – VGMA6) × 2/8
1EH	0	1	1	1	1	0	VH30	VGMA6 + (VGMA5 – VGMA6) × 1/8
1FH	0	1	1	1	1	1	VH31	VGMA6

NOTE: VDD2≥VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6>VGMA7>VGMA8>VGMA9>VGMA10>VGMA11≥ VSS2

Table 3. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
20H	1	0	0	0	0	0	VH32	VGMA7 + (VGMA6 – VGMA7) × 7/8
21H	1	0	0	0	0	1	VH33	VGMA7 + (VGMA6 – VGMA7) × 7/8
22H	1	0	0	0	1	0	VH34	VGMA7 + (VGMA6 – VGMA7) × 7/8
23H	1	0	0	0	1	1	VH35	VGMA7 + (VGMA6 – VGMA7) × 7/8
24H	1	0	0	1	0	0	VH36	VGMA7 + (VGMA6 – VGMA7) × 7/8
25H	1	0	0	1	0	1	VH37	VGMA7 + (VGMA6 – VGMA7) × 7/8
26H	1	0	0	1	1	0	VH38	VGMA7 + (VGMA6 – VGMA7) × 7/8
27H	1	0	0	1	1	1	VH39	VGMA7
28H	1	0	1	0	0	0	VH40	VGMA8 + (VGMA7 – VGMA8) × 7/8
29H	1	0	1	0	0	1	VH41	VGMA8 + (VGMA7 – VGMA8) × 6/8
2AH	1	0	1	0	1	0	VH42	VGMA8 + (VGMA7 – VGMA8) × 5/8
2BH	1	0	1	0	1	1	VH43	VGMA8 + (VGMA7 – VGMA8) × 4/8
2CH	1	0	1	1	0	0	VH44	VGMA8 + (VGMA7 – VGMA8) × 3/8
2DH	1	0	1	1	0	1	VH45	VGMA8 + (VGMA7 – VGMA8) × 2/8
2EH	1	0	1	1	1	0	VH46	VGMA8 + (VGMA7 – VGMA8) × 1/8
2FH	1	0	1	1	1	1	VH47	VGMA8
30H	1	1	0	0	0	0	VH48	VGMA9 + (VGMA8 – VGMA9) × 7/8
31H	1	1	0	0	0	1	VH49	VGMA9 + (VGMA8 – VGMA9) × 6/8
32H	1	1	0	0	1	0	VH50	VGMA9 + (VGMA8 – VGMA9) × 5/8
33H	1	1	0	0	1	1	VH51	VGMA9 + (VGMA8 – VGMA9) × 4/8
34H	1	1	0	1	0	0	VH52	VGMA9 + (VGMA8 – VGMA9) × 3/8
35H	1	1	0	1	0	1	VH53	VGMA9 + (VGMA8 – VGMA9) × 2/8
36H	1	1	0	1	1	0	VH54	VGMA9 + (VGMA8 – VGMA9) × 1/8
37H	1	1	0	1	1	1	VH55	VGMA9
38H	1	1	1	0	0	0	VH56	VGMA10 + (VGMA9 – VGMA10) × 6/7
39H	1	1	1	0	0	1	VH57	VGMA10 + (VGMA9 – VGMA10) × 5/7
3AH	1	1	1	0	1	0	VH58	VGMA10 + (VGMA9 – VGMA10) × 4/7
3BH	1	1	1	0	1	1	VH59	VGMA10 + (VGMA9 – VGMA10) × 3/7
3CH	1	1	1	1	0	0	VH60	VGMA10 + (VGMA9 – VGMA10) × 2/7
3DH	1	1	1	1	0	1	VH61	VGMA10 + (VGMA9 – VGMA10) × 1/7
3EH	1	1	1	1	1	0	VH62	VGMA10
3FH	1	1	1	1	1	1	VH63	VGMA11

RGMA (Gamma-Corrected Resistance) Ratio. (if the RGMA2 equals 1)

RGMA1	-	RGMA6	0.42
RGMA2	1.00	RGMA7	0.33
RGMA3	1.39	RGMA8	0.42
RGMA4	0.75	RGMA9	0.71
RGMA5	0.45	RGMA10	0.53

RGMA1 = 4.62 kΩ

Table 4. Relationship between Input Data and Output Voltage Value:
In case of using 10 levels of Gamma-corrected power supplies (VGMA2 = OPEN)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	VH0	VGMA3 + (VGMA2 – VGMA3) × 7/8
01H	0	0	0	0	0	1	VH1	VGMA3 + (VGMA2 – VGMA3) × 6/8
02H	0	0	0	0	1	0	VH2	VGMA3 + (VGMA2 – VGMA3) × 5/8
03H	0	0	0	0	1	1	VH3	VGMA3 + (VGMA2 – VGMA3) × 4/8
04H	0	0	0	1	0	0	VH4	VGMA3 + (VGMA2 – VGMA3) × 3/8
05H	0	0	0	1	0	1	VH5	VGMA3 + (VGMA2 – VGMA3) × 2/8
06H	0	0	0	1	1	0	VH6	VGMA3 + (VGMA2 – VGMA3) × 1/8
07H	0	0	0	1	1	1	VH7	VGMA3
08H	0	0	1	0	0	0	VH8	VGMA4 + (VGMA3 – VGMA4) × 7/8
09H	0	0	1	0	0	1	VH9	VGMA4 + (VGMA3 – VGMA4) × 6/8
0AH	0	0	1	0	1	0	VH10	VGMA4 + (VGMA3 – VGMA4) × 5/8
0BH	0	0	1	0	1	1	VH11	VGMA4 + (VGMA3 – VGMA4) × 4/8
0CH	0	0	1	1	0	0	VH12	VGMA4 + (VGMA3 – VGMA4) × 3/8
0DH	0	0	1	1	0	1	VH13	VGMA4 + (VGMA3 – VGMA4) × 2/8
0EH	0	0	1	1	1	0	VH14	VGMA4 + (VGMA3 – VGMA4) × 1/8
0FH	0	0	1	1	1	1	VH15	VGMA4
10H	0	1	0	0	0	0	VH16	VGMA5 + (VGMA4 – VGMA5) × 7/8
11H	0	1	0	0	0	1	VH17	VGMA5 + (VGMA4 – VGMA5) × 6/8
12H	0	1	0	0	1	0	VH18	VGMA5 + (VGMA4 – VGMA5) × 5/8
13H	0	1	0	0	1	1	VH19	VGMA5 + (VGMA4 – VGMA5) × 4/8
14H	0	1	0	1	0	0	VH20	VGMA5 + (VGMA4 – VGMA5) × 3/8
15H	0	1	0	1	0	1	VH21	VGMA5 + (VGMA4 – VGMA5) × 2/8
16H	0	1	0	1	1	0	VH22	VGMA5 + (VGMA4 – VGMA5) × 1/8
17H	0	1	0	1	1	1	VH23	VGMA5
18H	0	1	1	0	0	0	VH24	VGMA6 + (VGMA5 – VGMA6) × 7/8
19H	0	1	1	0	0	1	VH25	VGMA6 + (VGMA5 – VGMA6) × 6/8
1AH	0	1	1	0	1	0	VH26	VGMA6 + (VGMA5 – VGMA6) × 5/8
1BH	0	1	1	0	1	1	VH27	VGMA6 + (VGMA5 – VGMA6) × 4/8
1CH	0	1	1	1	0	0	VH28	VGMA6 + (VGMA5 – VGMA6) × 3/8
1DH	0	1	1	1	0	1	VH29	VGMA6 + (VGMA5 – VGMA6) × 2/8
1EH	0	1	1	1	1	0	VH30	VGMA6 + (VGMA5 – VGMA6) × 1/8
1FH	0	1	1	1	1	1	VH31	VGMA6

NOTE: VDD2≥VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6>VGMA7>VGMA8>VGMA9>VGMA10>VGMA11≥ VSS2

Table 4. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
20H	1	0	0	0	0	0	VH32	VGMA7 + (VGMA6 – VGMA7) × 7/8
21H	1	0	0	0	0	1	VH33	VGMA7 + (VGMA6 – VGMA7) × 7/8
22H	1	0	0	0	1	0	VH34	VGMA7 + (VGMA6 – VGMA7) × 7/8
23H	1	0	0	0	1	1	VH35	VGMA7 + (VGMA6 – VGMA7) × 7/8
24H	1	0	0	1	0	0	VH36	VGMA7 + (VGMA6 – VGMA7) × 7/8
25H	1	0	0	1	0	1	VH37	VGMA7 + (VGMA6 – VGMA7) × 7/8
26H	1	0	0	1	1	0	VH38	VGMA7 + (VGMA6 – VGMA7) × 7/8
27H	1	0	0	1	1	1	VH39	VGMA7
28H	1	0	1	0	0	0	VH40	VGMA8 + (VGMA7 – VGMA8) × 7/8
29H	1	0	1	0	0	1	VH41	VGMA8 + (VGMA7 – VGMA8) × 6/8
2AH	1	0	1	0	1	0	VH42	VGMA8 + (VGMA7 – VGMA8) × 5/8
2BH	1	0	1	0	1	1	VH43	VGMA8 + (VGMA7 – VGMA8) × 4/8
2CH	1	0	1	1	0	0	VH44	VGMA8 + (VGMA7 – VGMA8) × 3/8
2DH	1	0	1	1	0	1	VH45	VGMA8 + (VGMA7 – VGMA8) × 2/8
2EH	1	0	1	1	1	0	VH46	VGMA8 + (VGMA7 – VGMA8) × 1/8
2FH	1	0	1	1	1	1	VH47	VGMA8
30H	1	1	0	0	0	0	VH48	VGMA9 + (VGMA8 – VGMA9) × 7/8
31H	1	1	0	0	0	1	VH49	VGMA9 + (VGMA8 – VGMA9) × 6/8
32H	1	1	0	0	1	0	VH50	VGMA9 + (VGMA8 – VGMA9) × 5/8
33H	1	1	0	0	1	1	VH51	VGMA9 + (VGMA8 – VGMA9) × 4/8
34H	1	1	0	1	0	0	VH52	VGMA9 + (VGMA8 – VGMA9) × 3/8
35H	1	1	0	1	0	1	VH53	VGMA9 + (VGMA8 – VGMA9) × 2/8
36H	1	1	0	1	1	0	VH54	VGMA9 + (VGMA8 – VGMA9) × 1/8
37H	1	1	0	1	1	1	VH55	VGMA9
38H	1	1	1	0	0	0	VH56	VGMA10 + (VGMA9 – VGMA10) × 6/7
39H	1	1	1	0	0	1	VH57	VGMA10 + (VGMA9 – VGMA10) × 5/7
3AH	1	1	1	0	1	0	VH58	VGMA10 + (VGMA9 – VGMA10) × 4/7
3BH	1	1	1	0	1	1	VH59	VGMA10 + (VGMA9 – VGMA10) × 3/7
3CH	1	1	1	1	0	0	VH60	VGMA10 + (VGMA9 – VGMA10) × 2/7
3DH	1	1	1	1	0	1	VH61	VGMA10 + (VGMA9 – VGMA10) × 1/7
3EH	1	1	1	1	1	0	VH62	VGMA10
3FH	1	1	1	1	1	1	VH63	VGMA11

RGMA (Gamma-Corrected Resistance) Ratio. (if the sum of RGMA1 and RGMA2 equals 1)

RGMA1	1.00	RGMA6	0.37
RGMA2		RGMA7	0.29
RGMA3	1.21	RGMA8	0.37
RGMA4	0.66	RGMA9	0.62
RGMA5	0.39	RGMA10	0.46

RGMA1 + RGMA2 = 5.28 kΩ

Table 5. Relationship between Input Data and Output Voltage Value:
In case of using 9 levels of Gamma-corrected power supplies (VGMA2, VGMA10 = OPEN)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	VH0	VGMA3 + (VGMA2 – VGMA3) × 7/8
01H	0	0	0	0	0	1	VH1	VGMA3 + (VGMA2 – VGMA3) × 6/8
02H	0	0	0	0	1	0	VH2	VGMA3 + (VGMA2 – VGMA3) × 5/8
03H	0	0	0	0	1	1	VH3	VGMA3 + (VGMA2 – VGMA3) × 4/8
04H	0	0	0	1	0	0	VH4	VGMA3 + (VGMA2 – VGMA3) × 3/8
05H	0	0	0	1	0	1	VH5	VGMA3 + (VGMA2 – VGMA3) × 2/8
06H	0	0	0	1	1	0	VH6	VGMA3 + (VGMA2 – VGMA3) × 1/8
07H	0	0	0	1	1	1	VH7	VGMA3
08H	0	0	1	0	0	0	VH8	VGMA4 + (VGMA3 – VGMA4) × 7/8
09H	0	0	1	0	0	1	VH9	VGMA4 + (VGMA3 – VGMA4) × 6/8
0AH	0	0	1	0	1	0	VH10	VGMA4 + (VGMA3 – VGMA4) × 5/8
0BH	0	0	1	0	1	1	VH11	VGMA4 + (VGMA3 – VGMA4) × 4/8
0CH	0	0	1	1	0	0	VH12	VGMA4 + (VGMA3 – VGMA4) × 3/8
0DH	0	0	1	1	0	1	VH13	VGMA4 + (VGMA3 – VGMA4) × 2/8
0EH	0	0	1	1	1	0	VH14	VGMA4 + (VGMA3 – VGMA4) × 1/8
0FH	0	0	1	1	1	1	VH15	VGMA4
10H	0	1	0	0	0	0	VH16	VGMA5 + (VGMA4 – VGMA5) × 7/8
11H	0	1	0	0	0	1	VH17	VGMA5 + (VGMA4 – VGMA5) × 6/8
12H	0	1	0	0	1	0	VH18	VGMA5 + (VGMA4 – VGMA5) × 5/8
13H	0	1	0	0	1	1	VH19	VGMA5 + (VGMA4 – VGMA5) × 4/8
14H	0	1	0	1	0	0	VH20	VGMA5 + (VGMA4 – VGMA5) × 3/8
15H	0	1	0	1	0	1	VH21	VGMA5 + (VGMA4 – VGMA5) × 2/8
16H	0	1	0	1	1	0	VH22	VGMA5 + (VGMA4 – VGMA5) × 1/8
17H	0	1	0	1	1	1	VH23	VGMA5
18H	0	1	1	0	0	0	VH24	VGMA6 + (VGMA5 – VGMA6) × 7/8
19H	0	1	1	0	0	1	VH25	VGMA6 + (VGMA5 – VGMA6) × 6/8
1AH	0	1	1	0	1	0	VH26	VGMA6 + (VGMA5 – VGMA6) × 5/8
1BH	0	1	1	0	1	1	VH27	VGMA6 + (VGMA5 – VGMA6) × 4/8
1CH	0	1	1	1	0	0	VH28	VGMA6 + (VGMA5 – VGMA6) × 3/8
1DH	0	1	1	1	0	1	VH29	VGMA6 + (VGMA5 – VGMA6) × 2/8
1EH	0	1	1	1	1	0	VH30	VGMA6 + (VGMA5 – VGMA6) × 1/8
1FH	0	1	1	1	1	1	VH31	VGMA6

NOTE: VDD2≥VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6>VGMA7>VGMA8>VGMA9>VGMA10>VGMA11≥ VSS2

Table 5. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
20H	1	0	0	0	0	0	VH32	VGMA7 + (VGMA6 – VGMA7) × 7/8
21H	1	0	0	0	0	1	VH33	VGMA7 + (VGMA6 – VGMA7) × 7/8
22H	1	0	0	0	1	0	VH34	VGMA7 + (VGMA6 – VGMA7) × 7/8
23H	1	0	0	0	1	1	VH35	VGMA7 + (VGMA6 – VGMA7) × 7/8
24H	1	0	0	1	0	0	VH36	VGMA7 + (VGMA6 – VGMA7) × 7/8
25H	1	0	0	1	0	1	VH37	VGMA7 + (VGMA6 – VGMA7) × 7/8
26H	1	0	0	1	1	0	VH38	VGMA7 + (VGMA6 – VGMA7) × 7/8
27H	1	0	0	1	1	1	VH39	VGMA7
28H	1	0	1	0	0	0	VH40	VGMA8 + (VGMA7 – VGMA8) × 7/8
29H	1	0	1	0	0	1	VH41	VGMA8 + (VGMA7 – VGMA8) × 6/8
2AH	1	0	1	0	1	0	VH42	VGMA8 + (VGMA7 – VGMA8) × 5/8
2BH	1	0	1	0	1	1	VH43	VGMA8 + (VGMA7 – VGMA8) × 4/8
2CH	1	0	1	1	0	0	VH44	VGMA8 + (VGMA7 – VGMA8) × 3/8
2DH	1	0	1	1	0	1	VH45	VGMA8 + (VGMA7 – VGMA8) × 2/8
2EH	1	0	1	1	1	0	VH46	VGMA8 + (VGMA7 – VGMA8) × 1/8
2FH	1	0	1	1	1	1	VH47	VGMA8
30H	1	1	0	0	0	0	VH48	VGMA9 + (VGMA8 – VGMA9) × 7/8
31H	1	1	0	0	0	1	VH49	VGMA9 + (VGMA8 – VGMA9) × 6/8
32H	1	1	0	0	1	0	VH50	VGMA9 + (VGMA8 – VGMA9) × 5/8
33H	1	1	0	0	1	1	VH51	VGMA9 + (VGMA8 – VGMA9) × 4/8
34H	1	1	0	1	0	0	VH52	VGMA9 + (VGMA8 – VGMA9) × 3/8
35H	1	1	0	1	0	1	VH53	VGMA9 + (VGMA8 – VGMA9) × 2/8
36H	1	1	0	1	1	0	VH54	VGMA9 + (VGMA8 – VGMA9) × 1/8
37H	1	1	0	1	1	1	VH55	VGMA9
38H	1	1	1	0	0	0	VH56	VGMA11 + (VGMA9 – VGMA11) × 7/8
39H	1	1	1	0	0	1	VH57	VGMA11 + (VGMA9 – VGMA11) × 6/8
3AH	1	1	1	0	1	0	VH58	VGMA11 + (VGMA9 – VGMA11) × 5/8
3BH	1	1	1	0	1	1	VH59	VGMA11 + (VGMA9 – VGMA11) × 4/8
3CH	1	1	1	1	0	0	VH60	VGMA11 + (VGMA9 – VGMA11) × 3/8
3DH	1	1	1	1	0	1	VH61	VGMA11 + (VGMA9 – VGMA11) × 2/8
3EH	1	1	1	1	1	0	VH62	VGMA11 + (VGMA9 – VGMA11) × 1/8
3FH	1	1	1	1	1	1	VH63	VGMA11

RGMA (Gamma-Corrected Resistance) Ratio. (if the sum of RGMA1 and RGMA2 equals 1)

RGMA1	1.00	RGMA6	0.37
RGMA2		RGMA7	0.29
RGMA3	1.21	RGMA8	0.37
RGMA4	0.66	RGMA9	0.71
RGMA5	0.39	RGMA10	

RGMA1 + RGMA2 = 5.28 kΩ

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings (VSS1 = VSS2 = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD1	-0.3 to 6.5	V
Driver supply voltage	VDD2	-0.3 to 6.5	
Input voltage	VGMA1 - 10	-0.3 to VDD2 + 0.3	
	Others	-0.3 to VDD1 + 0.3	
Output voltage	DIO1, 2	-0.3 to VDD1 + 0.3	
	Y1 - Y309	-0.3 to VDD2 + 0.3	
Operation temperature	Topr	-20 to 75	°C
Storage temperature	Tstg	-55 to 125	

CAUTIONS:

If LSIs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Turn on power order: VDD1 → control signal input → VDD2 → VGMA1 - VGMA11 Turn off power order: VGMA1 - VGMA11 → VDD2 → control signal input → VDD1

RECOMMENDED OPERATION CONDITIONS

Table 7. Recommended Operation Conditions (Ta = -20 to 75 °C, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD1	3.0	3.3	5.5	V
Driver supply voltage	VDD2	3.0	5.0	5.5	V
Gamma corrected voltage	VGMA1 – VGMA11	VSS2	-	VDD2	V
Maximum clock frequency	fmax	VDD1 = 3.3 V		55	MHz
Output load capacitance	CL	-	-	150	pF / PIN

DC CHARACTERISTICS

Table 8. DC Characteristics (Ta = -20 to 75 °C, VDD1 = 3.0 to 5.5 V, VDD2 = 3.0 to 5.5 V, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK2, D00 – D25, CLK1, DIO1 (DIO2)	0.7 VDD1	-	VDD1	V
Low level input voltage	VIL		0	-	0.3 VDD1	
Input leakage current	IL		--0.5	-	0.5	μA
High level output voltage	VOH	DIO1 (DIO2), VDD1=3.3V IO = -1.0 mA	VDD1 - 0.5	-	-	V
Low level output voltage	VOL	DIO1 (DIO2), VDD1=3.3V IO = +1.0 mA	-	-	0.5	
Resistor	R0 - R62		Rn × 0.7		Rn × 1.3	Ω
Driver output current	IVOH	VDD2 = 5.0 V, Vx = 3.5 V, Vyo = 4.5 V	-	-1.5	-0.5	mA
	IVOL	VDD2 = 5.0 V, Vx = 1.5 V, Vyo = 0.5 V	0.5	0.5	-	mA
Output voltage deviation	ΔVO	VSS2 + 0.2 V to VDD2 - 1.5 V	-	±10	±20	mV
Output voltage range	Vyo	Input data: 00H to 3FH	VSS2 + 0.2	-	VDD2 - 0.2	V
Logic part dynamic current	IDD1	VDD1 = 3.0 V (2)	-	3.5	5.5	mA
Driver part dynamic current	IDD2	VDD1 = 3.0 V, VDD2 = 5.0 V, VGMA1 = 4.5 V, VGMA11 = 0.5 V	-	5.5	7.0	

NOTES:

1. Vyo is the output voltage of analog output pins Y1 to Y309. Vx is the voltage applied to analog output pins Y1 to Y309.
2. CLK1 period is defined to be 30 μs at fCLK2 = 30 MHz, data pattern = 101010 , (checkerboard pattern), Ta = 25 °C

AC CHARACTERISTICS

Table 9. AC Characteristics (Ta = -20 to 75 °C, VDD2 = 3.0 to 5.5 V, VDD1 = 3.0 to 5.5 V, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	-	18	-	-	ns
Clock pulse low period	PWCLK(L)	-	4	-	-	
Clock pulse high period	PWCLK(H)	-	4	-	-	
Data setup time	tSETUP1	(1)	4	-	-	
Data hold time	tHOLD1	(1)	0	-	-	
Start pulse setup time	tSETUP2	(1)	4	-	-	
Start pulse hold time	tHOLD2	(1)	0	-	-	
Start pulse delay time	tPLH1	VDD1 = 3.3 V CL = 35 pF	-	-	14	
CLK1 setup time	tSETUP3	-	1	-	-	CLK2 period
Driver output delay time1	tPHL1	(2)	-	-	3	µs
Driver output delay time2	tPHL2	(3)	-	-	10	
CLK1 pulse high period	PWCLK1	-	2	-	-	CLK2 period
Data invalid period	tINV	DIO1 (2) ↑ → CLK2↑	1			CLK2 period
Last data timing	tLDT	-	0	-	-	ns
CLK1-CLK2 time	tCLK1–CLK2	CLK1↑ → CLK2↑	6	-	-	ns

NOTES:

1. Input condition (VIH = 0.7 VDD1, VIL = 0.3 VDD1)
2. The value is specified when the drive voltage value reaches the target output voltage level of 90%
3. The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.

WAVEFORMS

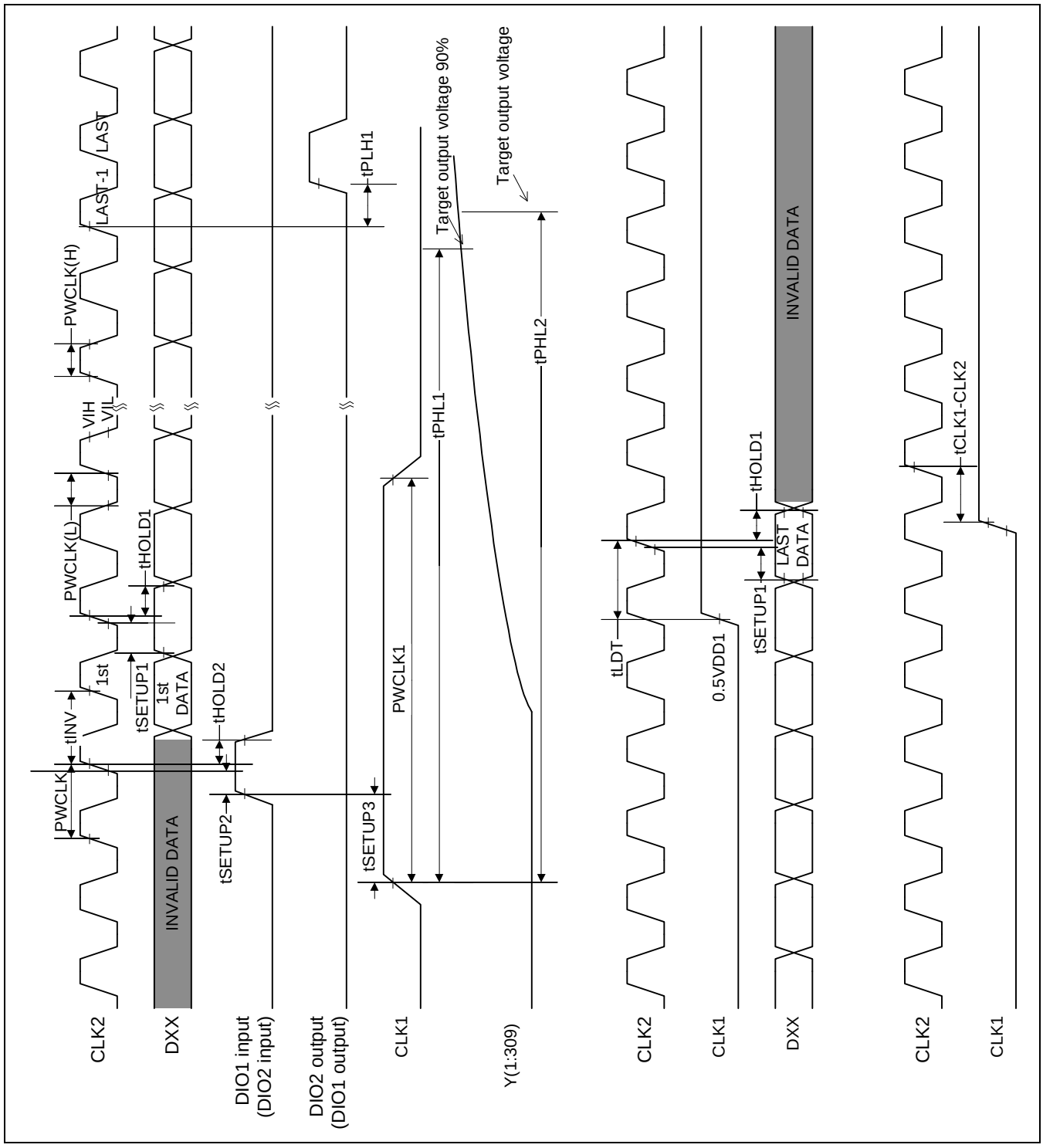

Figure 5. Waveforms

RELATIONSHIPS BETWEEN CLK1, START PULSE (DIO1, DIO2) AND BLANKING PERIOD

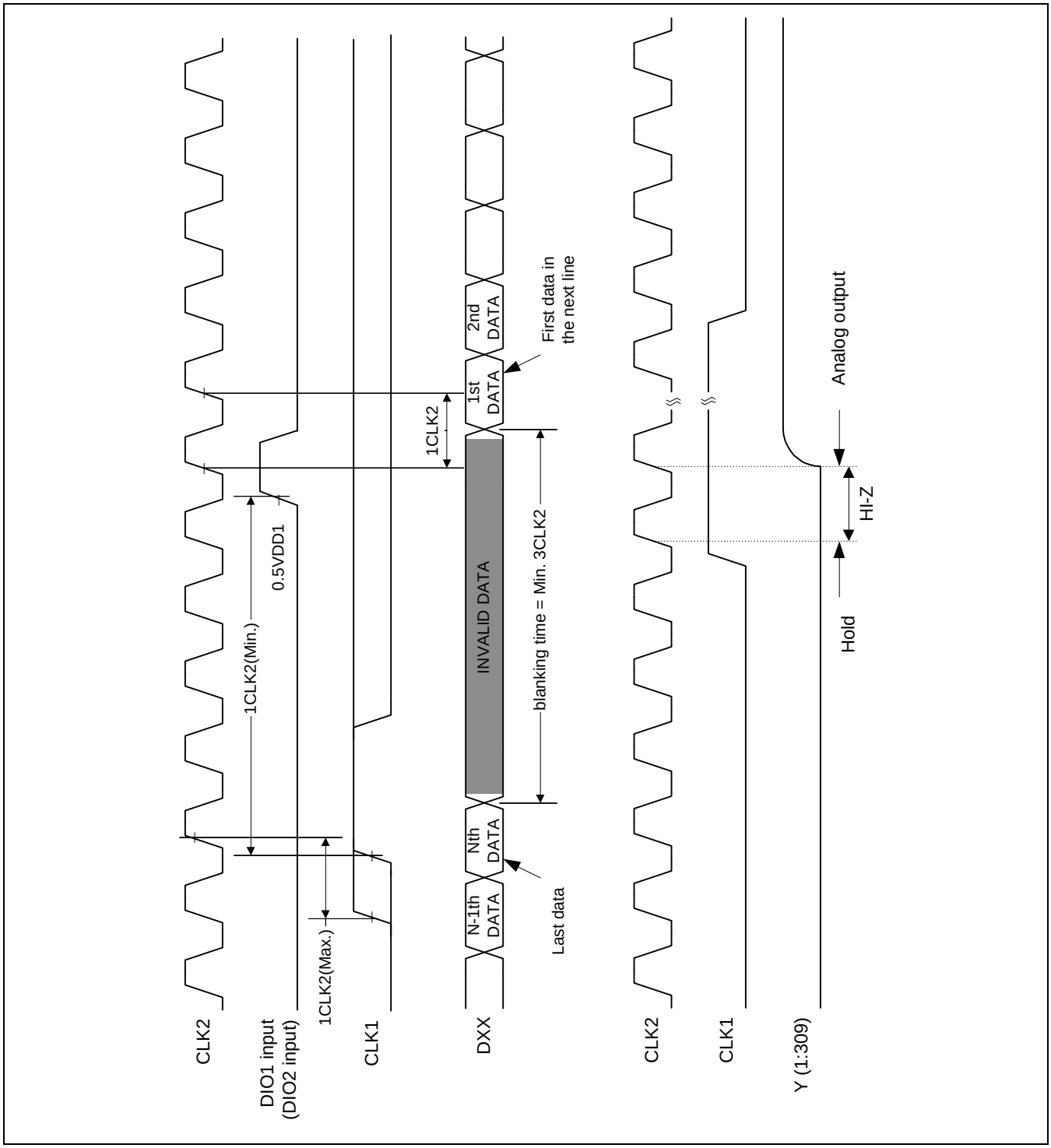

Figure 6. Waveforms