

LH531024

CMOS 1M (64K × 16) MROM

FEATURES

- 65,536 words × 16 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:
 - Operating: 412.5 mW (MAX.)
 - Standby: 550 μW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- JEDEC standard EPROM pinout (DIP)
- Packages:
 - 40-pin, 600-mil DIP
 - 40-pin, 525-mil SOP
 - 44-pin, 650-mil QFJ (PLCC)

DESCRIPTION

The LH531024 is a mask-programmable ROM organized as 65,536 × 16 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

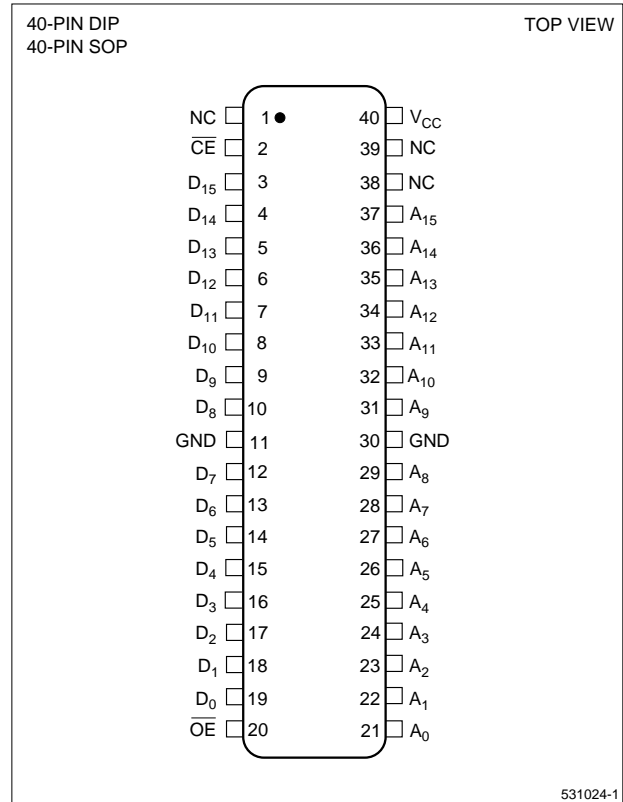


Figure 1. Pin Connections for DIP and SOP Packages

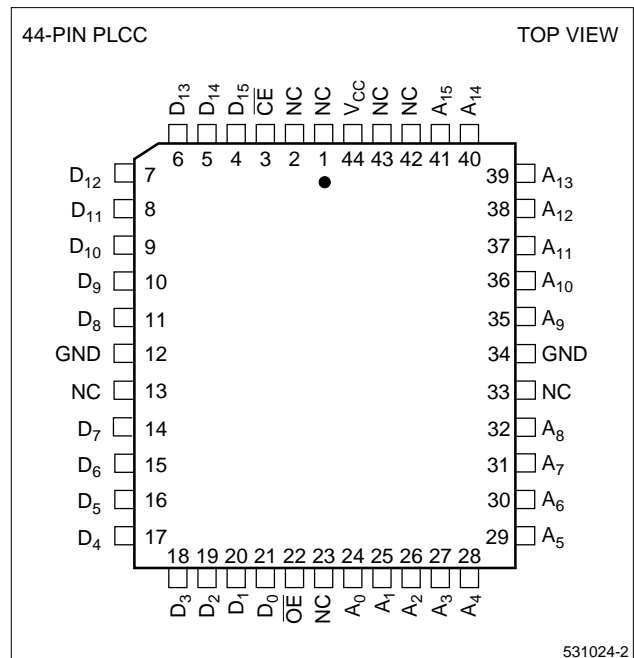


Figure 2. Pin Connections for QFJ (PLCC) Package

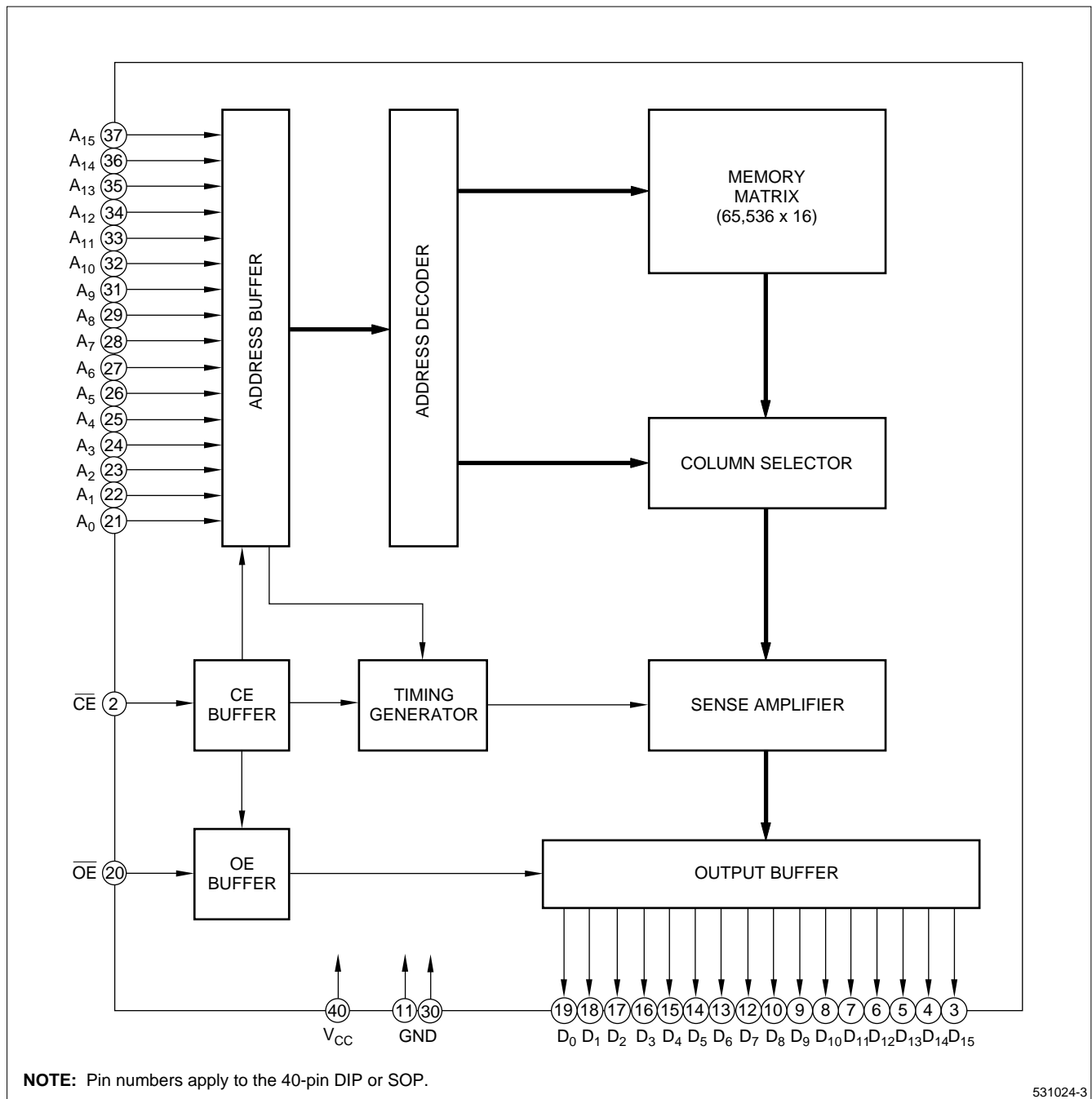


Figure 3. LH531024 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ – A ₁₅	Address input
D ₀ – D ₁₅	Data output
CE	Chip Enable input

SIGNAL	PIN NAME
OE	Output enable input
V _{CC}	Power supply (+5 V)
GND	Ground

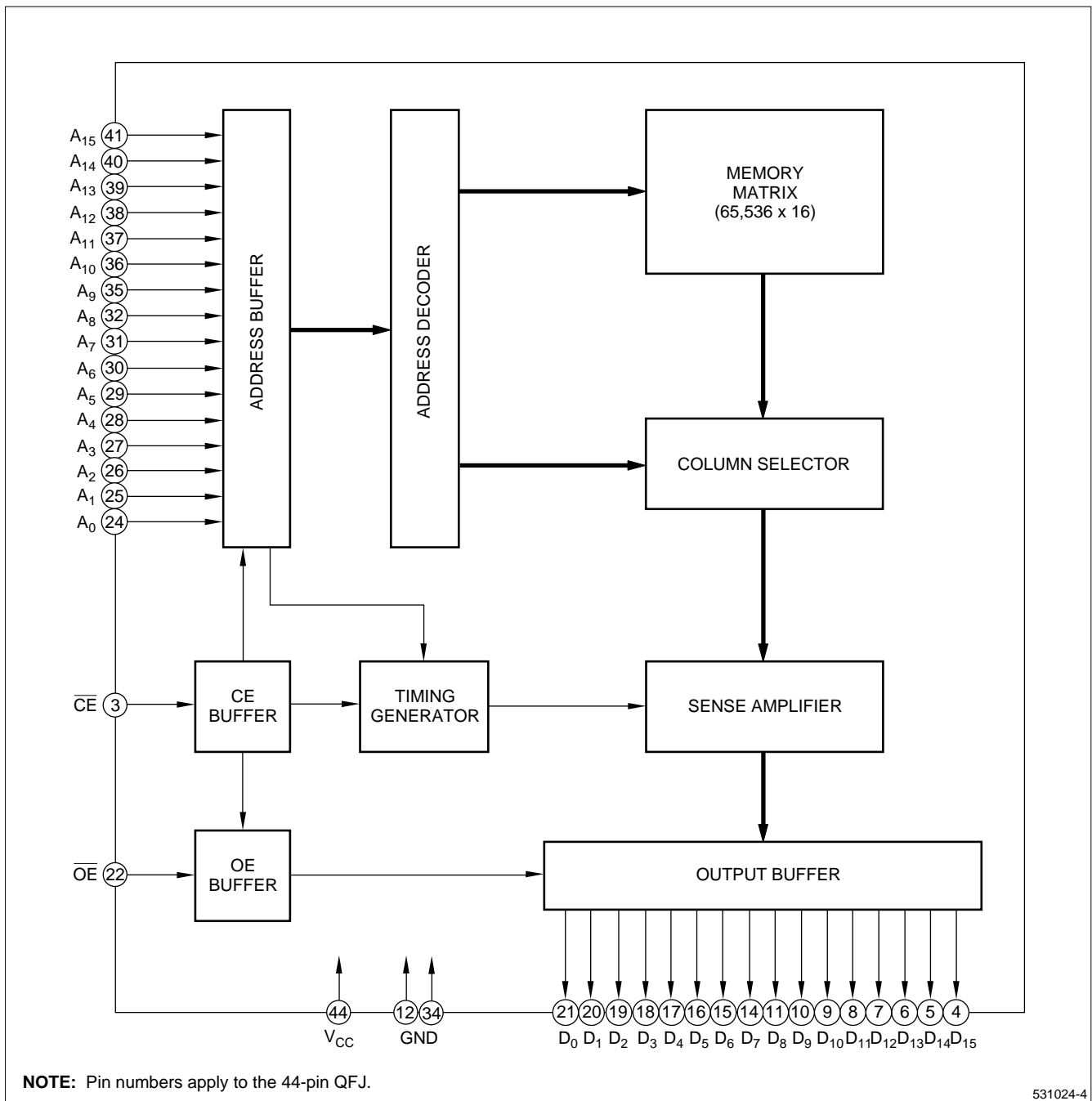


Figure 4. LH531024 Block Diagram

TRUTH TABLE

\overline{CE}	\overline{OE}	D ₀ – D ₁₅	SUPPLY CURRENT	NOTE
H	X	High-Z	Standby (I _{SB})	1
L	H		Operating (I _{CC})	
L	L	D ₀ – D ₁₅		

NOTE:

- X = H or L.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	–0.3 to +7.0	V
Input voltage	V _{IN}	–0.3 to V _{CC} +0.3	V
Output voltage	V _{OUT}	–0.3 to V _{CC} +0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V _{IL}		–0.3		0.8	V	
Input 'High' voltage	V _{IH}		2.2		V _{CC} + 0.3	V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V _{OH}	I _{OH} = –400 μA	2.4			V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}			10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}			10	μA	1
Operating current	I _{CC1}	t _{RC} = 100 ns			75	mA	2
	I _{CC2}	t _{RC} = 1 μs			65	mA	
	I _{CC3}	t _{RC} = 100 ns			70	mA	3
	I _{CC4}	t _{RC} = 1 μs			60	mA	
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$			3	mA	
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$			100	μA	
Input capacitance	C _{IN}	f = 1 MHz			10	pF	
Output capacitance	C _{OUT}	T _A = 25°C			10	pF	

NOTES:

- CE/OE = V_{IH}
- V_{IN} = V_{IH} or V_{IL}, $\overline{CE} = V_{IL}$, outputs open
- V_{IN} = (V_{CC} – 0.2 V) or 0.2 V, CE = 0.2 V, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
Output enable delay time	t_{OE}			50	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			50	ns	1
OE to output in High-Z	t_{OHZ}			50	ns	

NOTE:

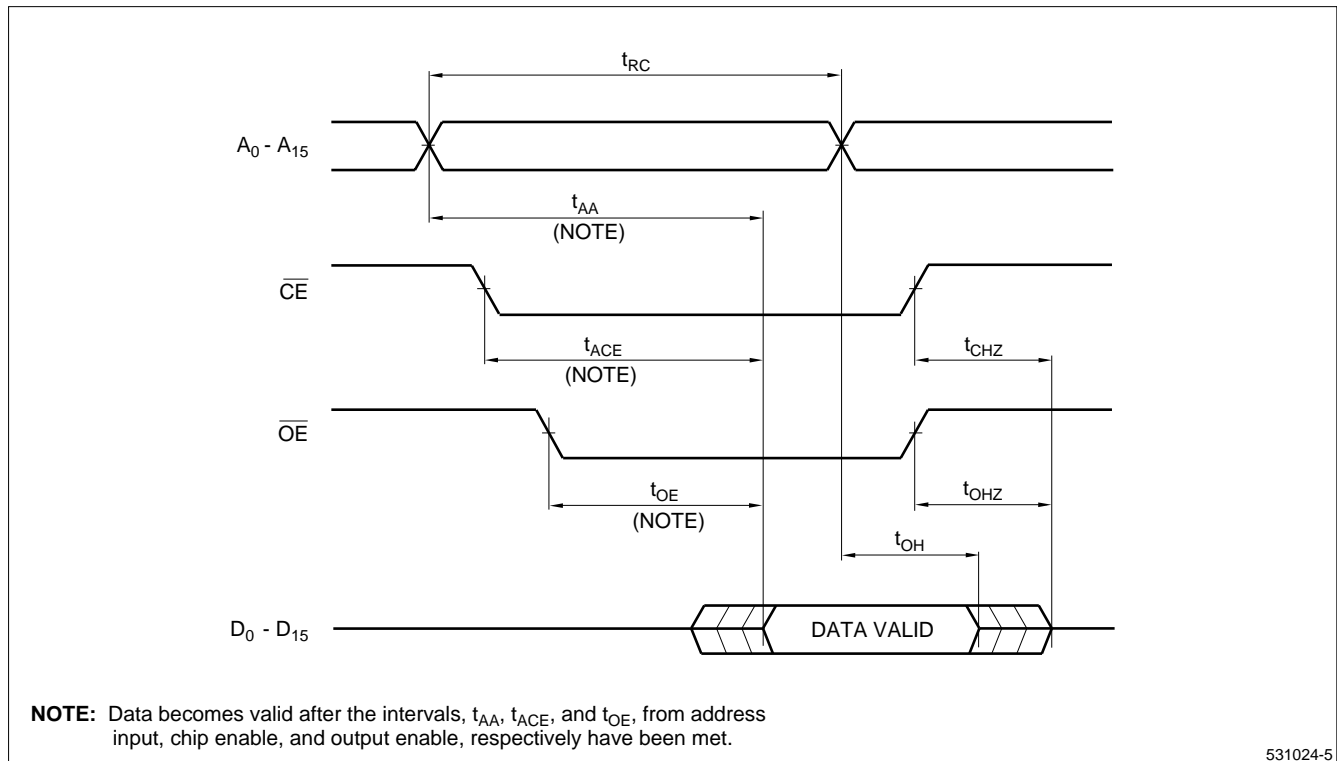
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

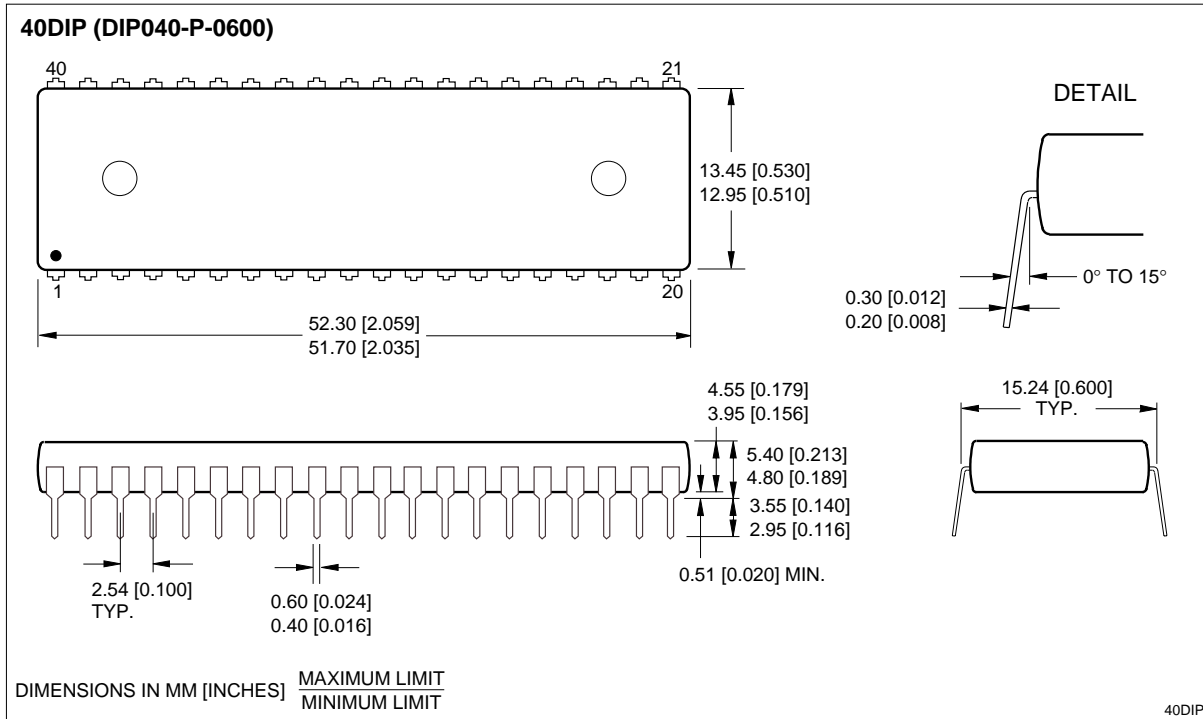
PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input signal rise time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL +100 pF

CAUTION

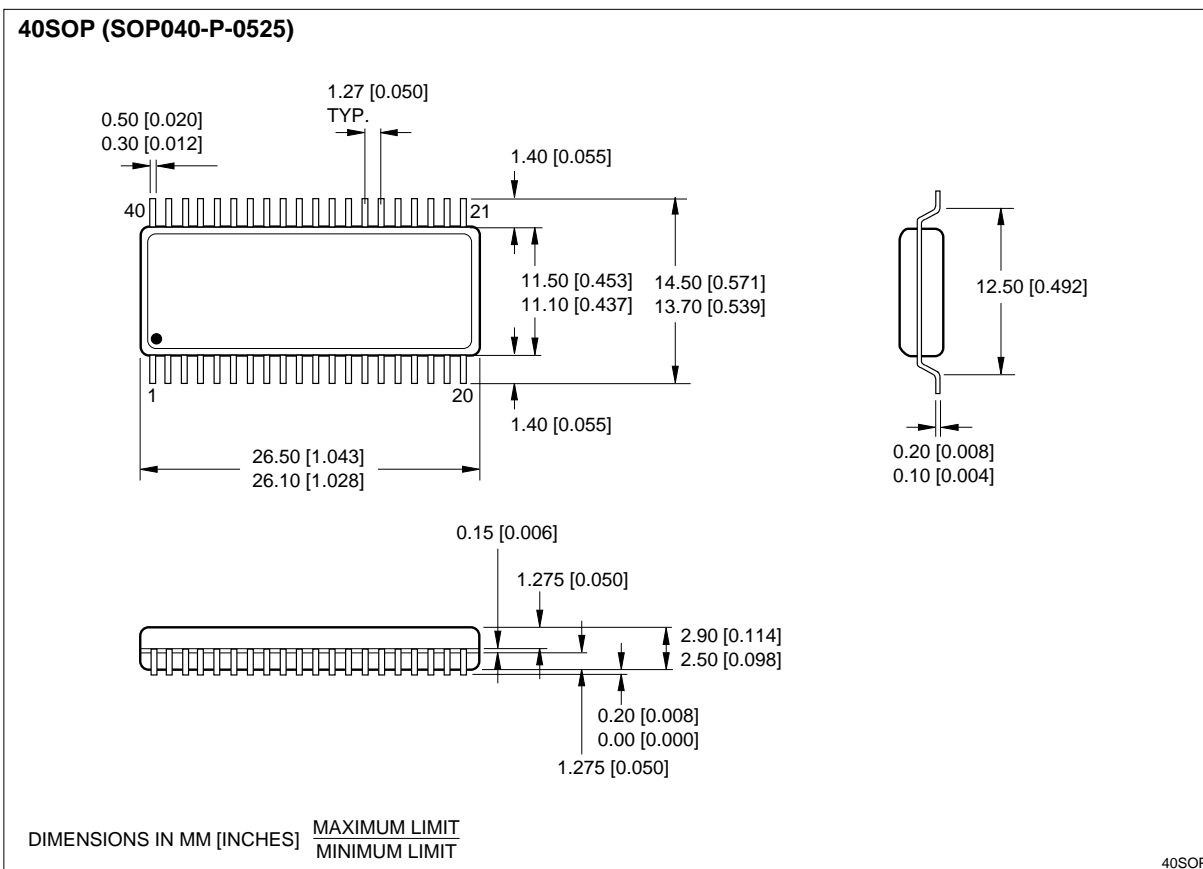
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

**Figure 5. Timing Diagram**

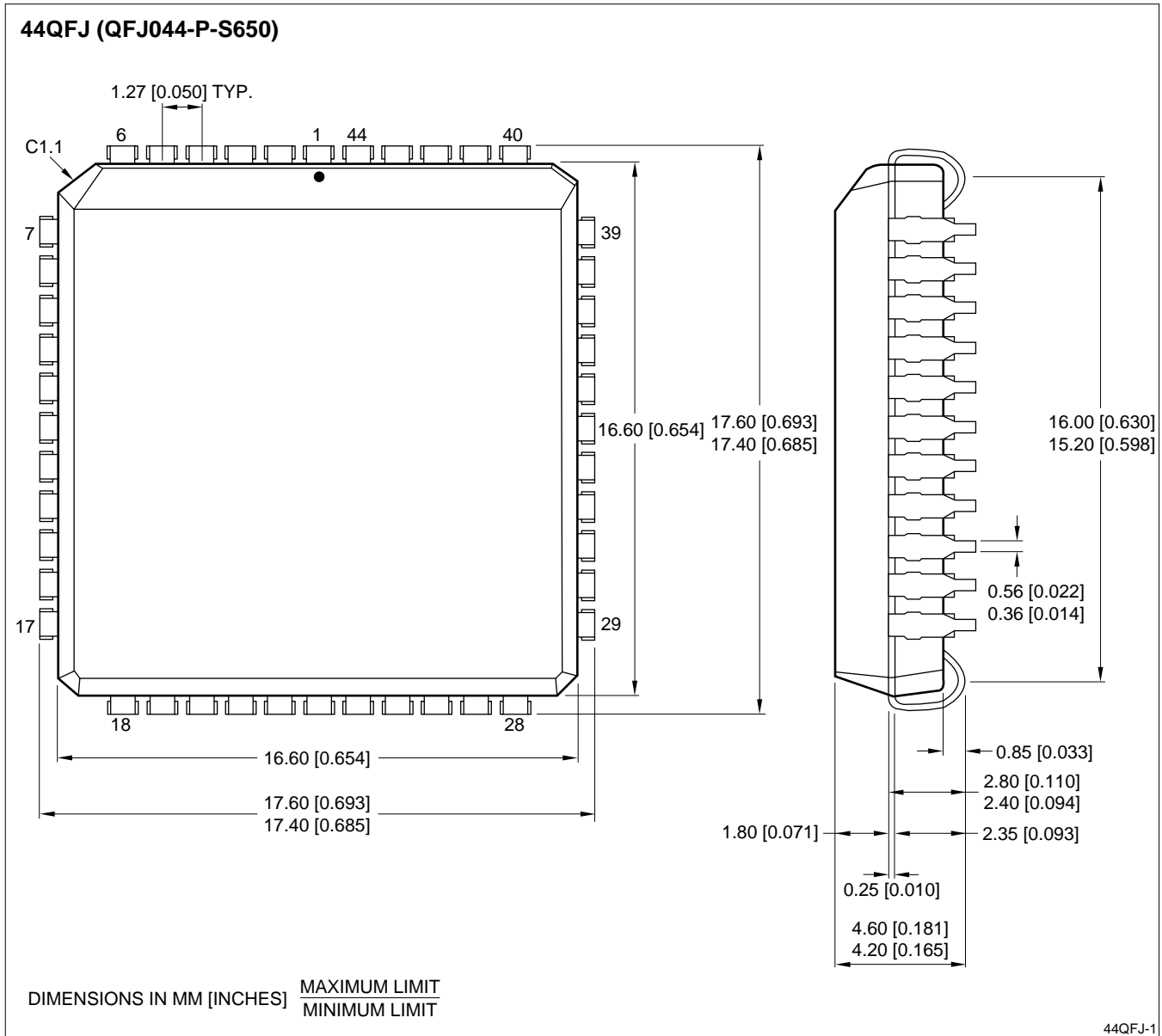
PACKAGE DIAGRAMS



40-pin, 600-mil DIP



40-pin, 525-mil SOP



44-pin, 650-mil QFJ (PLCC)

ORDERING INFORMATION

