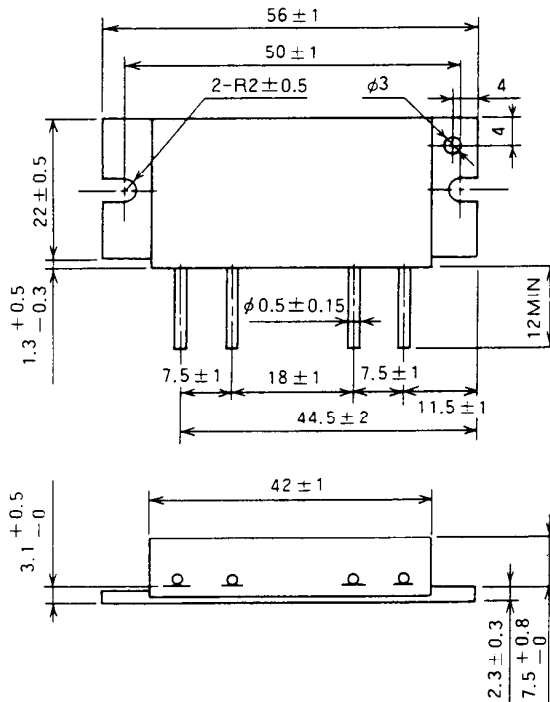


# M57747

144-148MHz, 12.5V, 13W, FM MOBILE RADIO

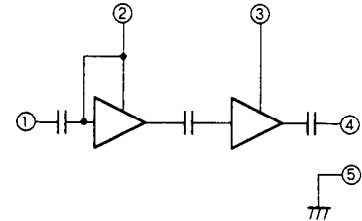
### OUTLINE DRAWING

Dimensions in mm



H6

### BLOCK DIAGRAM



PINNING :

- ① Pin : RF INPUT
- ② Vcc1 : 1st. DC SUPPLY
- ③ Vcc2 : FINAL DC SUPPLY
- ④ Po : RF OUTPUT
- ⑤ GND : FIN

### ABSOLUTE MAXIMUM RATINGS (Tc = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		17	V
Icc	Total current		5	A
Pin(max)	Input power	Vcc1 ≤ 12.5V, ZG = ZL = 50 Ω	0.4	W
PO(max)	Output power	Same as above	20	W
Tc(OP)	Operation case temperature	Same as above	- 30 to 110	°C
Tstg	Storage temperature		- 40 to 110	°C

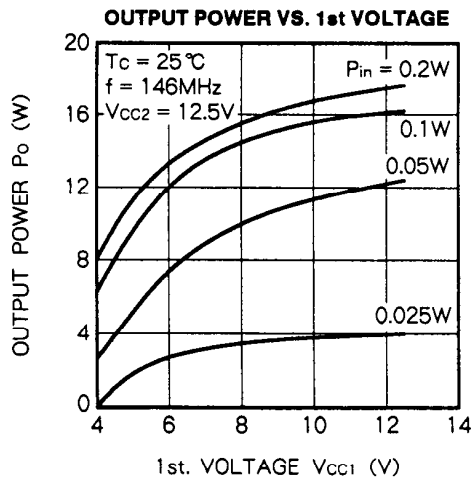
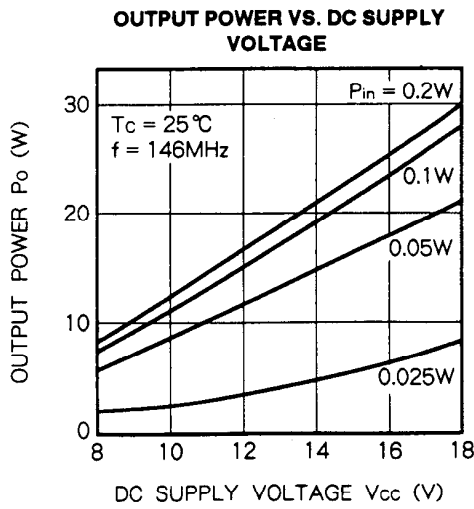
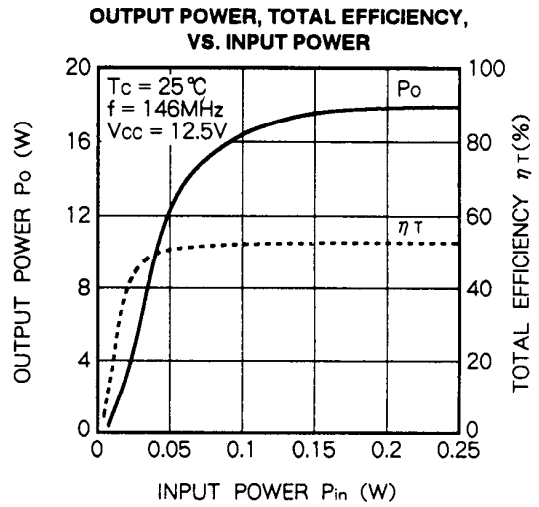
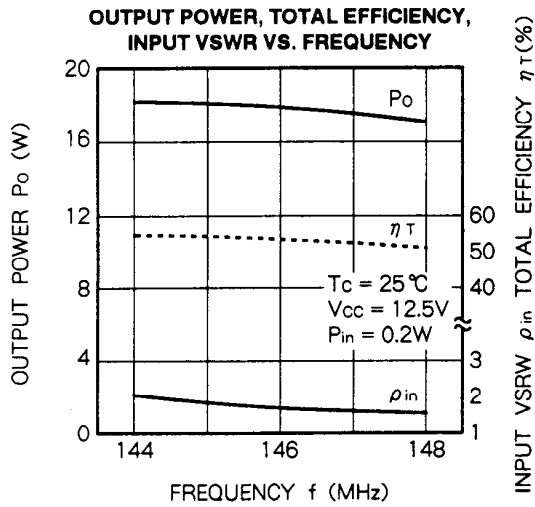
Note. Above parameters are guaranteed independently.

### ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	Pin = 0.2W Vcc = 12.5V ZG = ZL = 50 Ω	144	148	MHz
Po	Output power		13		W
ηT	Total efficiency		48		%
2fo	2nd. harmonic			- 25	dBc
3fo	3rd. harmonic			- 35	dBc
ρin	Input VSWR			2.8	-
-	Load VSWR tolerance	Vcc = 15.2V Po = 14W (Pin : controlled) ρL = 20 : 1 (All phase) ZG = 50 Ω	No degradation or destroy		-

Note. Above parameters, ratings, limits and conditions are subject to change.

TYPICAL PERFORMANCE DATA



**DESIGN CONSIDERATION OF HEAT RADIATION**

Please refer to following consideration when designing heat sink.

**1. Junction temperature of incorporated transistors at standard operation.**

(1) Thermal resistance between junction and package of incorporated transistors.

a) First stage transistor

$$R_{th(j-c)1} = 10\text{ }^{\circ}\text{C/W(Typ.)}$$

b) Final stage transistor

$$R_{th(j-c)2} = 3\text{ }^{\circ}\text{C/W(Typ.)}$$

(2) Junction temperature of incorporated transistors at standard operation.

- Conditions for standard operation.

$P_o = 13\text{W}$ ,  $V_{cc} = 12.5\text{V}$ ,  $P_{in} = 0.2\text{W}$ ,  $\eta T = 48\%$  (minimum rating).  $P_{o1}(\text{Note1}) = 2.5\text{W}$ ,  $I_T = 2.2\text{A}(I_{T1}(\text{2}) = 0.45\text{A}$ ,  $I_{T2}(\text{3}) = 1.75\text{A}$ )

Note1 : Output power of the first stage transistor

Note2 : Circuit current of the first stage transistor

Note3 : Circuit current of the first stage transistor

- Junction temperature of the first stage transistor

$$T_{j1} = (V_{cc} \times I_{T1} - P_{o1} + P_{in}) \times R_{th(j-c)1} + T_c(\text{4})$$

$$= (12.5 \times 0.45 - 2.5 + 0.2) \times 10 + T_c$$

$$= 33 + T_c(\text{ }^{\circ}\text{C})$$

Note4 : Package temperature of device

- Junction temperature of the final stage transistor

$$T_{j2} = (V_{cc} \times I_{T2} - P_o + P_{o1}) \times R_{th(j-c)2} + T_c$$

$$= (12.5 \times 1.75 - 13 + 2.5) \times 3 + T_c$$

$$= 34 + T_c(\text{ }^{\circ}\text{C})$$

**2. Heat sink design**

In thermal design of heat sink, try to keep the package temperature at the upper limit of the operating ambient temperature (normally  $T_a = 60\text{ }^{\circ}\text{C}$ ) and at the output power of 13W below  $90\text{ }^{\circ}\text{C}$ .

The thermal resistance  $R_{th(c-a)}(\text{5})$  of the heat sink to realize this :

$$R_{th(c-a)} = \frac{T_c - T_a}{(P_o / \eta T) - P_o + P_{in}} = \frac{90 - 60}{(13 / 0.48) - 13 + 0.2} = 2.8(\text{ }^{\circ}\text{C/W})$$

Note5 : Inclusive of the contact thermal resistance between device and heat sink

Mounting the heat sink of the above thermal resistance on the device,

$$T_{j1} = 113\text{ }^{\circ}\text{C}$$
,  $T_{j2} = 134\text{ }^{\circ}\text{C}$  at  $T_a = 60\text{ }^{\circ}\text{C}$ ,  $T_c = 90\text{ }^{\circ}\text{C}$ ,

In the annual average of ambient temperature is  $30\text{ }^{\circ}\text{C}$ ,

$$T_{j1} = 103\text{ }^{\circ}\text{C}$$
,  $T_{j2} = 104\text{ }^{\circ}\text{C}$

As the maximum junction temperature of these incorporated transistors  $T_{jmax}$  are  $175\text{ }^{\circ}\text{C}$ , application under fully derated condition is ensured.