■ OVERVIEW

The SM5617 series are C-MOS ICs for quartz crystal oscillating module. Each IC has a high frequency oscillating circuit and an output buffer with low current consumption.
There are many kinds of type - output level-TTL or CMOS, output driverbility - 10TTL or 10LSTTL. (Refer to the SERIES TABLE).
The SM5617 series also incorporate built-in feed back resistance made of high accuracy Thin Film resistance and built-in capacitor having excellent frequency characteristics, so it enables stable third overtone oscillation without any external parts.

■ FEATURES

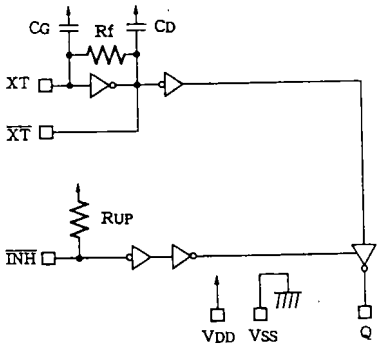
- Available up to 70MHz
- For a third overtone wave use
- Built-in feed back resistance of oscillating circuit
- Built-in capacitor of oscillating circuit
- 3-state function
- TTL compatible I/O interface
- Low current consumption
- Operating voltage
  4.0 to 6.0V (22MHz ≤ f0 ≤ 50MHz)
  4.5 to 5.5V (50MHz < f0 ≤ 70MHz)
- Chip form
- Molybdenum gate C-MOS

■ PIN DESCRIPTION

NAME	FUNCTION
XT	Input terminal for oscillating
$\overline{XT}$	Output terminal for oscillating
$\overline{INH}$	"L" High impedance On-chip pull-up resistance
V_{DD}	Power supply
V_{SS}	Ground
Q	Output (fo)

fo: Oscillating frequency

■ BLOCK DIAGRAM



■ SERIES TABLE

VERSIONS	Frequency Range (MHz)	Output Duty Level	Output Driverbility
SM5617NA	30 to 42	CMOS	10TTL
NB	33 to 45	CMOS	10TTL
NC	36 to 48	CMOS	10TTL
ND	39 to 52	CMOS	10TTL
NE	48 to 70	CMOS	10TTL
NF	22 to 34	CMOS	10TTL
HA	30 to 42	CMOS	10LSTTL
HB	33 to 45	CMOS	10LSTTL
HC	36 to 48	CMOS	10LSTTL
HD	39 to 52	CMOS	10LSTTL
HE	48 to 60	CMOS	10LSTTL
HF	22 to 34	CMOS	10LSTTL
KA	30 to 42	TTL	10TTL
KB	33 to 45	TTL	10TTL
KC	36 to 48	TTL	10TTL
KD	39 to 52	TTL	10TTL
KE	48 to 70	TTL	10TTL
KF	22 to 34	TTL	10TTL

■ ABSOLUTE MAXIMUM RATING

(V_{SS}=0V)

ITEM	SYMBOL	CONDITIONS	UNIT
Supply voltage	V_{DD}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	-0.5 to V_{DD}+0.5	V
Storage temperature	T_{STG}	-65 to +150	°C

■ RECOMMENDED OPERATIONAL CONDITIONS

(V_{SS}=0V)

ITEM	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	22MHz ≤ f_o ≤ 40MHz, C_L ≤ 50pF	V_{DD}	4.0	5.0	6.0	V
	40MHz ≤ f_o ≤ 50MHz, C_L ≤ 50pF		4.0	5.0	6.0	
	40MHz ≤ f_o ≤ 50MHz, 15pF < C_L ≤ 50pF		4.5	5.0	5.5	
	50MHz ≤ f_o ≤ 60MHz, C_L ≤ 15pF (H versions)		4.5	5.0	5.5	
	50MHz ≤ f_o ≤ 70MHz, C_L ≤ 15pF (K, N versions)		4.5	5.0	5.5	
Input voltage		V_{IN}	V_{SS}		V_{DD}	V
Operating temperature	22MHz ≤ f_o ≤ 50MHz	T_{OPR}	-20		+80	°C
	50MHz ≤ f_o ≤ 60MHz (H versions)		-15		+75	
	50MHz ≤ f_o ≤ 70MHz (K, N versions)		-15		+75	

■ ELECTRICAL CHARACTERISTICS

1. N Versions

(24MHz ≤fo≤50MHz, Vss=0V, Ta=-20 to +80°C) or
(50MHz ≤fo≤60MHz, Vss=0V, Ta=-15 to +75°C) unless otherwise noted

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output voltage ("H" level)	V_{OH}	Q terminal Fig. 1	V_{DD}=4.5V, I_{OH}=16.0mA		3.9	4.2		V
			V_{DD}=4.0V, I_{OH}=14.4mA		3.4	3.7		
Output voltage ("L" level)	V_{OL}		V_{DD}=4.5V, I_{OH}=16.0mA			0.3	0.4	
			V_{DD}=4.0V, I_{OH}=14.4mA			0.3	0.4	
Output leak current	I_Z	Q terminal, Fig. 1	V_{OH}=V_{DD}				10	μA
		$\overline{INH}$=L, V_{DD}=6.0V	V_{OL}=V_{SS}				10	
Input voltage ("H" level)	V_{IH}	$\overline{INH}$ terminal	V_{DD}=5±0.5V		20			V
			V_{DD}=5±1.0V		2.2			
Input voltage ("L" level)	V_{IL}		V_{DD}=5±1.0V				0.8	
Current consumption	I_{DD1}	Load Circuit 1 Fig. 2 CL=15pF $\overline{INH}$=OPEN	SM5617NA,N,B,NC f=40MHz	V_{DD}= 4.0-6.0V		20	40	mA
			SM5617ND f=50MHz	V_{DD}= 4.0-6.0V		23	45	
			SM5617NE f=70MHz	V_{DD}= 4.5-5.5V		33	50	
			SM5617NE f=30MHz	V_{DD}= 4.0-6.0V		15	35	
	I_{DD2}	Load Circuit 1 Fig. 2 CL=50pF $\overline{INH}$=OPEN	SM5617NA,NB,NC f=40MHz	V_{DD}= 4.0-6.0V		30	50	mA
			SM5617ND f=50MHz	V_{DD}= 4.5-5.5V		33	50	
			SM5617NF f=30MHz	V_{DD}= 4.0-6.0V		25	45	
Pull-up resistance	R_{UP}	$\overline{INH}$ terminal, Fig. 3			50		250	kΩ
Feed back resistance	Rf	Fig. 4	SM5617NA, NF		4.1	4.5	5.0	kΩ
			SM5617NB		3.5	3.9	4.3	
			SM5617NC		3.0	3.3	3.6	
			SM5617ND, NE		2.4	2.7	3.0	
Built-in capacitor	C_G	SM5617NA, NB, NC, ND, NF			8.5	12	15.5	pF
	C_D				12	17	22	
	C_G	SM5617NE			7.0	10	13	pF
	C_D				7.0	10	13	

2. H Versions

(24MHz ≤fo≤50MHz, V_{SS}=0V, Ta=-20 to +80°C) or
(50MHz ≤fo≤60MHz, V_{SS}=0V, Ta=-15 to +75°C) unless otherwise noted

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output voltage ("H" level)	V_{OH}	Q terminal Fig. 1	V_{DD}=4.5V,	I_{OH}=4.0mA	3.9	4.2		V
			V_{DD}=4.0V,	I_{OH}=3.6mA	3.4	3.7		
Output voltage ("L" level)	V_{OL}		V_{DD}=4.5V,	I_{OH}=4.0mA		0.3	0.5	
			V_{DD}=4.0V,	I_{OH}=3.6mA		0.3	0.5	
Output leak current	I_Z	Q terminal, Fig. 1 $\overline{INH}$=L, V_{DD}=6.0V	V_{OH}=V_{DD}				10	µA
			V_{OL}=V_{SS}				10	
Input voltage ("H" level)	V_{IH}	$\overline{INH}$ terminal	V_{DD}=5±0.5V		20			V
			V_{DD}=5±1.0V		2.2			
Input voltage ("L" level)	V_{IL}		V_{DD}=5±1.0V				0.8	
Current consumption	I_{DD1}	Load Circuit 1 Fig. 2 CL=15pF $\overline{INH}$=OPEN	SM5617HA,HB,HC f=40MHz	V_{DD}= 4.0 to 6.0V		18	36	mA
			SM5617HD f=50MHz	V_{DD}= 4.0 to 6.0V		20	40	
			SM5617HE f=70MHz	V_{DD}=4.5 to 5.5V Ta=-15 to +75°C		25	40	
			SM5617HE f=30MHz	V_{DD}= 4.0 to 6.0V		13	33	
Pull-up resistance	R_{UP}	$\overline{INH}$ terminal, Fig. 3			50		250	kΩ
Feed back resistance	Rf	Fig. 4	SM5617HA, HF		4.1	4.5	5.0	kΩ
			SM5617HB		3.5	3.9	4.3	
			SM5617HC		3.0	3.3	3.6	
			SM5617HD, HE		2.4	2.7	3.0	
Built-in capacitor	C_G	SM5617HA, HB, HC, HD, HF			8.5	12	15.5	pF
	C_D				12	17	22	
	C_G	SM5617HE			7.0	10	13	pF
	C_D				7.0	10	13	

3. K Versions

(24MHz ≤fo≤50MHz, V_{SS}=0V, Ta=-20 to +80°C) or
(50MHz ≤fo≤60MHz, V_{SS}=0V, Ta=-15 to +75°C) unless otherwise noted

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output voltage ("H" level)	V_{OH}	Q terminal Fig. 1	V_{DD}=4.5V,	I_{OH}=16.0mA	3.9	4.2		V
			V_{DD}=4.0V,	I_{OH}=14.4mA	3.4	3.7		
Output voltage ("L" level)	V_{OL}		V_{DD}=4.5V,	I_{OH}=16.0mA		0.3	0.4	
			V_{DD}=4.0V,	I_{OH}=14.4mA		0.3	0.4	
Output leak current	I_Z	Q terminal, Fig. 1 $\overline{INH}$=L, V_{DD}=6.0V	V_{OH}=V_{DD}				10	µA
			V_{OL}=V_{SS}				10	
Input voltage ("H" level)	V_{IH}	$\overline{INH}$ terminal	V_{DD}=5±0.5V		20			V
			V_{DD}=5±1.0V		2.2			
Input voltage ("L" level)	V_{IL}		V_{DD}=5±1.0V				0.8	
Current consumption	I_{DD1}	Load Circuit 1 Fig. 2 CL=15pF $\overline{INH}$=OPEN	SM5617KA,KB,KC f=40MHz	V_{DD}= 4.0 to 6.0V		20	40	mA
			SM5617KD f=50MHz	V_{DD}= 4.0 to 6.0V		23	45	
			SM5617KE f=70MHz	V_{DD}=4.5 to 5.5V Ta=-15 to +75°C		33	50	
			SM5617KE f=30MHz	V_{DD}= 4.0 to 6.0V		13	35	
Pull-up resistance	R_{UP}	$\overline{INH}$ terminal, Fig. 3			50		250	kΩ
Feed back resistance	Rf	Fig. 4	SM5617KA, KF		4.1	4.5	5.0	kΩ
			SM5617KB		3.5	3.9	4.3	
			SM5617KC		3.0	3.3	3.6	
			SM5617KD, KE		2.4	2.7	3.0	
Built-in capacitor	C_G	SM5617KA, KB, KC, KD, KF			8.5	12	15.5	pF
	C_D				12	17	22	
	C_G	SM5617KE			7.0	10	13	pF
	C_D				7.0	10	13	

■ SWITCHING CHARACTERISTICS

1. N Versions

(24MHz ≤fo≤50MHz, V_{SS}=0V, Ta=-20 to +80°C) or
(50MHz ≤fo≤60MHz, V_{SS}=0V, Ta=-15 to +75°C) unless otherwise noted

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_{rl}	Fig. 2 Load Circuit 1	C_L=15pF	V_{DD}=5 ± 0.5V		2.0	4.0	ns
				V_{DD}=5 ± 1.0V			4.6	
	T_{r2}	0.1V_{DD} → 0.9V_{DD}	C_L=50pF	V_{DD}=5 ± 0.5V		4.0	8.0	
				V_{DD}=5 ± 1.0V			9.5	
Output fall time	T_{fl}	Fig. 2 Load Circuit 1	C_L=15pF	V_{DD}=5 ± 0.5V		2.0	4.0	ns
				V_{DD}=5 ± 1.0V			4.6	
	T_{f2}	0.9V_{DD} → 0.1V_{DD}	C_L=50pF	V_{DD}=5 ± 0.5V		4.0	8.0	
				V_{DD}=5 ± 1.0V			9.5	
Duty factor of fundamental output	DUTY	V_{DD}=5.0V Ta=25°C Fig. 2 Load Circuit 1	SM5617NA, NB, NC C_L=50pF f=40MHz		45		55	%
			SM5617ND C_L=50pF f=50MHz					
			SM5617NE C_L=15pF f=70MHz		40		60	
			SM5617NF C_L=50pF f=30MHz		45		55	
Output disable time	T_{PLZ}	Fig. 2, Ta=25°C, V_{DD}=5±1.0V					100	ns
	T_{PLZ}	Load C_L ≤50pF (SM5617NE: V_{DD}=5±0.5V)					100	
Operating frequency range	f	Fig. 2 Load Circuit 1 *1	SM5617NA		30		42	MHz
			SM5617NB		33		45	
			SM5617NC		36		48	
			SM5617ND		39		52	
			SM5617NE		48		70	
			SM5617NF		22		34	

2. H Versions

(24MHz ≤fo≤50MHz, V_{SS}=0V, Ta=-20 to +80°C) or
(50MHz ≤fo≤60MHz, V_{SS}=0V, Ta=-15 to +75°C) unless otherwise noted

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_{rl}	Fig. 2 Load Circuit 1	C_L=15pF	V_{DD}=5 ± 0.5V		5.0	8.0	ns
				V_{DD}=5 ± 1.0V			10.0	
	T_{r2}	0.1V_{DD} → 0.9V_{DD}	C_L=50pF	V_{DD}=5 ± 0.5V		13.0	21.0	
				V_{DD}=5 ± 1.0V			26.0	
Output fall time	T_{fl}	Fig. 2 Load Circuit 1	C_L=15pF	V_{DD}=5 ± 0.5V		5.0	8.0	ns
				V_{DD}=5 ± 1.0V			10.0	
	T_{f2}	0.1V_{DD} → 0.9V_{DD}	C_L=50pF	V_{DD}=5 ± 0.5V		13.0	21.0	
				V_{DD}=5 ± 1.0V			26.0	
Duty factor of fundamental output	DUTY	V_{DD}=5.0V Ta=25°C Fig. 2 Load Circuit 1	SM5617HA, HB, HC C_L=50pF f=40MHz		45		55	%
			SM5617HD C_L=50pF f=50MHz		45		55	
			SM5617HE C_L=15pF f=60MHz		40		60	
			SM5617HF C_L=50pF f=30MHz		45		55	
Output disable time	T_{PLZ}	Fig. 2, Ta=25°C, V_{DD}=5±1.0V					100	ns
	T_{PLZ}	Load C_L ≤50pF (SM5617HE: V_{DD}=5±0.5V)					100	
Operating frequency range	f	Fig. 2 Load Circuit 1 *1	SM5617HA		30		42	MHz
			SM5617HB		33		45	
			SM5617HC		36		48	
			SM5617HD		39		52	
			SM5617HE		48		60	
			SM5617HF		22		34	

*1: Recommended operating conditions will change in accordance with operating frequency. (See Recommended Operating Conditions.)

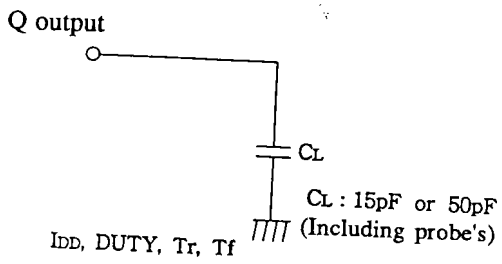
3. K Versions

(24MHz ≤fo≤50MHz, V_{SS}=0V, Ta=-20 to +80°C) or
(50MHz ≤fo≤60MHz, V_{SS}=0V, Ta=-15 to +75°C) unless otherwise noted

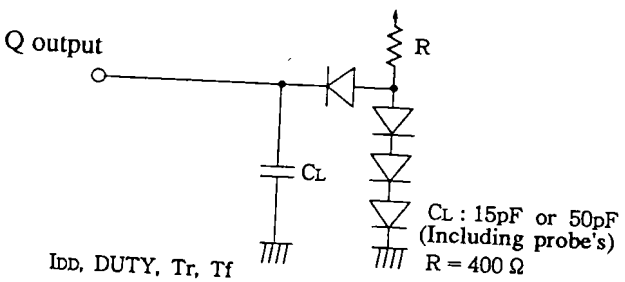
ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_{r1}	Fig. 2 Load Circuit 2	C_L=15pF	V_{DD}=5 ± 0.5V		1.5	3.0	ns
				V_{DD}=5 ± 1.0V			3.5	
	T_{r2}	0.4V_{DD} → 2.4V_{DD}	C_L=50pF	V_{DD}=5 ± 0.5V		3.0	6.0	
				V_{DD}=5 ± 1.0V			7.0	
Output fall time	T_{f1}	Fig. 2 Load Circuit 2	C_L=15pF	V_{DD}=5 ± 0.5V		1.5	3.0	ns
				V_{DD}=5 ± 1.0V			3.5	
	T_{f2}	2.4V_{DD}→ 0.4V_{DD}	C_L=50pF	V_{DD}=5 ± 0.5V		3.0	6.0	
				V_{DD}=5 ± 1.0V			7.0	
Duty factor of fundamental output	DUTY	V_{DD}=5.0V Ta=25°C Fig. 2 Load Circuit 2	SM5617KA, KB, KC C_L=50pF f=40MHz		45		55	%
			SM5617KD C_L=50pF f=50MHz		45		55	
			SM5617KE C_L=15pF f=60MHz		40		60	
			SM5617KF C_L=50pF f=30MHz		45		55	
Output disable time	T_{PLZ}	Fig. 2, Ta=25°C, V_{DD}=5±1.0V					100	ns
	T_{PLZ}	Load C_L ≤50pF (SM5617KE: V_{DD}=5±0.5V)					100	
Operating frequency range	f	Fig. 2 Load Circuit 1 *1	SM5617KA		30		42	MHz
			SM5617KB		33		45	
			SM5617KC		36		48	
			SM5617KD		39		52	
			SM5617KE		48		70	
			SM5617KF		22		34	

*1: Recommended operating conditions will change in accordance with operating frequency. (See Recommended Operating Conditions.)

■ LOAD CIRCUIT



Load Circuit 1 (N, H versions)



Load Circuit 2 (K versions)

■ TEST CIRCUIT

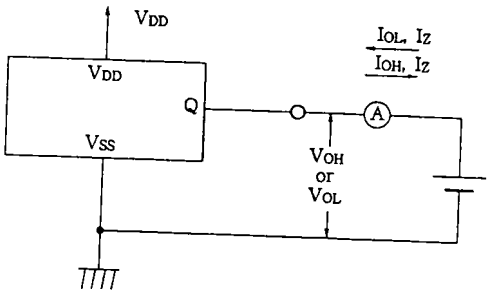


Fig. 1

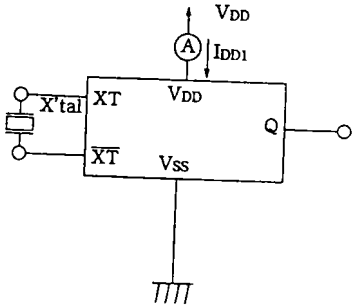


Fig. 2

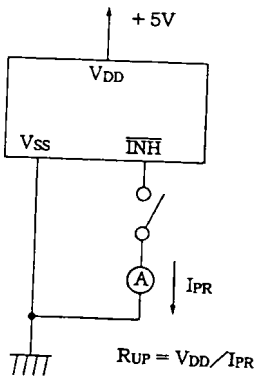


Fig. 3

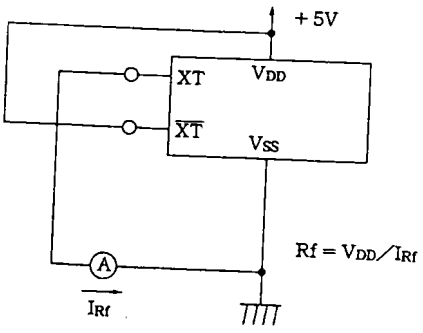
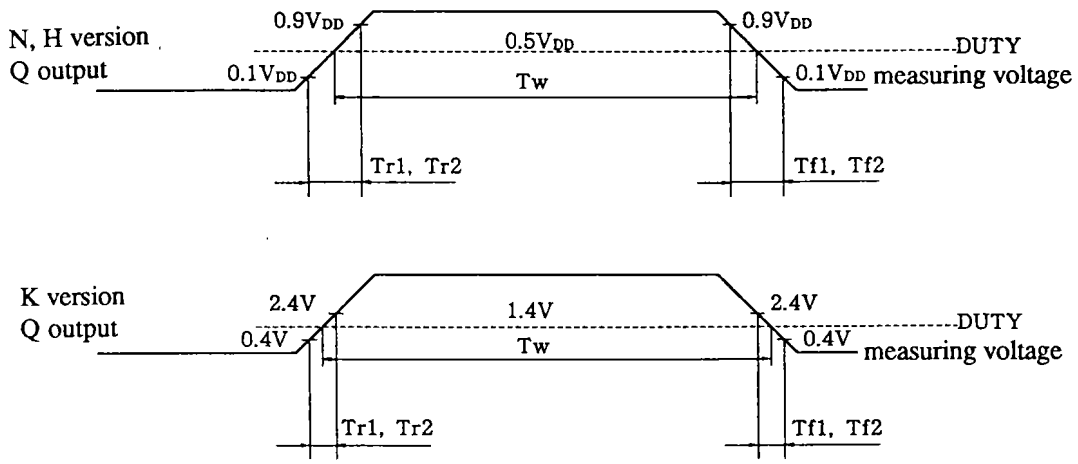
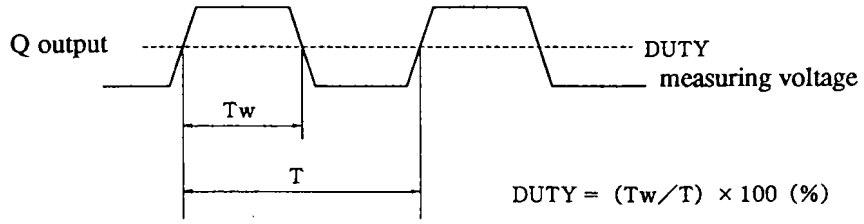


Fig. 4

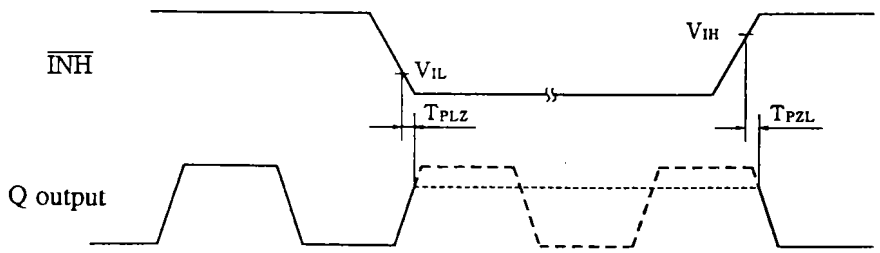
■ WAVEFORMS FOR SWITCHING TIME



■ DUTY FACTOR



■ OUTPUT DISABLE TIME

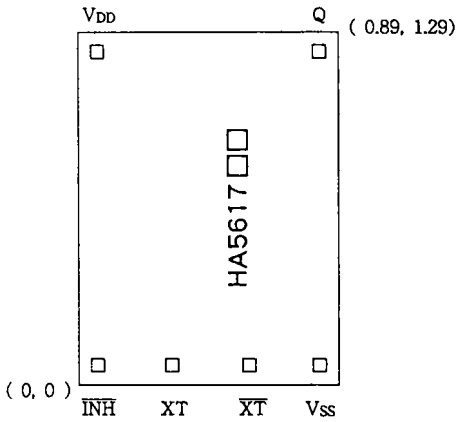


■ FUNCTION

VERSIONS	Output frequence
$\overline{INH}$	Q
H (OPEN)	Output (f_o)
L	High impedance

f_o : Oscillating frequency

■ PAD LOCATION (Unit: mm)



CHIP SIZE: 0.89 × 1.29mm

CHIP THICKNESS: 400 ±30 µm

■ PAD COORDINATES

UNIT: µm

NAME	X	Y
$\overline{INH}$	145	140
XT	345	140
$\overline{XT}$	545	140
VSS	745	140
Q	745	1150
VDD	145	1155