TOSHIBA INTEGRATED CIRCUIT
TECHNICAL DATA

CMOS DIGITAL INTEGRATED CIRCUIT
TC35190F
SILICON MONOLITHIC

TC35190F (Video-data Compression and Expansion Controller*) 1988-11-03

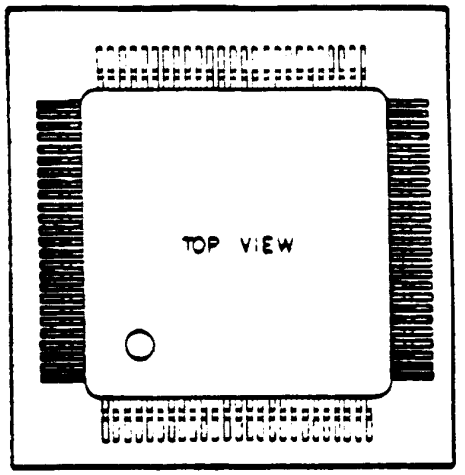
DESCRIPTION

TC35190F (VCEC*) performs encoding and decoding of video-data based on the CCITT Recommendations T.4 and T.6.

Only with simple initialization, the VCEC* processes a page of data without any host processer's help.

FEATURES

- High speed data transfer
- 3 independent 8-bit buses
- Directly connectable with Intel/Zilog 8bit MPU
- Can access maximum 8k-byte line memory
- Horizontal video sizes from 32 to 7736pels/line
- A variety of processing mode by parameter set-up
  - Minimum number of transmission bit
  - Line-Pad-Bit
  - Number of 'RTC' component 'EOL'
  - Number of 'RTC' detective 'EOL'
- 8-bit error line counter
- C-MOS Low Power (Typical 100 mA)
- +5V single power supply
- LFP100 Plastic Package



No	Name	No	Name	No	Name	No	Name
1	VDD	26	T6	51	MDC	76	VSS
2	CD0	27	$\overline{RAS}$	52	MD1	77	IRQ
3	CD1	28	$\overline{WR}$	53	MD2	78	$\overline{PREQ}$
4	CD2	29	$\overline{CAS}$	54	MD3	79	$\overline{PACK}$
5	CD3	30	VDD	55	VDD	80	$\overline{VR}$
6	VSS	31	VSS	56	VSS	81	$\overline{RES}$
7	VDD	32	MA12	57	MD4	82	VSS
8	CD4	33	MA11	58	MD5	83	VDD
9	CD5	34	MA10	59	MD6	84	D0
10	CD6	35	MA9	60	MD7	85	D1
11	CD7	36	MA8	61	VDD	86	D2
12	VDD	37	VDD	62	VDD	87	D3
13	VSS	38	VSS	63	VSS	88	VSS
14	VSS	39	MA7	64	VSS	89	VDD
15	VDD	40	MA6	65	PD0	90	D4
16	$\overline{CREQ}$	41	MA5	66	PD1	91	D5
17	$\overline{CACK}$	42	MA4	67	PD2	92	D6
18	$\overline{T1}$	43	VDD	68	PD3	93	D7
19	$\overline{T2}$	44	VSS	69	VDD	94	VSS
20	$\overline{T3}$	45	MA3	70	VSS	95	A0
21	$\overline{T4}$	46	MA2	71	PD4	96	A1
22	$\overline{T5}$	47	MA1	72	PD5	97	$\overline{CS}$
23	CLK	48	MA0	73	PD6	98	$\overline{RD}$
24	VSS	49	VSS	74	PD7	99	VSS
25	VDD	50	VDD	75	VDD	100	VDD

Absolute Maximum Ratings

Item	Symbol	Rated Value	Unit
Supply Voltage	VDD	− 0.5 ~ 7.0	V
Input Voltage	Vin	− 0.5 ~ 7.0	V
Output Voltage	Vout	− 0.5 ~ 7.0	V
Operating Temperature	Topr	0 ~ 70	℃
Strage Temperature	Tstg	− 55 ~ 150	℃
Soldering Temperature	Tsol	260℃ · 10 sec	

TOSHIBA INTEGRATED CIRCUIT TECHNICAL DATA

TC35190F

PIN DESCRIPTION

□ System Terminals

Pin Name	I/O	Functions
VDD	Input	Connect +5V
VSS	Input	Connect +5V
CLK	Input	Input VCEC+ system clock
RES	Input	When VCEC+ is reset by hardware, this pin is set at 'L' level
IRQ	Output	Interrupt request signal to 'MPU'

□ MPU BUS Control Terminals

Pin Name	I/O	Functions	
CS	Input	When 'MPU' access VCEC+, this pin is set at 'L' level	
RD	Input	When 'MPU' reads data from internal register, this pin is set at 'L' level	
WR	Input	When 'MPU' writes data into internal register, this pin is set at 'L' level	
A0 A1	Input	Internal register selecting address	
D0	I/O 3State	This pin is LSB	8-bit bus to read/write data from/into internal Register Connect 'MPU' data buses
D1			
D2			
D3			
D4			
D5			
D6			
D7		This pin is MSB	

□ PIX BUS Control Terminals

Pin Name	I/O	Functions		
PREQ	Output	Signal requesting data transfer to Scanner & Printer side		
PACK	Input	Response signal from the Scanner & Printer side to 'PREQ' signal		
PD0	I/O 3State	— This pin is LSB	—	Decoding mode • PIX data output
PD1		e	—	Decoding mode • Enable signal input
PD2		—	e	Decoding mode • Synchronous signal input
PD3		—	—	Decoding mode • Line-End signal output
PD4		e	b	
PD5		b	e	Encoding mode • Synchronous signal input
PD6		e	s	Encoding mode • Enable signal input
PD7		e This pin is MSB		Encoding mode • PIX data input

Note) Serial mode is future function. Not supported !

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TOSHIBA INTEGRATED CIRCUIT
TECHNICAL DATA

TC35190F

□ CODE BUS Control Terminals

Pin Name	I/O	Functions			
CREQ	Output	Signal requesting data transfer to Communication-Line & data-storage side			
CACK	Input	Response signal from Communication-Line & data-storage side to 'CREQ' signal			
CD0	I/O 3State	—	This pin is LSB	—	Encoding mode • data output CODE
CD1		—		—	Encoding mode • Enable signal input
CD2		—		—	Encoding mode • Synchronous signal input
CD3		—		—	
CD4		—		—	
CD5		—		—	Decoding mode • Synchronous signal input
CD6		—		—	Decoding mode • Enable signal input
CD7		—	This pin is MSB	—	Decoding mode • data input CODE

(Note) Serial mode is future function. Not supported !

□ Line-Memory Control Terminals

Pin Name	I/O	Functions	
RAS	Output	Reserved. Use in open state. For future connection of Dynamic RAM.	
CAS	Output	Use for 'OE' signal of Static RAM. ('CAS' signal of Dynamic RAM)	
MWR	Output	Use for 'Write' signal of RAM	
MD0	I/O 3State	This pin is LSB	8-bit buses for exchanging data with Line memory
MD1			
MD2			
MD3			
MD4			
MD5			
MD6			
MD7		This pin is MSB	
MA0	Output	This pin is LSB	18-bit address signals of RAM.
MA1			
MA2			
MA3			
MA4			
MA5			
MA6			
MA7			
MA8			
MA9			
MA10			
MA11			
MA12		This pin is MSB	

(Note) Dynamic RAM is not supported !

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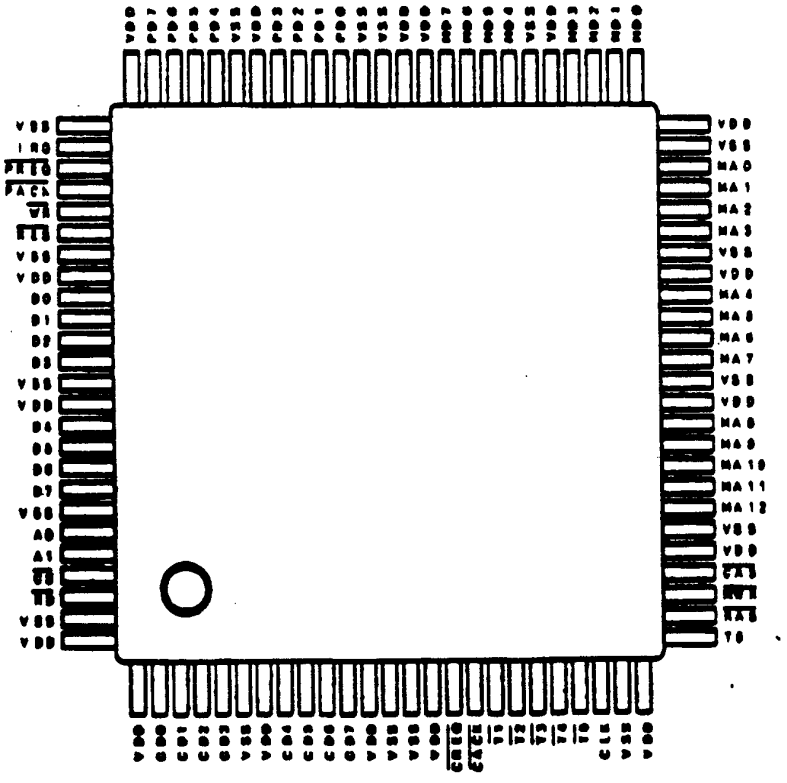
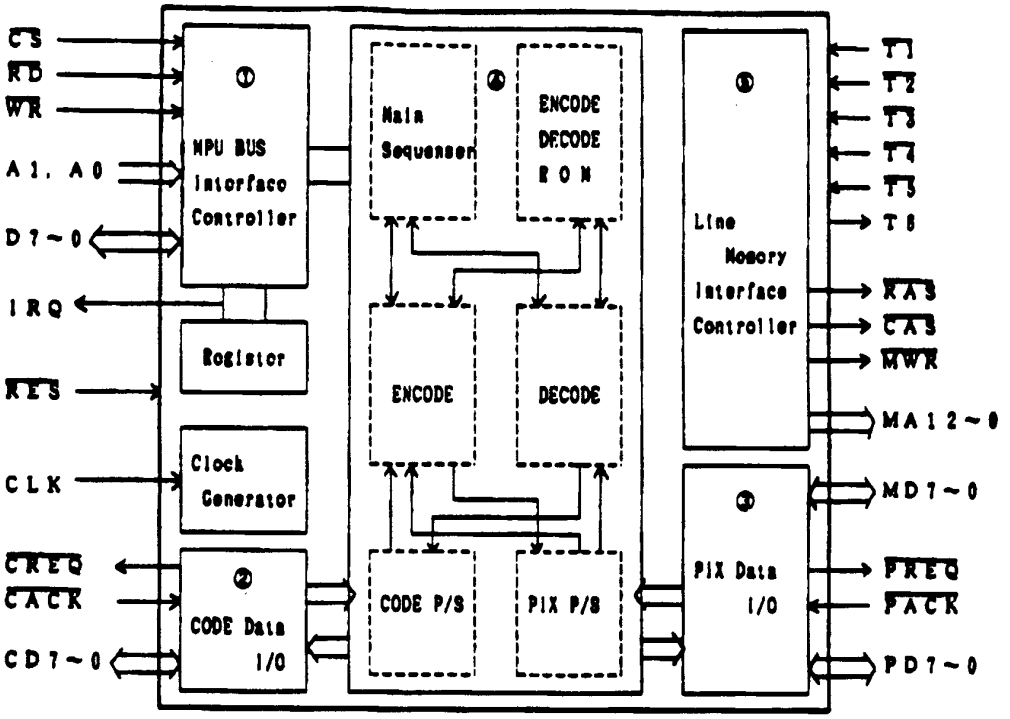
□ Test Terminals

Pin Name	I/O	Functions
T 1	Input	Test terminal 1. Keep at 'H' level during normal operation.
T 2	Input	Test terminal 2. Keep at 'H' level during normal operation.
T 3	Input	Test terminal 3. Keep at 'H' level during normal operation.
T 4	Input	Test terminal 4. Keep at 'H' level during normal operation.
T 5	Input	Test terminal 5. Keep at 'H' level during normal operation.
T 6	Output	Test terminal 6. Use in 'OPEN' state during normal operation.



BLOCK DIAGRAM



Internal Block Diagram

① MPU BUS Interface Block

This block consists of the MPU BUS interrface.connectable with 80Series MPU.and Registers. Processing mode is set by write access operations. If the IMR (Interrupt Mask Register) is set at un-masking mode. the VCEC* drives the 'IRQ' signal at High level. whenever the 'IRQ' item is occurred. The host processer finds the operating status or interrupt request item by reading operation.

② CODE BUS Interface Block

This block controlls the coded-data transfer timing. Coded-data-BUS (CD7-0)connects to the 'Communication Line' or 'Data storage memorys'. When the VCEC * prepare for the coded-data. the 'CREQ' signal is active. More detailed timing. refer to after page : CODE BUS AC Timing.

③ PIX BUS Interface Block

This block controlls the Pix-data transfer timing. Pix-data-BUS(PD7-0) connects to the Scanner and Printer side. When the Line-memory has enough space for data storage. the 'PREQ' signal is active. More detailed timing. refer to after page : PIX BUS AC Timing.

⑦ Encoding and Decoding Block

This block consists of 'the Main Sequencer','Code/Decode ROM','Coding control','Decoding-control','Code-data parallel to sereal transfer' and 'Pix-data parallel to sereal transfer'

☐ Main sequencer unit

Controlls each block of VCEC° according as the micro-progras stored in Main-Sequencer-ROM. This is compatible with CCITT recommendations T.4 and T.6 for Group-III and Group IV facsimile. [Modified Huffman coding / Modified READ / Modified Modified READ]

☐ Code/Decode ROM unit

Consists of 3-Encoding ROMs and 3-Decoding ROMs.

Encoding ROM : Run-Length ROM . Encoding mode set ROM . Minium Number of Transition bit set ROM

Decoding ROM : Run-Length ROM . Decoding mode set ROM . Uncompressed mode decoding ROM

☐ Encoding unit

Detects color changing point. and generates coded-data using MH.MR.or.MMR coding algo-rithms.

☐ Decoding unit

Compares the data with code-table. and generates the video-image-data corresponding with Run-Length Decode ROM.

☐ Video-image-data parallel to serial converter unit

In the case of encoding. 8-bit parallel Video-image-data. inputs from PIX BUS inter-face. converts into serial data. And send to Encoding unit. In the case of decoding. serial to parallel conversion is carried out.

☐ Coded-data parallel to serial converter unit

This unit acts in similar fasion. as video-image-data parallel to serial converter unit. But. in this unit. parallel to serial conversion carries out in decoding operation. Serial to parallel conversion is in encoding operation.

⑧ Line memory Interface controll Block

This block consists of Memory address BUS (18 bit). and Memory controll signals (RAS . CAS . WWR). Controlls Write/Readaccess timing ; Stops write operation before the line-memory becomes full. or stops read operation before short. In the case of decoding. if any error occurs. performs the pre-coding line substitution.

OPERATIONAL DESCRIPTION

□ Summary

The VCEC* is facsimile CODEC Processor. After initialization, the VCEC* processes a page of data automatically. If the document consists of more than one sheet, initialization processure should be done before coding (decoding) starts. More details of initialization process explains after page : Initialization and Termination Process

Note) Following sentence '1' means High level input
'0' means Low level input
'H' means High level output
'L' means Low level output

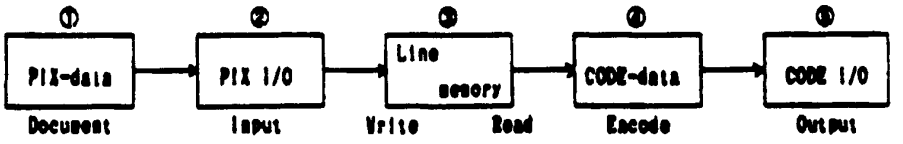
□ Encoding

When 'STRT' bit of the System Control1 Set Register (SCSR), is set at '1', then coding process starts. Coded-data generates according to the coding algorithm, setting in Register by initialization. In case of coding, PIX BUS Interface functions as INPUTS, and CODE BUS interface functions as OUTPUTS. If the system detects 'PREQ' is 'L', MPU should be ready for PIX-data, and keeps 'PACK' signal at '0' for the resolving time. Data is gotten by system in rising edge of 'PACK', and stored in the line memory. When this stored data reaches a set-up paper width, the coding is started. A coded-data is generated whenever the VCEC* detects changeing color point. Father, the 'EOL' code is generated every line's data has been coded. In the CODE BUS interface, a valid data is output during 'CACK' is at '0'. When the MH or MR coding is started, the system generates the End-Of-Line code (EOL) at first. After PIX-data has been input, the MPU should be done Terminating processure. When the VCEC* is set to Waiting-mode, the data remains in the line memory, is encoded.

After this, Return-To-Control code (RTC) is generated. In this time, 'PHD' bit of the Interrupt Mask Register (IMR) is active, then 'IRQ' becomes 'H'. After coding a page of data, if the document has next page, MPU could be done re-start processure. And whole pages data of the document has been coded, MPU sets the VCEC* is in initializing state.

In MMR codings, 'EOL' code is not using, then coded-data is generates serialcy. And End-Facsimile-Block code (EOFB) uses instead of 'RTC' code.

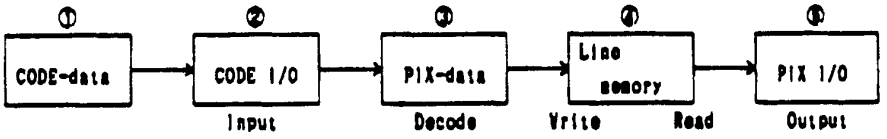
Note) PIX : picture element



Encoding mode Data Flow

□ Decoding

In the case of decoding, CODE BUS interface functions as INPUT, and PIX BUS interface functions as OUTPUT. The VCEC* decodes the coded-data, and it is stored in the line memory. When the MH or MR decoding mode is selected, the VCEC * searches 'EOL' code at first. If the coded-data contains any error, or the paper width could not be re-generated, the VCEC * prepares the previous decoded-line's data instead of this one. If the MMR mode is selected, the VCEC* stops all the operations after 'DERM' bit of Interrupt Request Register (IRR)is active. In this moment, VCEC* should be initialized again by host processor.



Decoding mode Data Flow

□ EOL code and RTC code

'EOL' code is composed of 11 bit of '0' + 1 bit of '1' : (000000000001). In practice, decoder recognizes 'EOL' code, detects more than 11 bit of '0' + 1 bit of '1'. In MR coding, the system using 'EOL'+'1' or 'EOL'+'0' for distinguish one-dimensional-coding-line or two-dimensional-coding-line. The one-dimensional coding line is encoded by using MH coding algorithm, and the two-dimensional-coding-line is encoded by MR. In coding side, the VCEC * transmits 6 or 9 times of 'EOL' codes continuously. In decoding side, a series of 2 or 6 times of 'EOL' codes detection means 'RTC' code detection. These are able to selects by Register setting. In MMR coding, 'EOFB' code is used, instead of 'RTC' code. 'EOFB' code composed of 2 times of 'EOL' code.

□ Fill-bit and Line-pad-bit

If every line's coded-data is less than Minimum Number Of Transmission Bit (MNTB), add '0' to the end of every line's coded-data, reaches to MNTB. This '0' data, additional coded-data is called Fill-bit. If the coded-data is not composed of in unit of byte, '0' data is added. This '0' data is called Line-pad-bit.

□ Transparent mode

If this mode is selected, the data is transmitted without coding, and received data is not decoded. This mode has a time lag, from data input to output. Because the data is stored in the line memory once, and it is not output until equivalent of one-line's data is stored.

□ White line skip mode

In this mode, if a coded-data of one-line composed of white pels only is short to 'MNTB', the system adds '0' data equivalent to a half of the 'MNTB'. For using in this mode, the MPU set at half of 'MNTB' by setting the 'MNTB' set bits of Transfer Register (PR).
ex.) the modem speed is 9600 bps : 10 ms/line

$$9600 \times 10E\text{-}3 = 96 \text{ (bit/sec)} \qquad 96 / 2 = 48 \text{ (bit/sec)}$$

In this case, 'MNTB' should be set 48 bit/line. More detail of 'MNTB' setting is explains at the following page : Parameter Register (Setting table for 'MNTB')

Register

VCEC* is able to a variety of processing mode by parameter set-up. The set-up depends on register setting by initialization. These registers are consists of 6-words of mode-set-registers and 4-words of status registers. In the first case, it is accessible to writing operation from MPU, and in the latter case, accessible to reading operation.

□ Mode set Registers

For setting the VCEC* 's processing mode (Writing Operation)

Register address		Access	Register Name
A 1	A 0		
0	0	1st.	SCSR Register (System Control Set Register)
0	1	1st.	IMR Register (Interrupt Mask Register)
1	0	1st.	RSR Register (RAM Size Register)
1	0	2nd.	PR Register (Parameter Register)
1	1	1st.	PWRL Register (Paper Width Register of Low)
1	1	2nd.	PWRH Register (Paper Width Register of High)

Note) In writing operation, if the register address is (A1,A0)=(1,0) or (A1,A0)=(1,1) is selected, the difference register is accessed in the first or the second access.

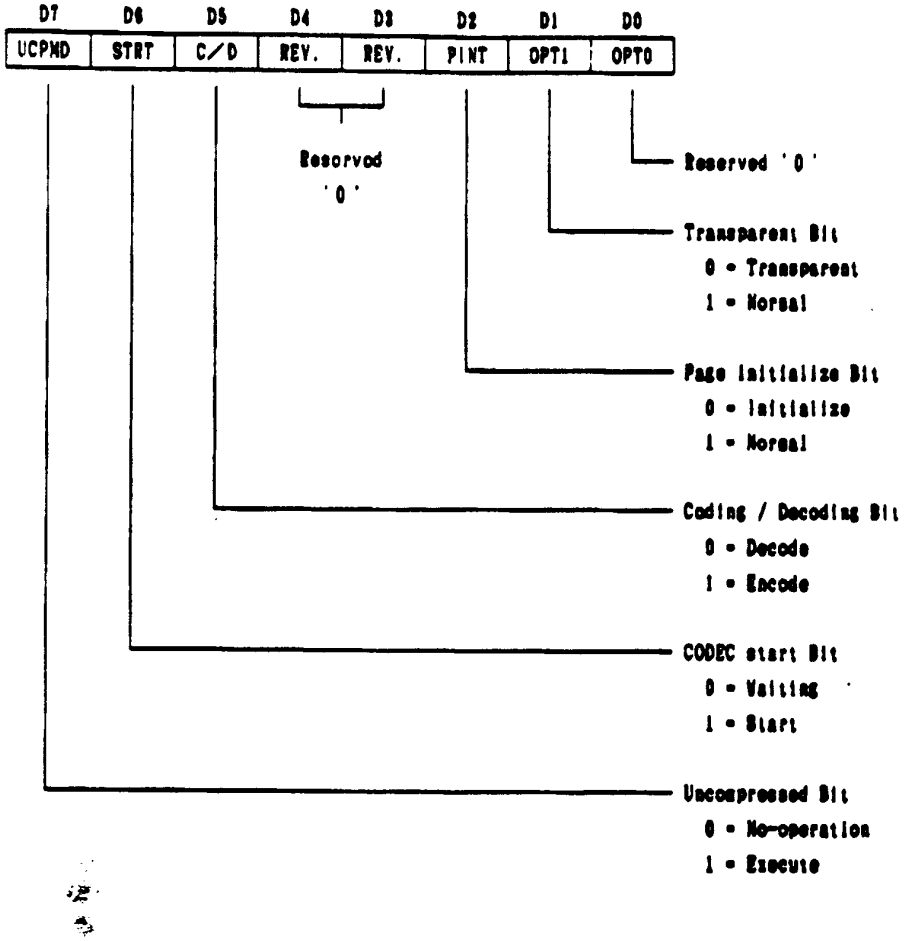
□ Status Registers

For indicating the VCEC* 's operating status (Read Operation)

Register address		Access	Register Name
A 1	A 0		
0	0	1st.	SCNR Register (System Control Notice Register)
0	1	1st.	IRR Register (Interrupt Request Register)
1	0	1st.	LSR Register (Line-memory Status Register)
1	1	1st.	ELR Register (Error Line Register)

Note) More details of Register setting are following topics ; Initialization and Termination process.

□ S C S R (System Controll Set Register)

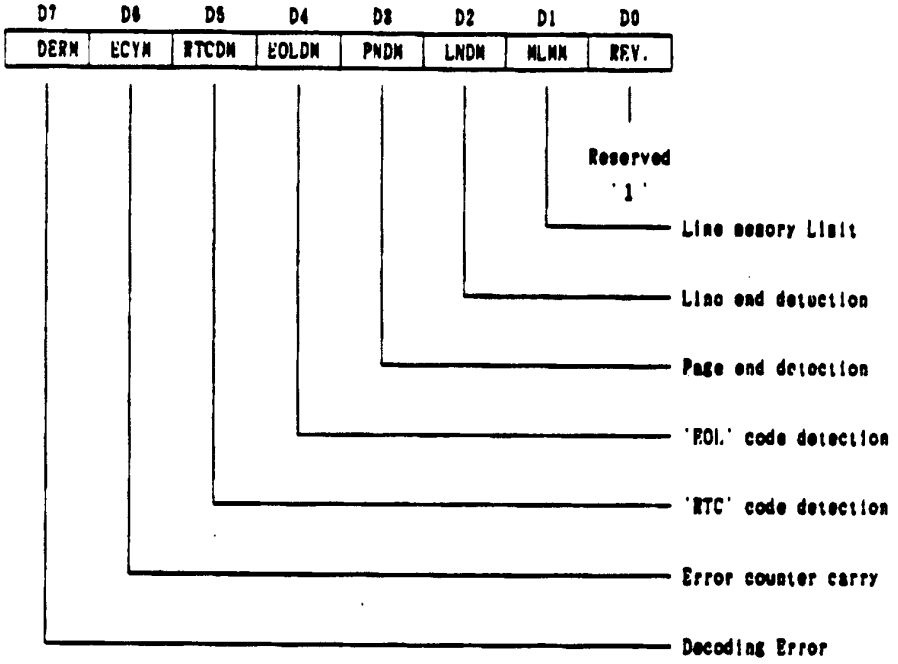


'SCSR' is accessible to writing operation by setting register address (A1.A0)=(0.0).

Bits D1 of 'SCSR' is Transparent mode set bit. The Transparent mode is explained by another topics : Operational Description. Page initialize bit should be set at 'initialize' whenever set-up the VCEC* .Coding/Decoding Bit selects the Coding or the Decoding. CODEC start Bit should be set at 'waiting' during initialization. Uncompressed Bit works in Decoding mode. Uncompressed mode is the optional cording of the Recommendation of T4 or T6. More details of this coding, refer to the Recommendation of CCITT.

Note) Reserve bits of this register are always set at ' 0 '

□ IMR (Interrupt Mask Register)



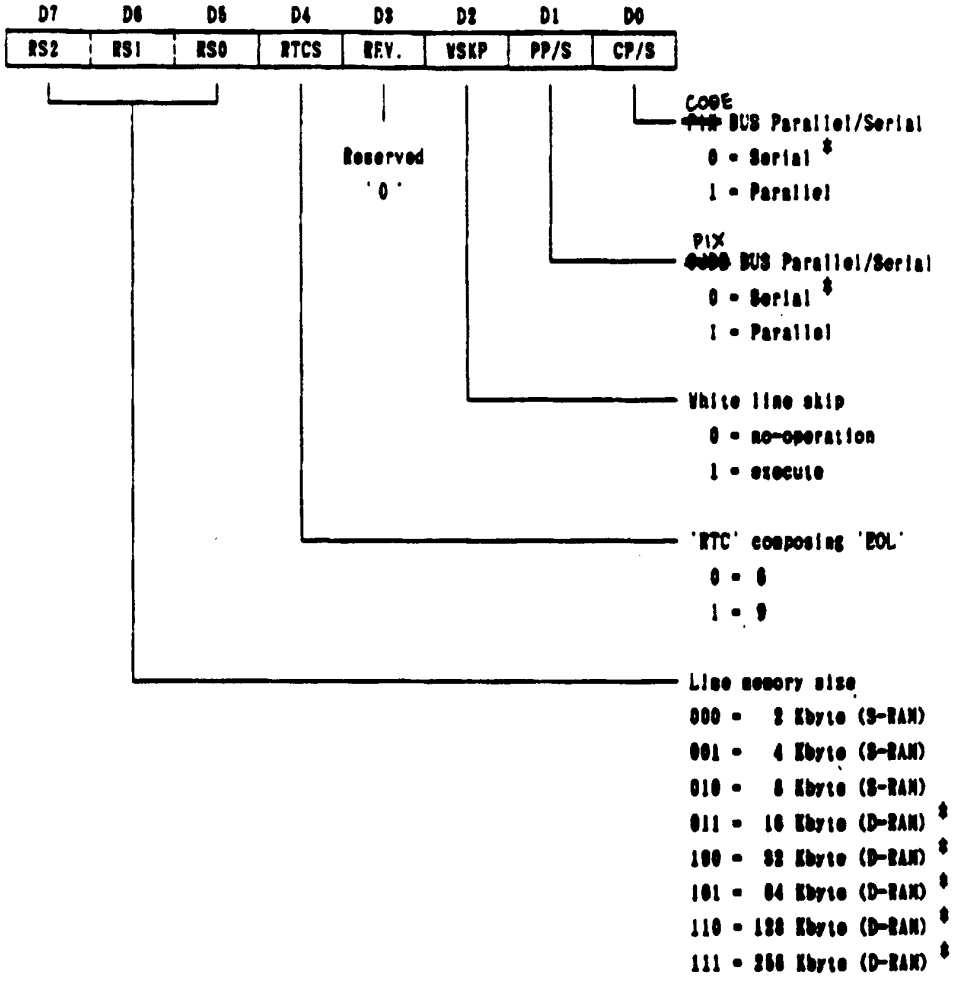
'IMR' is accessible to writing operation by setting register address (A1,A0)=(0,1).

This register controlls for interruption to the host processor. Meaning of each bit is explains following table. If each bit is set at '0', VCEC+ carries out the interruption of meaning of the bit. All the bits of this register are set at '1', the interruption is not occurred.

Bit	Name	Encoding	Decoding
D7	DERM		Error detection(unit of line)
D6	ECYM		Error counter curry (8-bit counter)
D5	RTCDM		'RTC' code detection
D4	EOLDM		'EOL' code detection
D3	PNDM	Output the last code of a page	Output the last data of a page
D2	LNDM	Generate the 'EOL' code	Output the last data of a line
D1	MLMM	Memory is Full	Line memory is empty
D0	REV.		

Note) Reserve bit of this register is always set at '1'

□ R S R (Ram Size Register)



'RSR' is accessible to writing operation by setting register address (A1,A0)=(1,0) of the first access.

Serial mode is not supported now. then bit D0 and D1 is always set at ' 1 '. And now the VCEC* can connect static-RAM only for the line memory. Then bit D7,D6,and D5 is able to set at (0,0,0), (0,0,1), or (0,1,0) only. White line skip is explains another topics. 'RTC' composing 'EOL' is selectable in bit D4.

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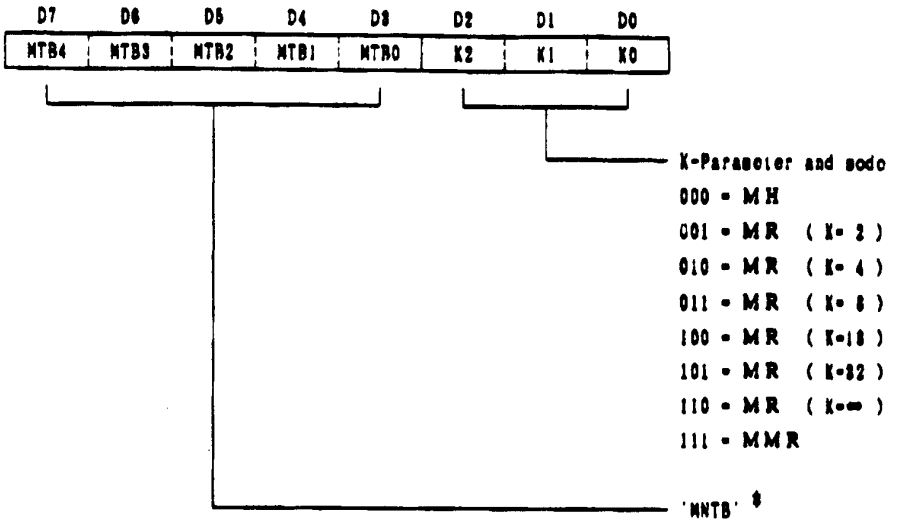
Note) Reserve bit of this register is always set at '0'

□ PR (Parameter Register)

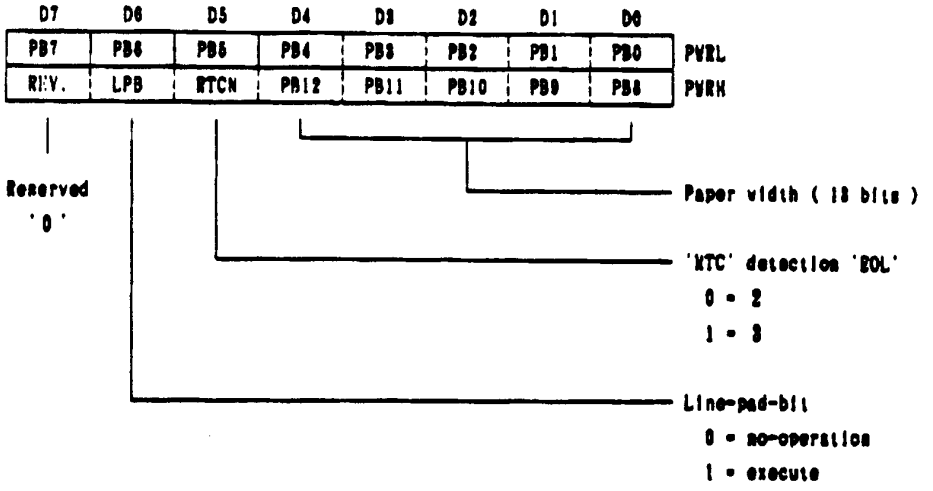


D7	D6	D5	D4	D3	MNTB	D7	D6	D5	D4	D3	MNTB	D7	D6	D5	D4	D3	MNTB
0	0	0	0	0	0	0	1	0	1	1	144	1	0	1	1	0	32
0	0	0	0	1	51	0	1	1	0	0	192	1	0	1	1	1	80
0	0	0	1	0	15	0	1	1	0	1	240	1	1	0	0	0	160
0	0	0	1	1	20	0	1	1	1	0	288	1	1	0	0	1	320
0	0	1	0	0	24	0	1	1	1	1	384	1	1	0	1	0	480
0	0	1	0	1	36	1	0	0	0	0	66	1	1	0	1	1	94
0	0	1	1	0	48	1	0	0	0	1	102	1	1	1	0	0	48
0	0	1	1	1	84	1	0	0	1	0	114	1	1	1	0	1	57
0	1	0	0	0	72	1	0	0	1	1	12	1	1	1	1	0	66
0	1	0	0	1	96	1	0	1	0	0	18	1	1	1	1	1	136
0	1	0	1	0	126	1	0	1	0	1	29						

Note) 'MNTB' means 'Minimum Number of Transmission Bit'

'PR' is accessible to writing operation by setting register address (A1.A0)=(1.0) of the second access.

□ PWRL/PWRH (Paper Width Register of Low/High)



'PWRL/H' is accessible to writing operation by setting register address (A1.A0)=(1.1)
The first access. 'PWRL' is accessed. and the second access. 'PWRH' is accessed.

Paper width (the number of pels composing one-line) is set by following processure.

Example) S e t B 4 (8 dot/mm)= 2 0 4 8 bit/line

① 2048(D) - 1(D) = 2047(D) minus 1
② 2047(D) = 7FF(H) HEX code
③ 7FF(H) = 0111 1111 1111(B) Binary code
④ 0111 1111 1111(B) = 0 0111 1111 1111(B) 13 bits of Binary code

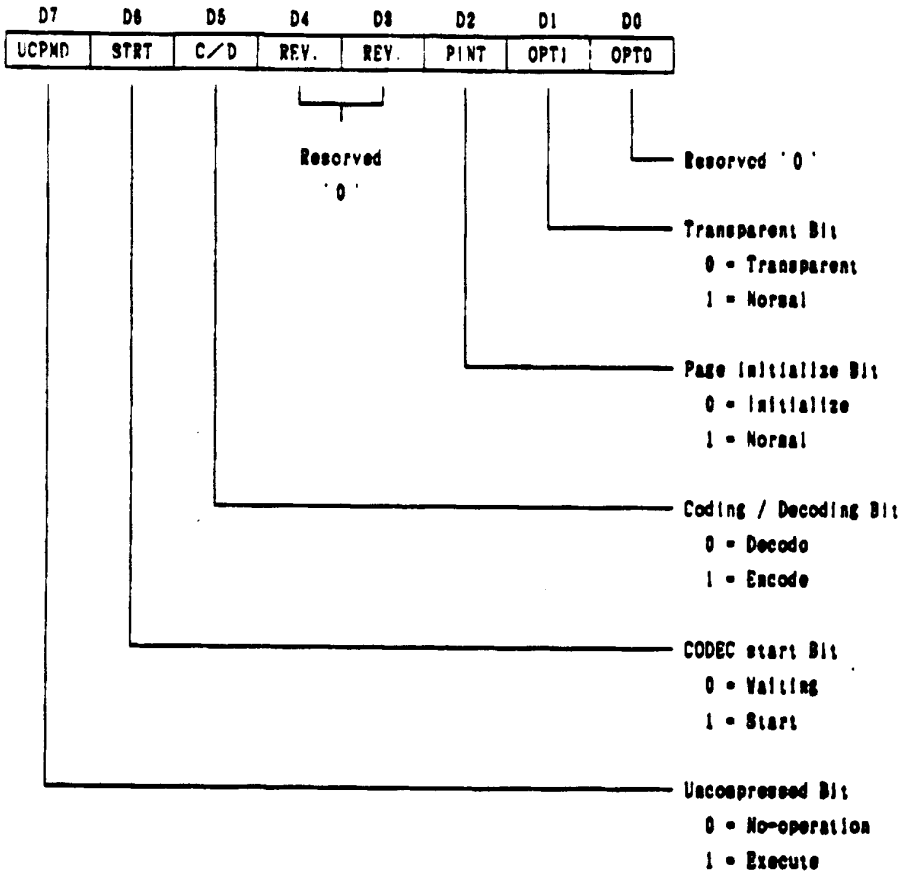
(PB12.PB11.PB10.·····.PB1.PB0)=(0.0.1.1.1.1.1.1.1.1.1.1.1)

But. If the paper width is set more than 7743 bit/line or less than 32 bit/line. the VCEC* is not processes the correct data. Then following setting is INHIBIT.

Less than (PB12.PB11.PB10.·····.PB1.PB0)=(0.0.0.0.0.0.0.0.1.1.1.1.1)
More than (PB12.PB11.PB10.·····.PB1.PB0)=(1.1.1.1.0.0.0.1.1.1.1.1.0)

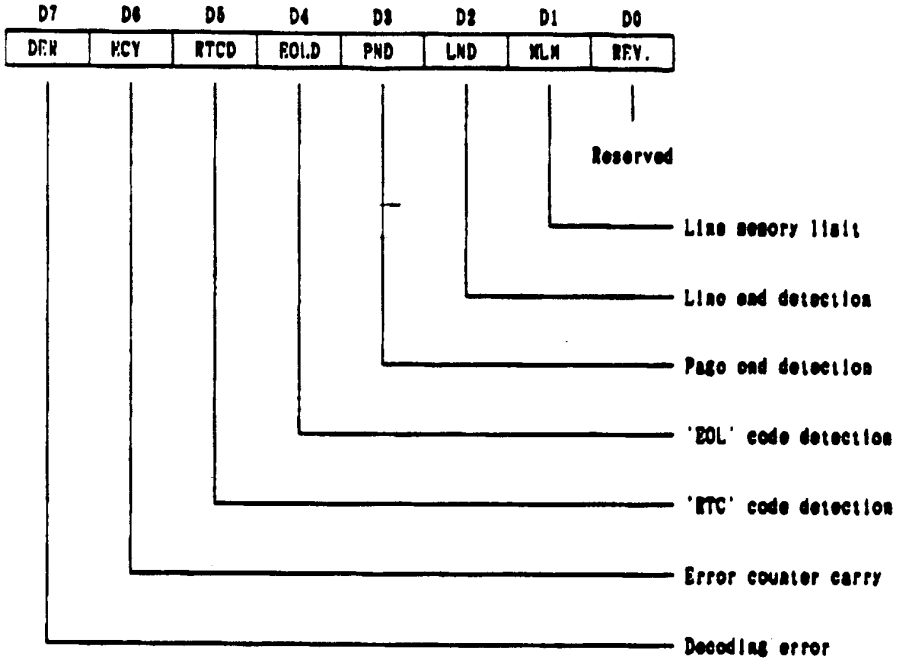
Note) Reserve bit of this register is always set at '0'

☐ SCNR (System Controll Notice Register)



'SCNR' is accessible to reading operation by setting register address (A1.A0)=(0.0).

□ I R R (Interrupt Request Register)



'IRR' is accessible to reading operation by setting register address (A1.A0)=(0.1).

Reading is this register, and the system finds the cause of the interuption. 'IRQ' signal and this register is reset, by reading this register. Meaning of each bit, see following table.

Name	Coding/Decoding	M e a n i n g
NLN	Coding	Line memory is Full
	Decoding	Line memory is empty
LND	Coding	generate 'EOL' code
	Decoding	Outputs the last data of a line
PND	Coding	Outputs the last coded-data of a page
	Decoding	Outputs the last PIX-data of a page
EOLD	Decoding	'EOL' code detection
RTCD	Decoding	'RTC' code detection
MCY	Decoding	Carry of error line counter (8-bit) This bit is active then error line counter is reset.
DER	Decoding	Decoding error detection Error line counter is increment in this time.

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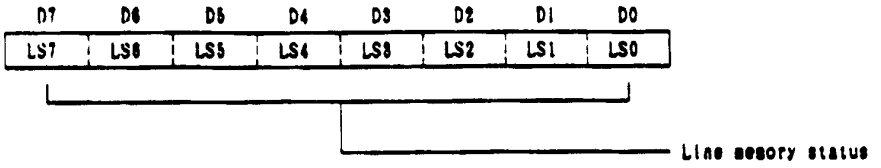
□ L S R (Line memory Status Register)



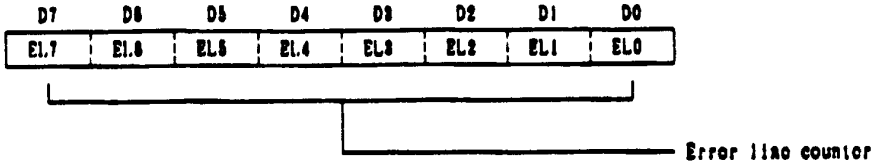
'LSR' is accessible to reading operation by setting register address (A1.A0)=(1.0).

This register shows the number of line's data stored in the line memory. If using 64kbyte RAM for line memory, this register is function as follows

Stored line	MLM [IRR(D1)]	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 line	L	0	0	0	0	0	0	0	0
1 line	L	0	0	0	0	0	0	0	1
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
2 5 4 line	L	1	1	1	1	1	1	1	0
2 5 5 line	L	1	1	1	1	1	1	1	1
2 5 6 line	L	1	1	1	1	1	1	1	1
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
3 0 2 line	H	1	1	1	1	1	1	1	1

302 line's data is able to stored in this memory. when this memory stored 302 line's data. th is register drives the 'MLM' bit of 'IRR' is active. and stops the data input.

□ E L R (Error Line count Register)



'ELR' is accessible to reading operation by setting register address (A1.A0)=(1.1).

This register counts the number of line contains error. This register drives 'IRQ' signal is active. every 256 error line is counted. This register and 'ECY' bit of 'IRR' functions as follows

Error Line	ECY [IRR(D6)]	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 line	L	0	0	0	0	0	0	0	0
1 line	L	0	0	0	0	0	0	0	1
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
254 line	L	1	1	1	1	1	1	1	0
255 line	H	1	1	1	1	1	1	1	1
256 line	L	0	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
510 line	L	1	1	1	1	1	1	1	0
511 line	H	1	1	1	1	1	1	1	1
512 line	L	0	0	0	0	0	0	0	0
513 line	L	0	0	0	0	0	0	0	1
:	:	:	:	:	:	:	:	:	:

Line memory Selection

□ Memory selection

Connects the Static-RAM as the line memory. The Memory size is decided by maximum number of pels for coding. The RAM size involved in the maximum number of pels is explains following table (next page). It should be selected that more than 3-lines of data is stored in.

If the decoding error is occurred, the VCEC+ is not increment the address of the line memory in this action, previous line's data is output instead of the error line's data. But during this action, data is transmitted continuously. The time for the recovering error line involved in the line memory access time is following table.

Access time	250 ns		500 ns		1000 ns	
paper width	Time	Bit	Time	Bit	Time	Bit
256 bit	0.016	0.15	0.016	0.15	0.016	0.15
512 bit	0.032	0.31	0.032	0.31	0.032	0.31
1024 bit	0.064	0.61	0.064	0.61	0.064	0.61
1728 bit	0.108	1.04	0.108	1.04	0.108	1.04
2048 bit	0.128	1.23	0.128	1.23	0.128	1.23
4096 bit	0.256	2.46	0.256	2.46	0.256	2.46
7743 bit	0.484	4.65	0.484	4.65	0.484	4.65

Note) Time means the time for recovering error line [unit : ms]
Bit means the total number of bit during the Time is past [unit : bit/sec]
(Transmission rate is 9600 bps)
Access time 250 ns equivalent to 16MHz master clock input

$$T = \frac{x}{8} \times y \times 2 + a \quad (ns)$$

$$D = T \times Z \quad (bit)$$

T : Time for recovering error line
x : Total number of bit composing paper width
y : Memory access time
a : Dynamicras refresh time (not supported)
D : total number of bit during Time is past
Z : Data transmission rate

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Line memory selection Table

[Unit : Pels/Line]

RAM Size / Paper Size (Byte)	Maximum storage line size							
	2K	4K	8K	16K	32K	64K	128K	256K
24 - 256	63	127	255	511	1023	2046	2046	2046
257 - 512	31	63	127	255	511	1023	2046	2046
513 - 768	20	41	84	169	340	681	1364	2046
769 - 1024	15	31	63	127	255	511	1023	2046
1025 - 1280	11	24	50	101	203	408	818	1637
1281 - 1536	9	20	41	84	169	340	681	1364
1537 - 1792	8	17	35	72	145	291	584	1169
1793 - 2048	7	15	30	63	127	255	511	1023
2049 - 2304	6	13	27	55	112	226	454	909
2305 - 2560	5	11	24	50	101	203	408	818
2561 - 2816	4	10	22	45	92	185	371	743
2817 - 3072	4	9	19	41	84	169	340	681
3073 - 3328	3	8	18	38	77	156	314	629
3329 - 3584	3	8	17	35	72	145	291	584
3585 - 3840	3	7	16	33	67	135	273	545
3841 - 4096	3	7	15	31	63	127	255	511
4097 - 4352	×	6	14	29	58	118	239	480
4353 - 4608	×	6	13	27	55	112	226	454
4609 - 4864	×	5	12	25	52	106	214	430
4865 - 5120	×	5	11	24	50	101	203	406
5121 - 5376	×	5	11	23	47	96	194	389
5377 - 5632	×	4	10	22	45	92	185	371
5633 - 5888	×	4	10	21	43	88	177	355
5889 - 6144	×	4	9	20	41	84	169	340
6145 - 6400	×	4	9	19	39	80	162	326
6401 - 6656	×	3	8	18	36	77	156	314
6657 - 6912	×	3	8	17	36	74	150	302
6913 - 7168	×	3	8	17	35	72	145	291
7169 - 7424	×	3	7	16	34	69	140	281
7425 - 7680	×	3	7	16	33	67	135	272
7681 - 7748	×	3	7	16	32	65	131	263
RAM Type	S-RAM			D-RAM				

Note) Dynamic RAM is not supported now. Can connect Static-RAM only.
× mark : not for use as the line memory

Recommendable RAM TC5565APL-10/-12/-15 (8k x 8bit)

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Initialization and Termination process

□ Initialization

The MPU should be done following initialization, before VCEC* starts the processing.
Exaspic for initialization explains after follows :

Conditions

- Paper width A4 (1728 bit/line)
- Interrupt Mask Register no-mask
- Line memory size 2K byte
- Line-pad-bit no operation
- 'RTC' composing 'EOL' 6
- 'RTC' detective 'EOL' 2
- Coding mode Modified Huffman
- Coding or Decoding Encoding

No.	Means	Register	Exaspic for setting	
			D7 ~ D0	HEX code
①	Set initializing mode	SCSR	(0.0.1.0.0.0.1.1)	2 3
②	Interrupt Mask Register setting	IMR	(0.0.0.0.0.0.0.0)	0 0
③	RAM size Register setting	RSR	(0.0.0.0.0.0.1.1)	0 3
④	Parasctor Register setting	PR	(0.0.0.0.0.0.0.0)	0 0
⑤	Paper width Register of Low setting	PWRL	(1.0.1.1.1.1.1.1)	B F
⑥	Paper width Register of High setting	PWRH	(0.0.0.0.0.1.1.0)	0 6
⑦	Set waiting mode	SCSR	(0.0.1.0.0.1.1.1)	2 7
⑧	CODEC start	SCSR	(0.1.1.0.0.1.1.1)	6 7

□ Termination 1 (Encoding mode Termination)

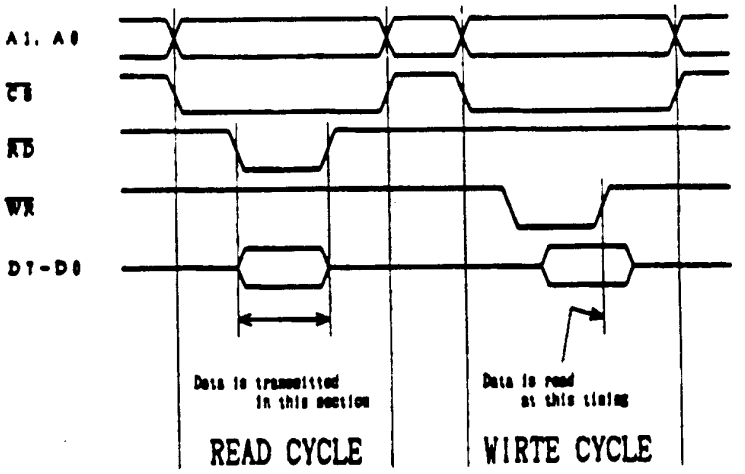
No.	Means	Register	Exaspic for setting	
			D7 ~ D0	HEX code
①	Input last data of a page			
②	Set waiting mode	SCSR	(0.0.1.0.0.1.1.1)	2 7
③	Detection of 'PND' bit of 'IRR'			
④	Set initializing mode	SCSR	(0.0.1.0.0.0.1.1)	2 3

□ Termination ① (Decoding mode Termination).

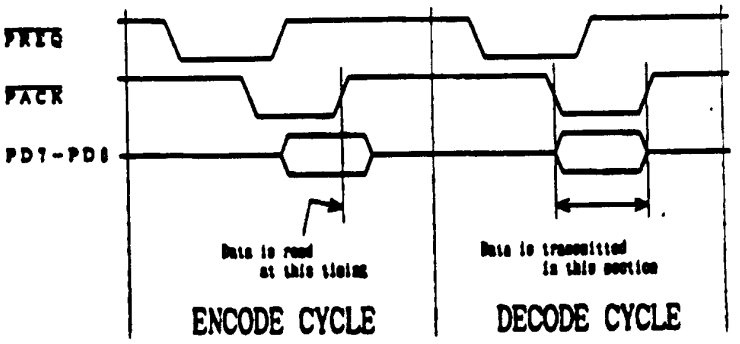
No.	Means	Register	Example for setting	
			D7 ~ D0	HEX code
①	Detects 'RTC' code			
②	Detects the 'PND' bit of 'IRR'			
③	Set waiting mode	SCSR	(0.0.0.0.0.1.1.1)	0 7
④	Set initializing mode	SCSR	(0.0.0.0.0.0.1.1)	0 3

If any changes are needed for initial setting before CEDEC re-start, initialization is should be done at the biginning.

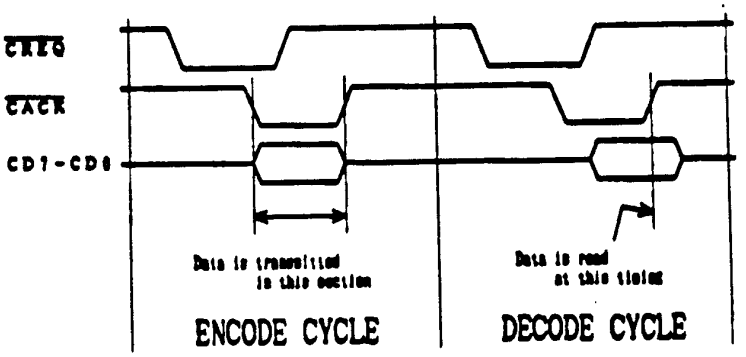
BUS INTERFACE



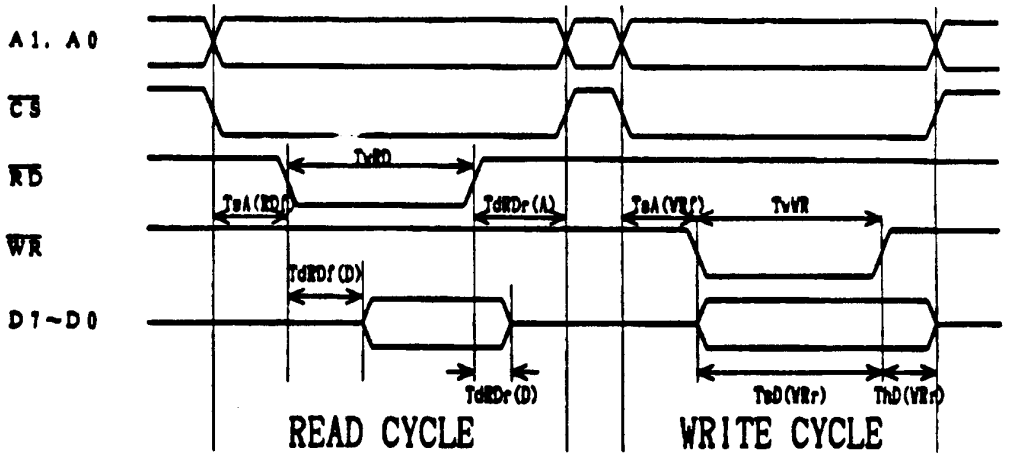
Interface 1 [MPU BUS]



Interface 2 [PIX BUS]



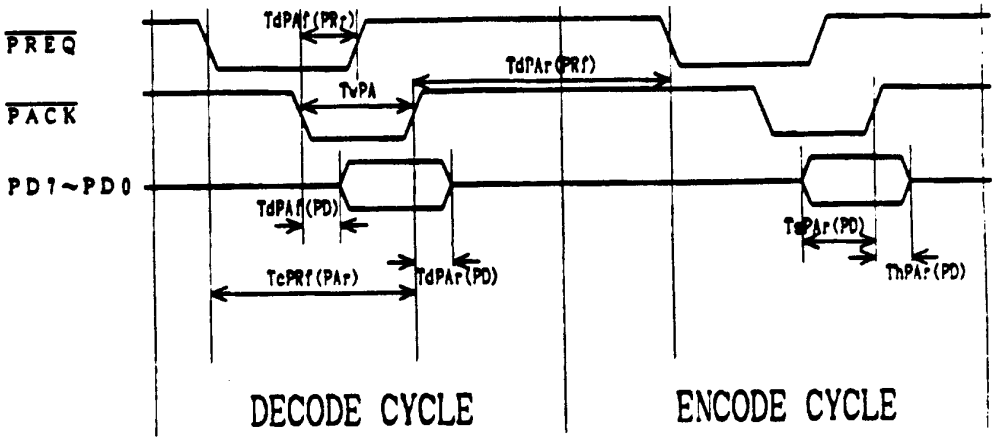
Interface 3 [CODE BUS]



MPU Bus AC Timing

UNIT : nS

Item	Meas	ng	Minimum	Typical	Maximum
TsA (RDf)	Address Set-up Time ti	'RD'='L'	70		
TdRDf (D)	'RD'='L' to Data Valid			75	
TdRDr (A)	Address Recovery Time from 'RD'='H'		30		
TdRDr (D)	'RD'='H' to Output Data='High-Z'		0		
TwRD	'RD' Signal Input Pulse Width		150		
TsA (WRf)	Address Set-up Time to 'WR'='L'		70		
TsD (WRr)	Data set-up Time for 'WR'='H'		140		
ThD (WRr)	Data Hold Time for 'WR'='H'		30		
TwWR	'WR' Signal Input Pulse Width		150		

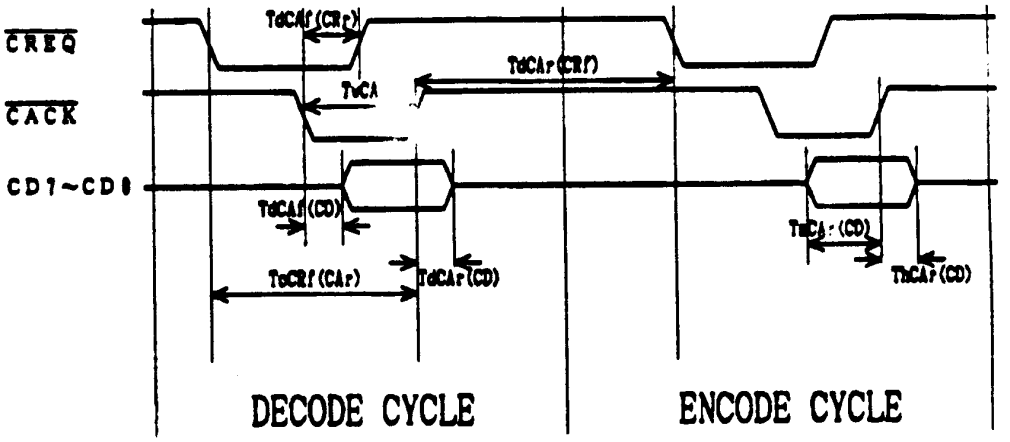


PIX Bus AC Timing

UNIT : nS

Item	Meaning	Minimum	Typical	Maximum
TcPRf (PAr)	'$\overline{PREQ}$'='L' to '$\overline{PACK}$'='H'	2T*		
TdPAf (PRr)	'$\overline{PACK}$'='L' to '$\overline{PREQ}$'='H'			60
TdPAf (PD)	'$\overline{PACK}$'='L' to Output Data Valid			80
TdPAr (PD)	'$\overline{PACK}$'='H' to Output Data='High-Z'	0		
TdPAr (PRf)	'$\overline{PACK}$'='H' to '$\overline{PREQ}$'='L'	20		
TsPAr (PD)	Data Set-up Time for '$\overline{PACK}$'='H'	60		
ThPAr (PD)	Data Hold Time for '$\overline{PACK}$'='H'	20		
TwPA	'$\overline{PACK}$' Input Pulse Width	120		

注) * : 'T' denotes one cycle time of VCEC input clock.

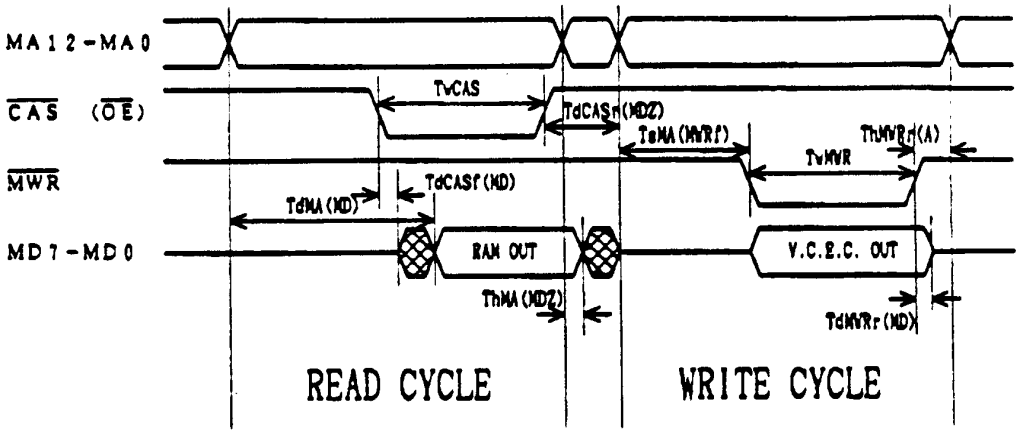


Code Bus AC Timing

UNIT : nS

Item	Meaning	Minimum	Typical	Maximum
TsCRf (CAr)	'CREQ'='L' to 'CACK'='H'	2T*		
TdCAf (CRr)	'CACK'='L' to 'CREQ'='H'			60
TdCAf (CD)	'CACK'='L' to Output Data Valid			80
TdCAr (CD)	'CACK'='H' to Output Data='High-Z'	0		
TdCAr (CRf)	'CACK'='H' to 'CREQ'='L'	20		
TsCAr (CD)	Data Set-up Time for 'CACK'='H'	60		
ThCAr (CD)	Data Hold Time for 'CACK'='H'	20		
TwCA	'CACK' Input Pulse Width	120		

注) * : 'T' denotes one cycle time of VCXC input clock.



Line Memory AC Timing

UNIT : nS

Item	Meaning	Minimum	Typical	Maximum
TdMA (MD)	Memory Address Valid to Data Valid			3T-30*
TdCASf (MD)	'$\overline{CAS}$'='L' to Data='Low-Z'			T*
ThMA (MDZ)	Data Hold Time after Address Change	0		
TdCASr (MDZ)	'$\overline{CAS}$'='H' to Data='High-Z'	30		T*
TwCAS	'$\overline{CAS}$' Signal Input Pulse Width		2T*	
TsMA (MWRf)	Address Set-up Time Prior to '$\overline{MWR}$'='L'	10		
TdMWRr (MD)	'$\overline{MWR}$'='H' to Data='High-Z'	T*		
ThMWRr (A)	Address Recovery Time for '$\overline{MWR}$'='H'	T*		
TwMWR	'$\overline{MWR}$' Signal Input Pulse Width		2T*	

注) * : 'T' denotes one cycle time of VCEC input clock.

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ELECTRICAL CHARACTERISTICS

Supply Voltage : 4.75 ~ 5.25 V Operating Temperature : 0 ~ 70 ℃

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input High Voltage	VIH	VDD = 5.25V	2.4			V
Input Low Voltage	VIL	VDD = 4.75V			0.8	V
Input Current(High)	IIH	VIN = 5.25V			±10	μA
Input Current(Low)	IIL	VIN = 5.25V			±10	μA
High-Level Output Voltage	VOH1	VDD = 4.75V / IOH = -1.5mA				
	VOH2	VDD = 4.75V / IOH = -1.0mA	4.0			V
Low-Level Output Voltage	VOL1	VDD = 4.75V / IOL = 3.0mA				
	VOL2	VDD = 4.75V / IOL = 2.0mA			0.4	V
Output High Current	IOH1	VDD = 4.75V / VOH = 4.35V	-1.5			
	IOH2	VDD = 4.75V / VOH = 4.35V	-1.0			mA
Output Low Current	IOL1	VDD = 4.75V / VOL = 0.40V	3.0			
	IOL2	VDD = 4.75V / VOL = 0.40V	2.0			mA
Standby Current	IQD	VDD = 5.25V			1	mA
Operating Supply Current	IDD	VDD = 5.25V / fcp = 8MHz		50	100	mA
		VDD = 5.25V / fcp = 16MHz		70	120	
		VDD = 5.25V / fcp = 24MHz		100	150	
		VDD = 5.25V / fcp = 32MHz		150	200	
Maximum Clock Frequency	fcp	Duty 40-60 % / Dynamic RAM	8		8/16/	
		Duty 40-60 % / Static RAM			24/32	MHz

NOTE) VOH1.VOL1.IOH1.IOL1 : D7~0, PD7~0, CD7~0, MD7~0 TERMINALS
VOH2.VOL2.IOH2.IOL2 : OTHERS

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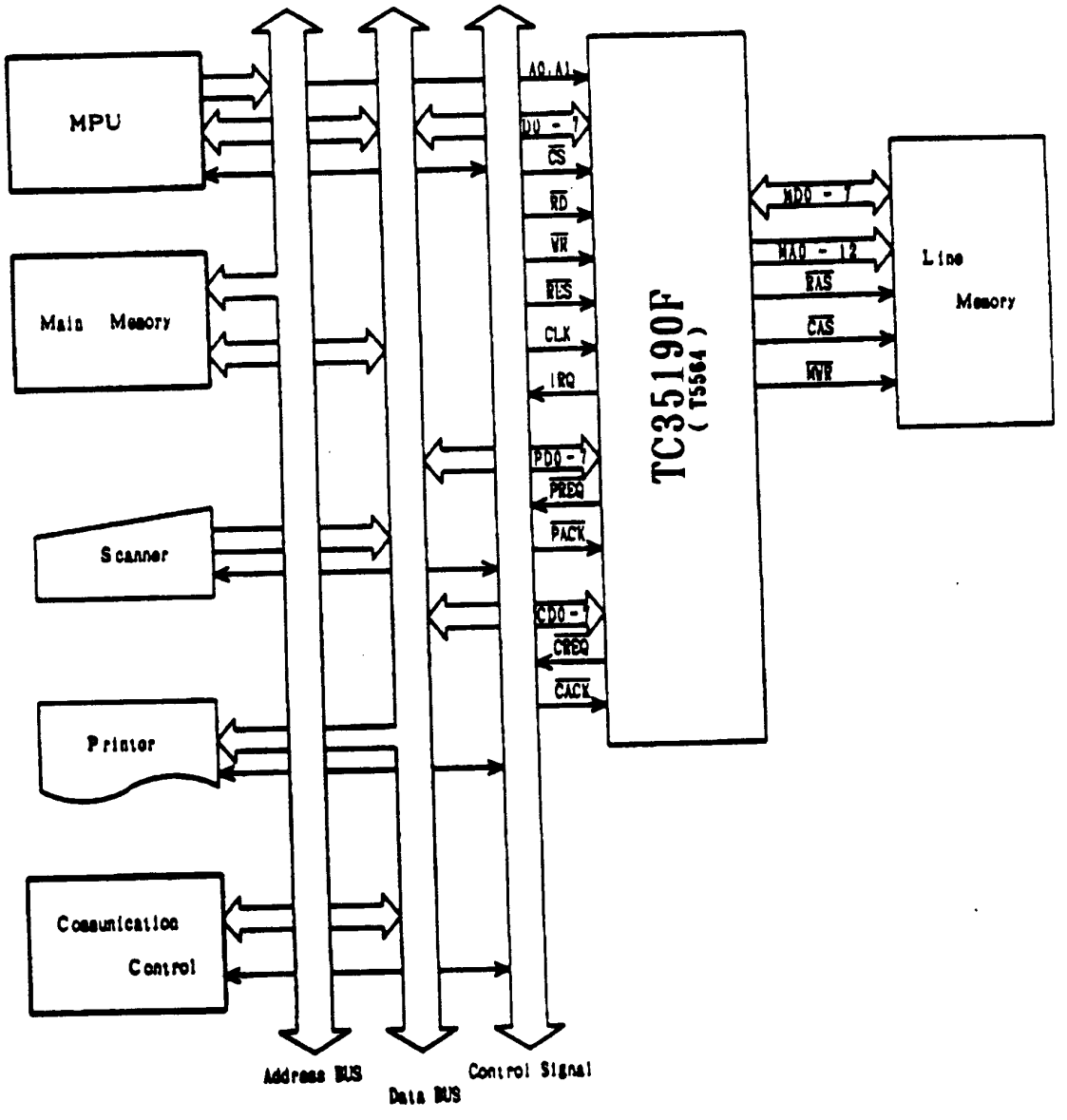
Example of Application



BUS Combined Type (For Small-Size Facsimile)

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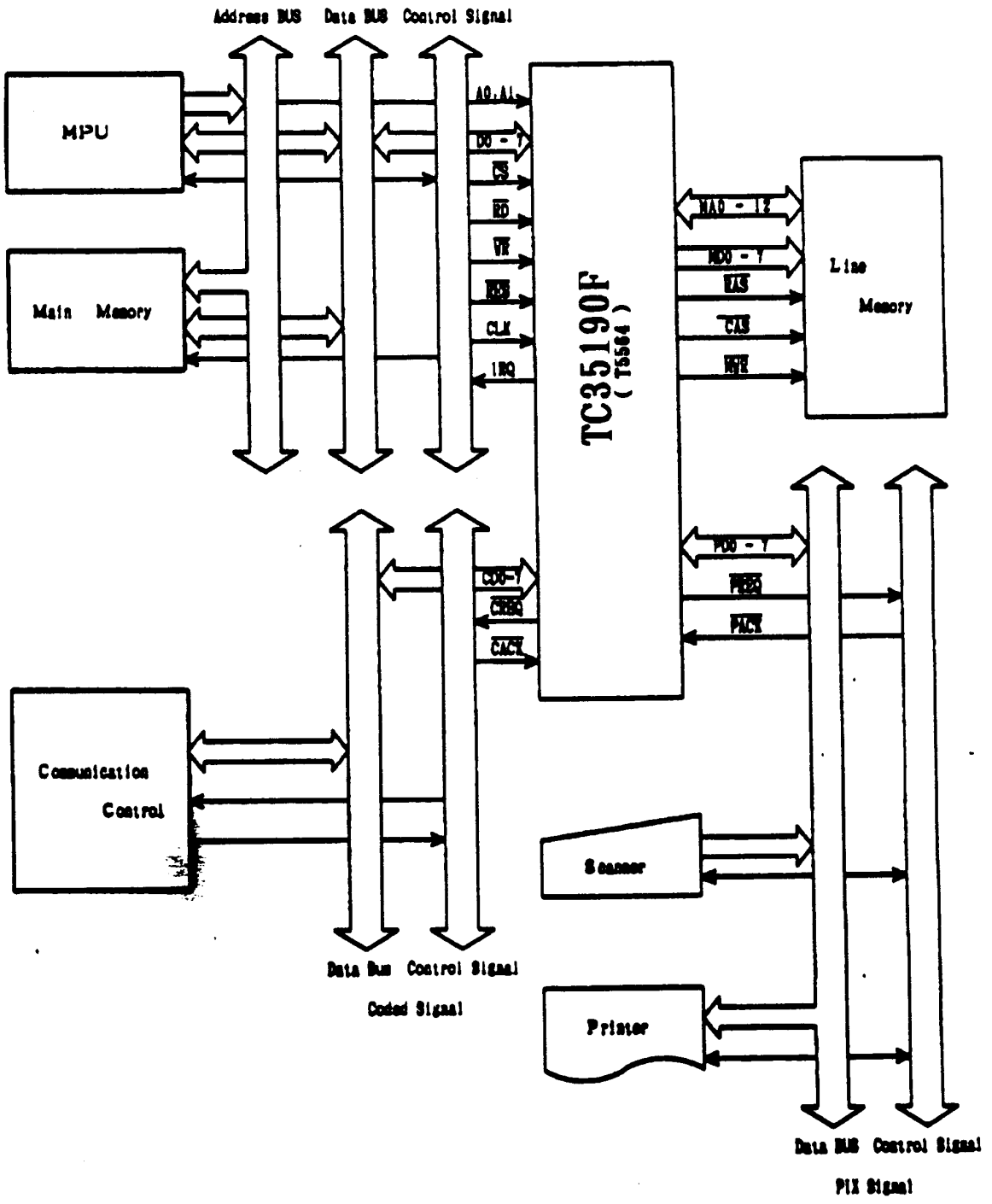

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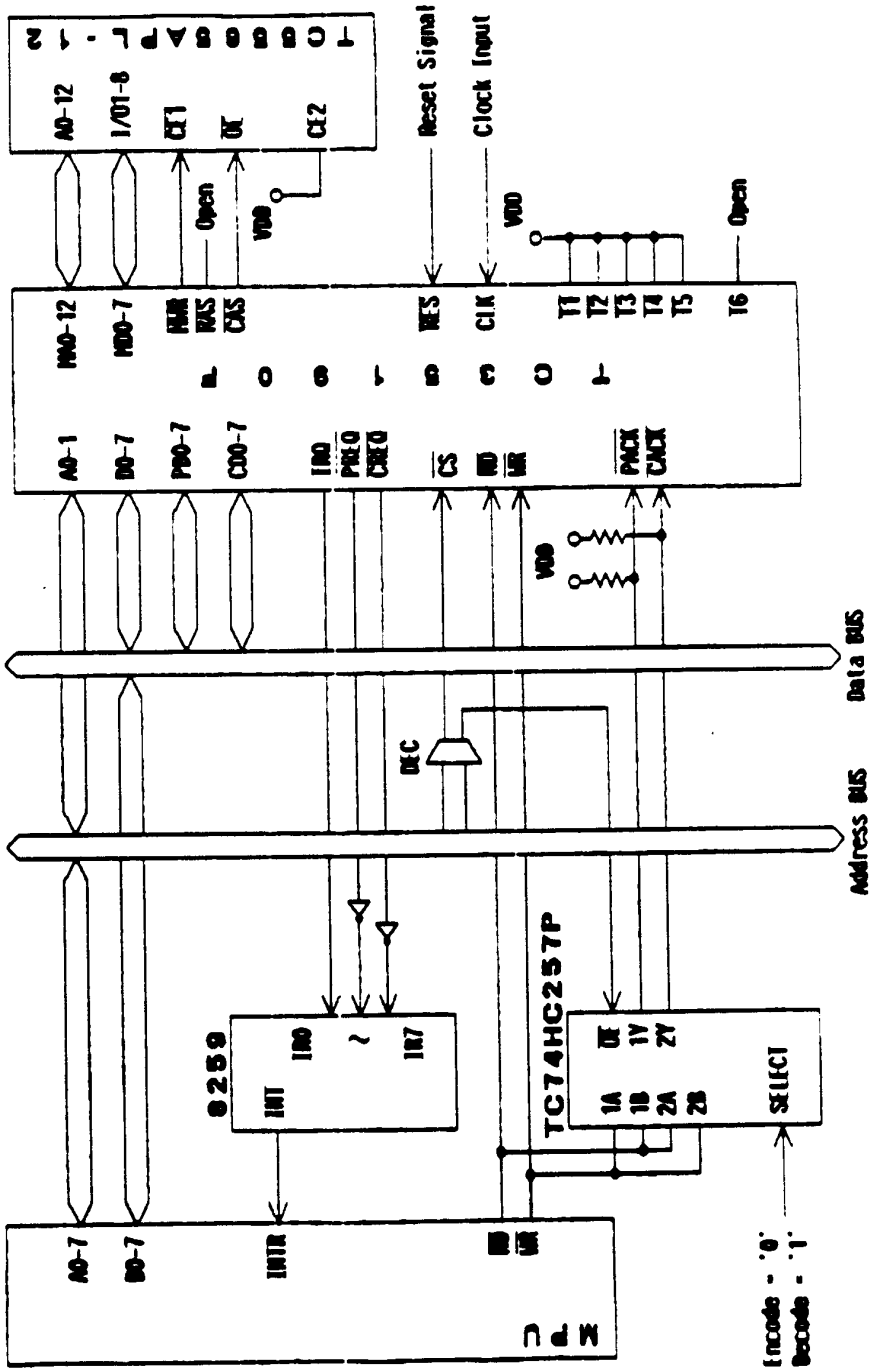
BUS Separate Type (For High-Speed Facsimile)



7. 8. 8 Page-End (Re-Start) [Decoding]

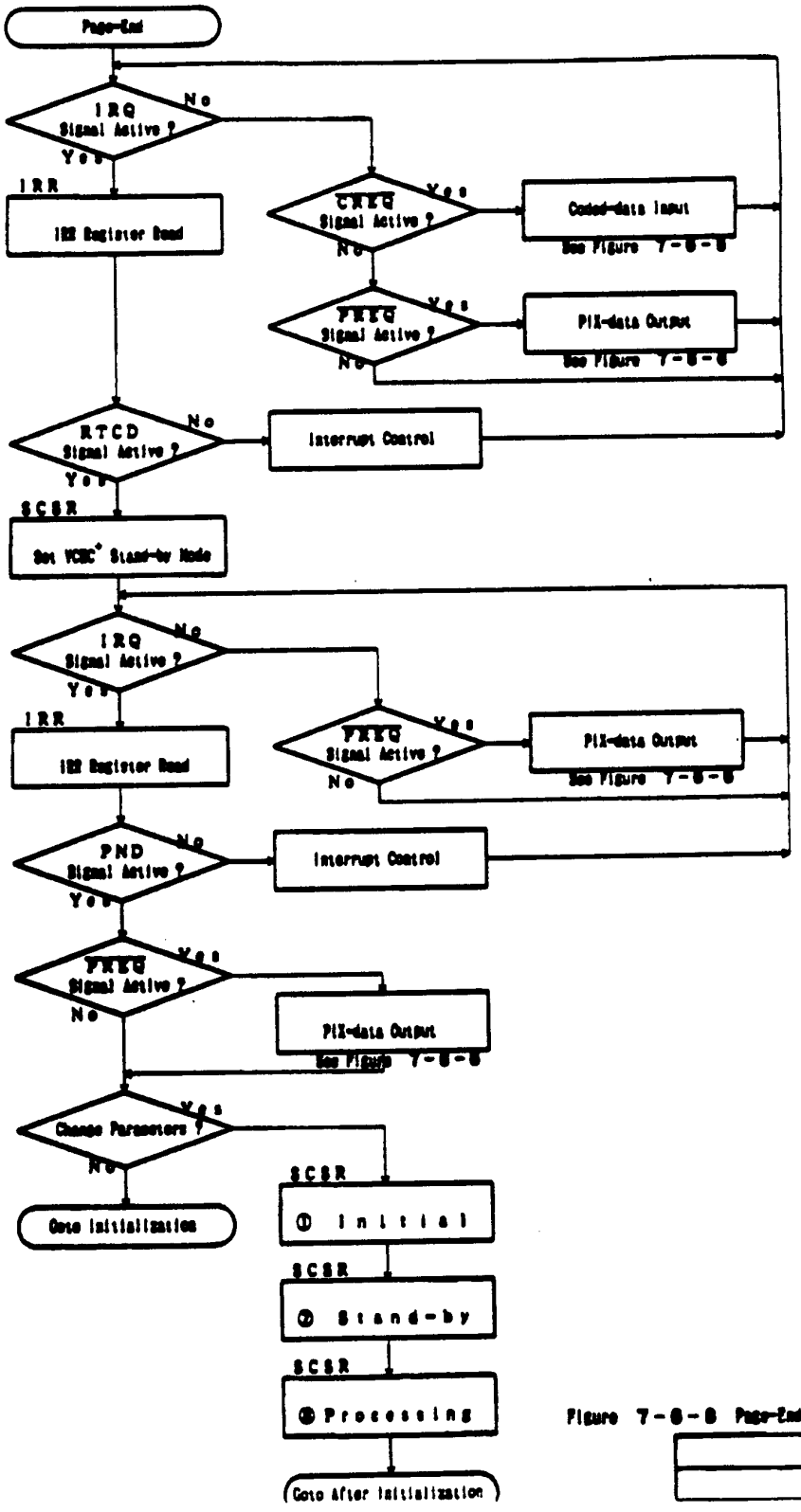


Figure 7-8-8 Page-End (Re-Start) FLOW

7. 8. 7 Page-End [Decoding]

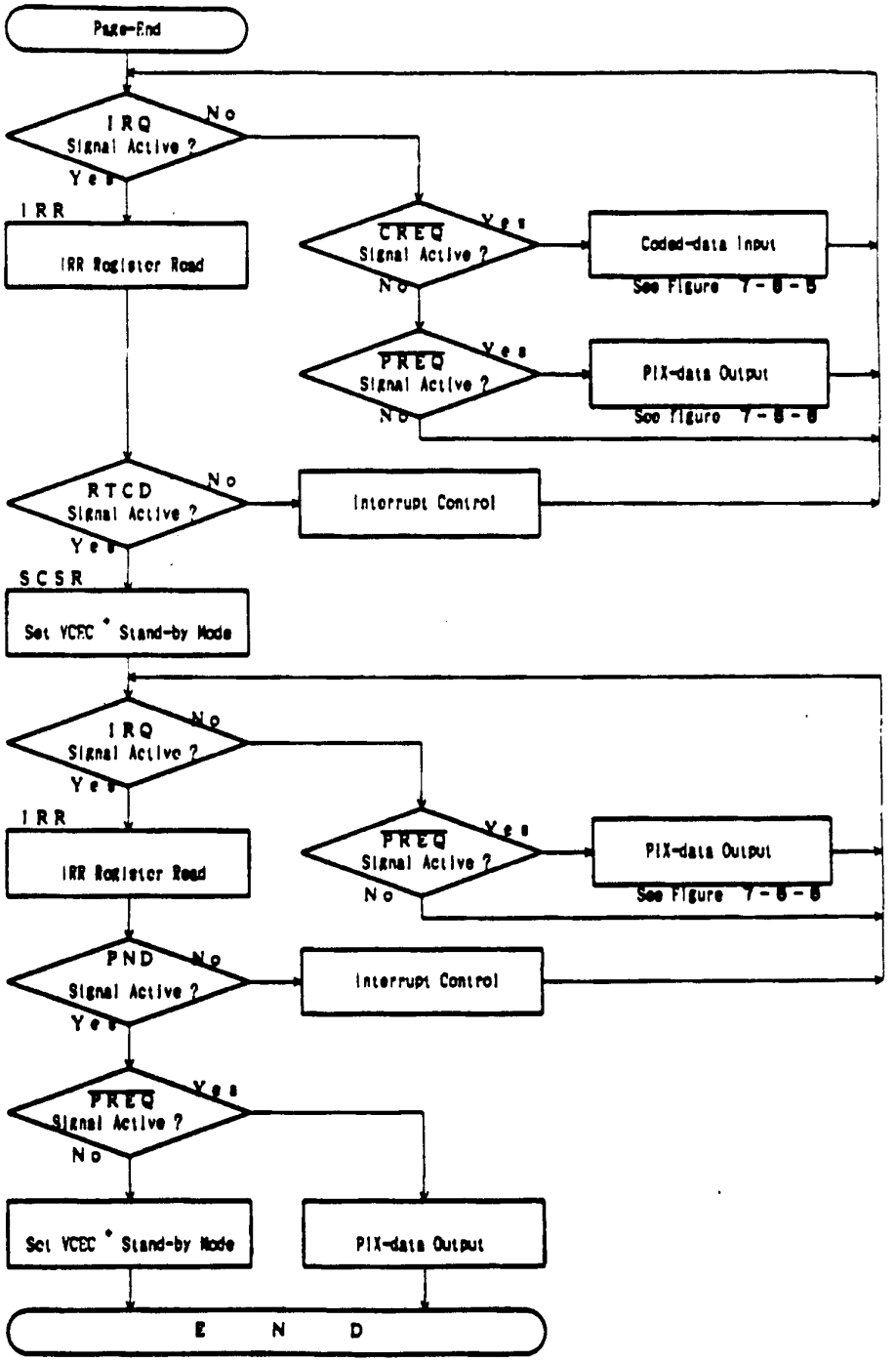


図7-8-7 Page-End FLOW [Decoding]

7. 6. 5 Coded-data Input [Decoding]

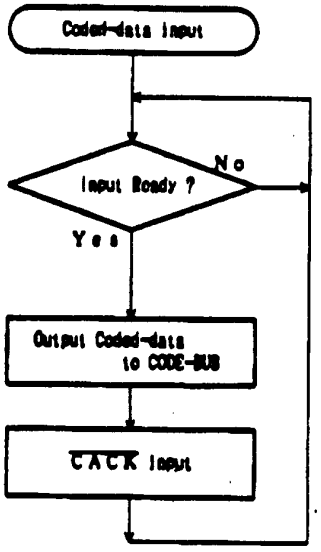


Figure 7 - 6 - 5 Coded-data Input FLOW

7. 6. 6 PIX-data output [Decoding]

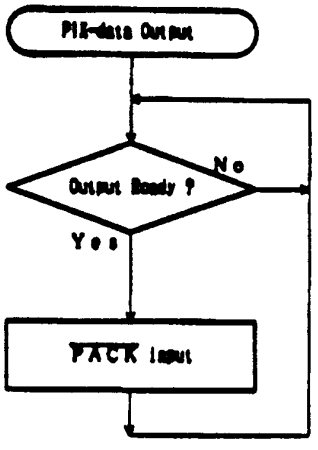


Figure 7 - 6 - 6 PIX-data output FLOW

7. 6. 4 Interrupt Item Reading [Decoding]

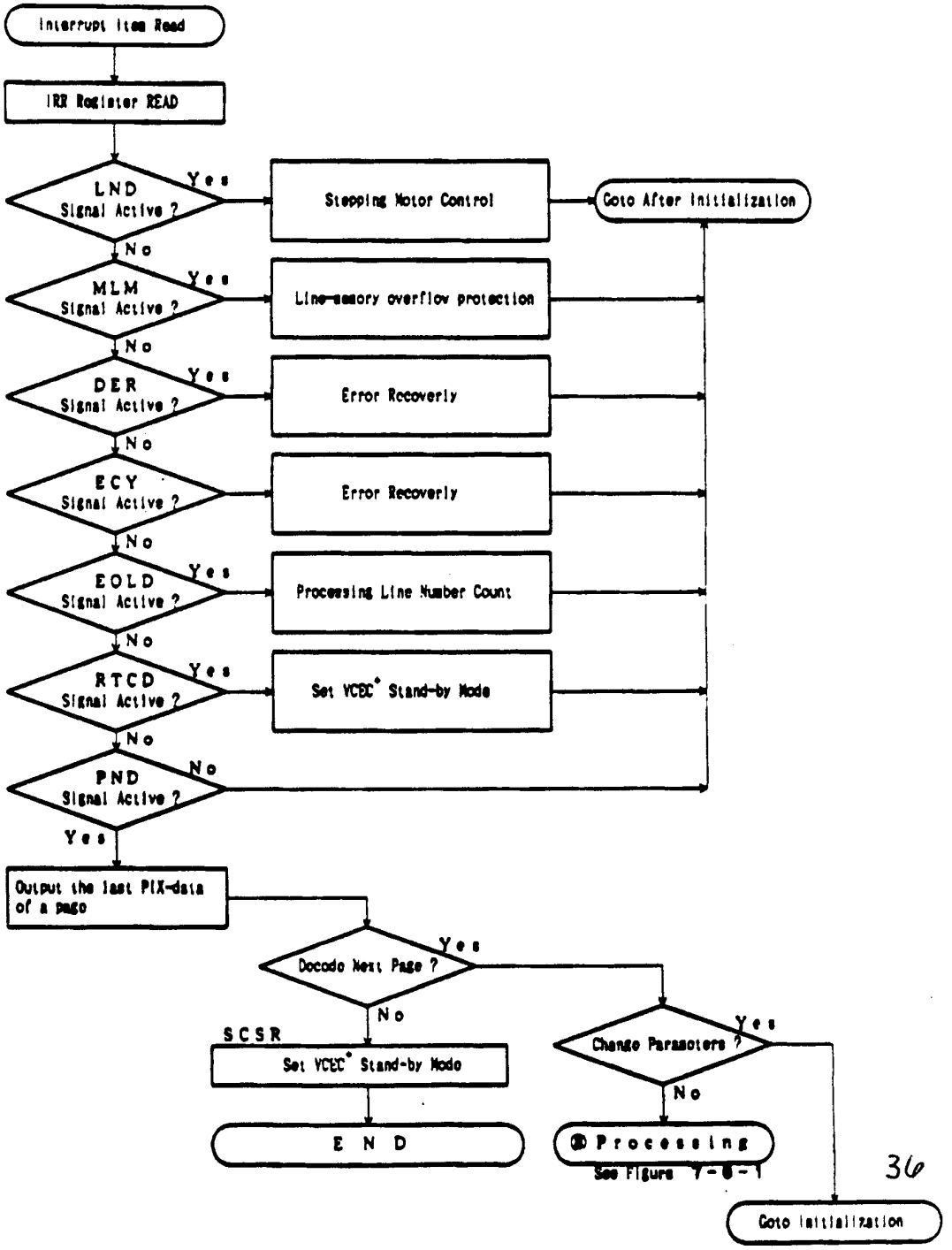


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図7-6-4 Interrupt Item Read FOW

7. 6. 3 After Initialization (II) [Decoding]

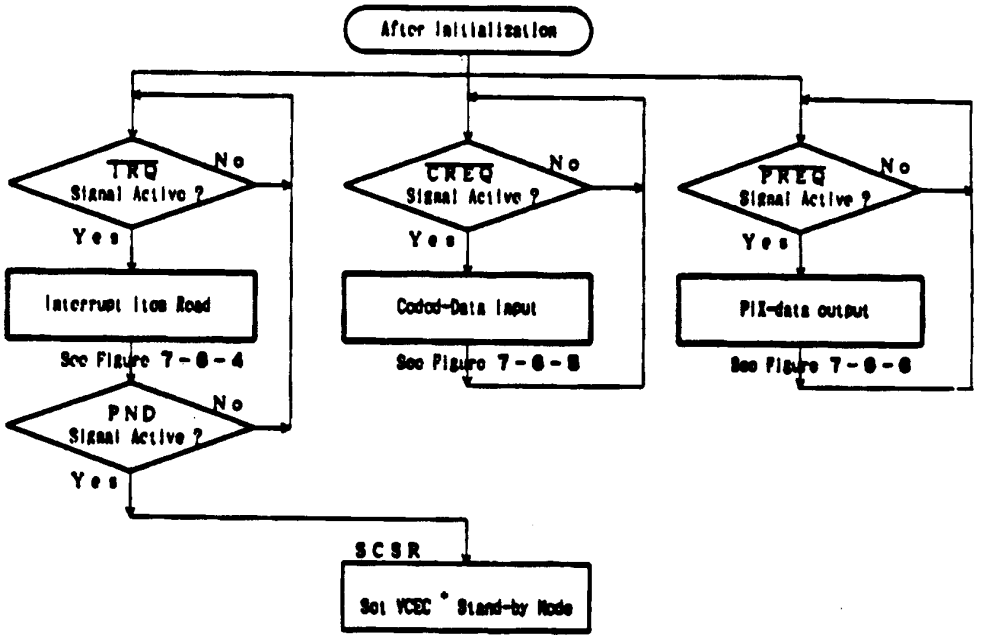


Figure 7-6-3 MAR Separate Type (For High Speed Facsimile) Decoding FLOW

7. 6. 2 After Initialization (I) [Decoding]

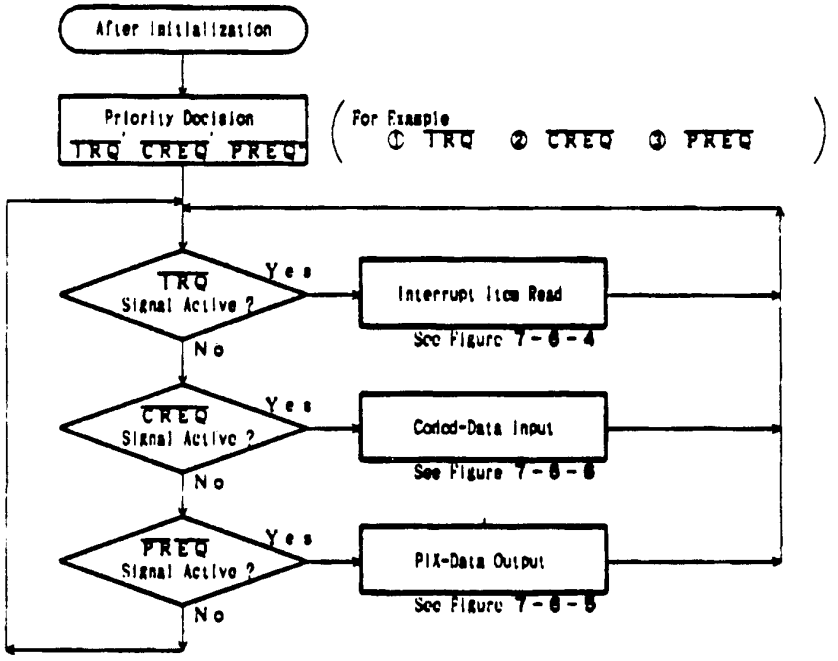


Figure 7-6-2 BUS Combined Type (For Small Size Facsimile) Decoding FLOW

7. 8. 1 Initialization

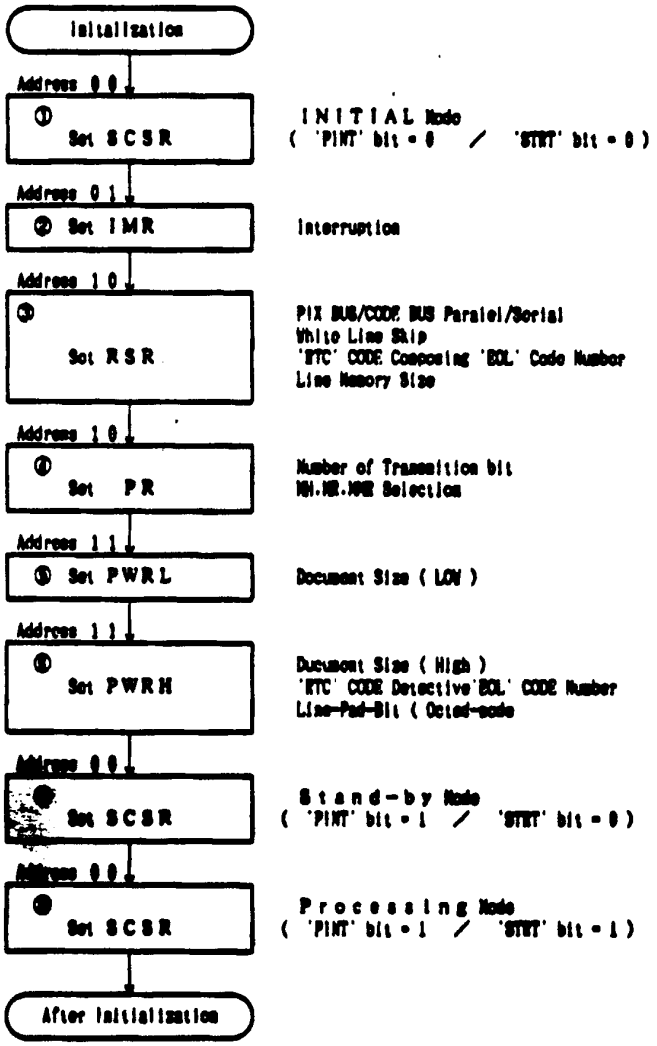


Figure 7 - 8 - 1 Initialization FLOW

7. 5. 8 Page-End (Re-Start) [Encoding]

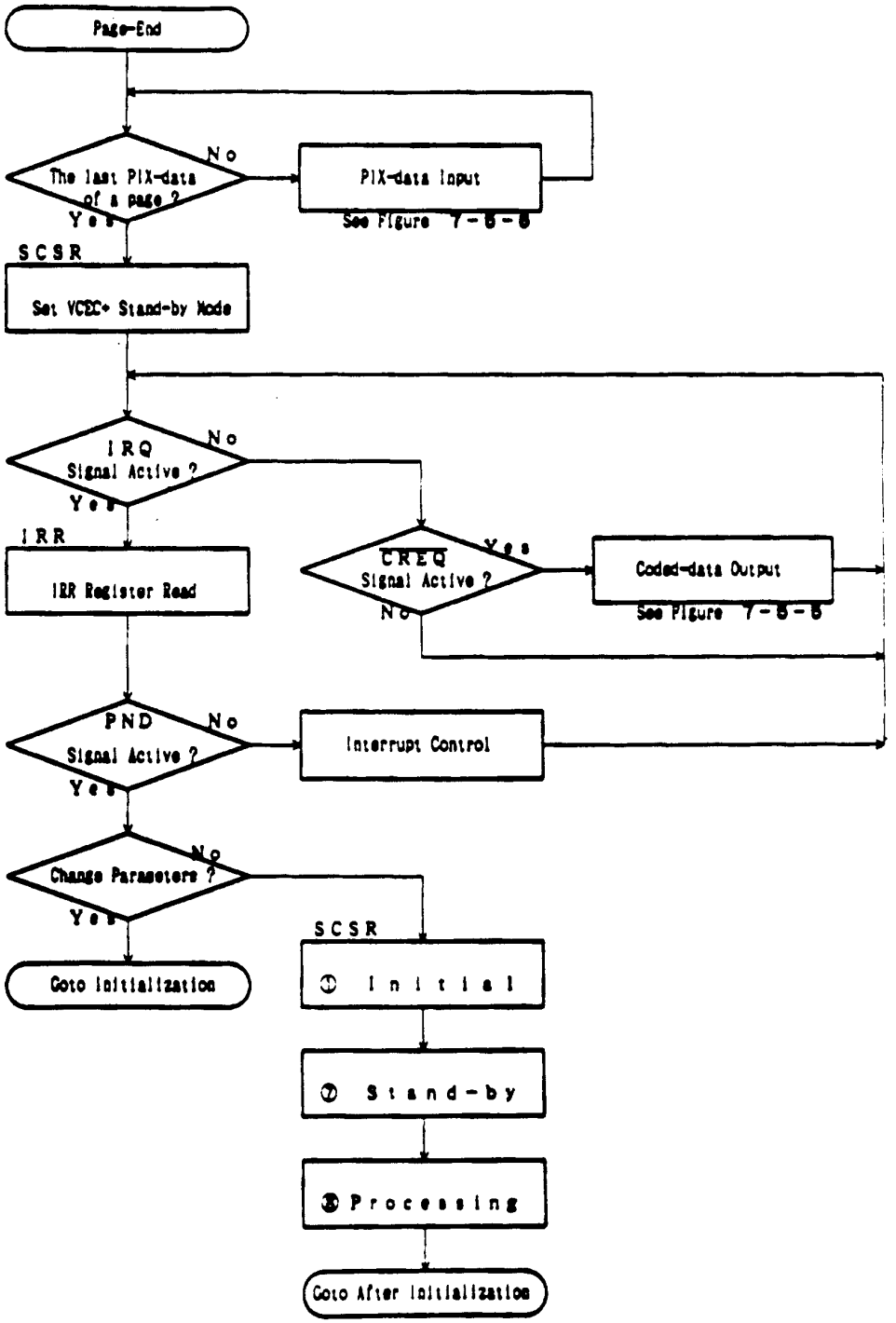


Figure 7-5-8 Page-End (Re-Start)FLOW

7. 5. 7 Page-End [Encoding]

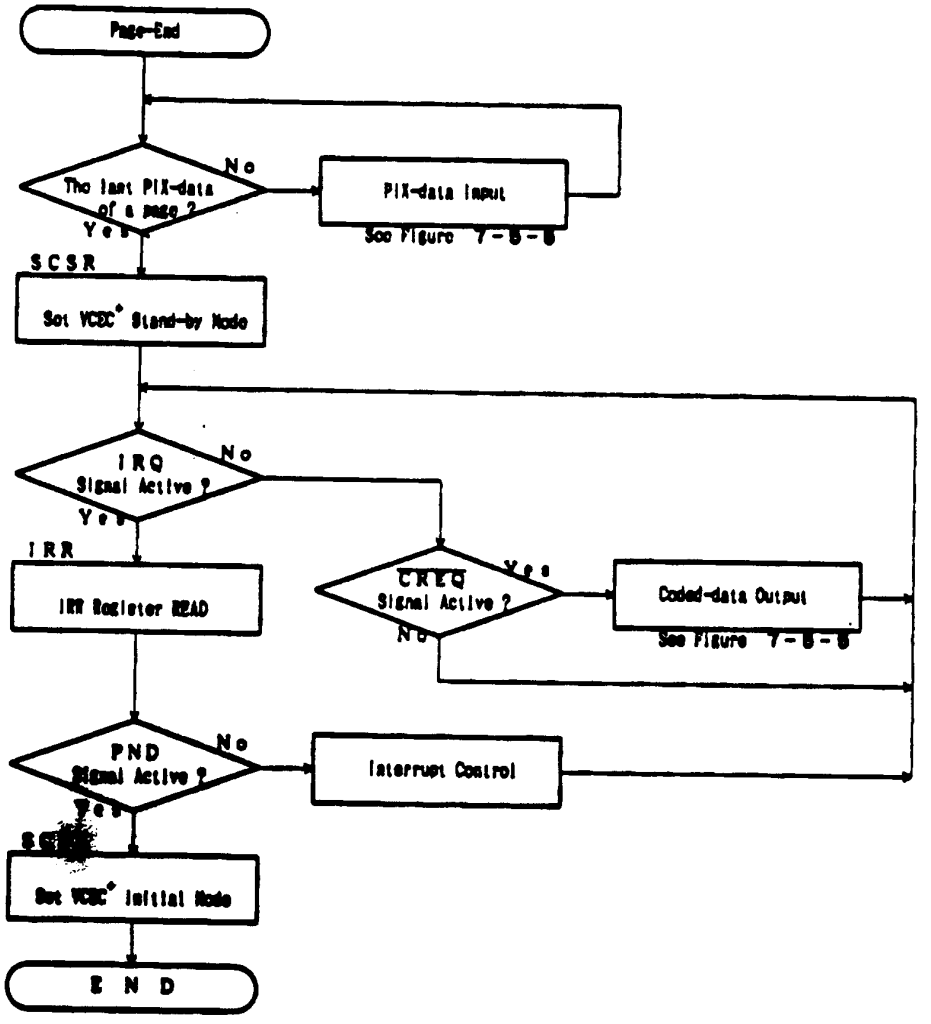


Figure 7-5-7 Page-End FLOW [Encoding]

7. 5. 5 Coded-data output [Encoding]

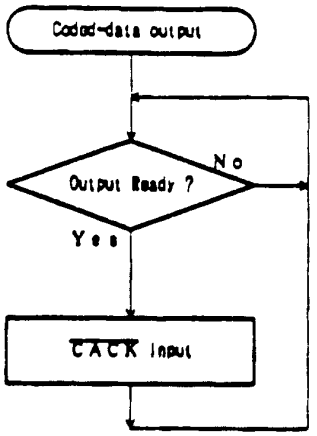


Figure 7 - 5 - 5 Coded-data output FLOW

7. 5. 6 PIX-data input [Encoding]

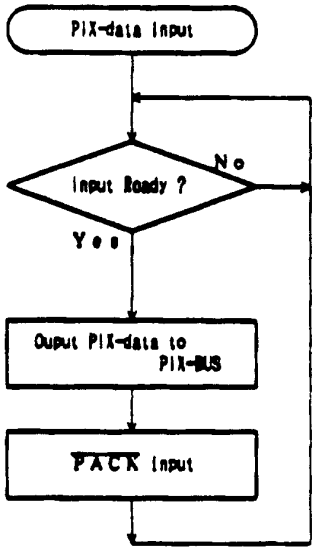


Figure 7 - 5 - 6 PIX-data input FLOW

7. 8. 4 Interrupt Item Reading [Encoding]

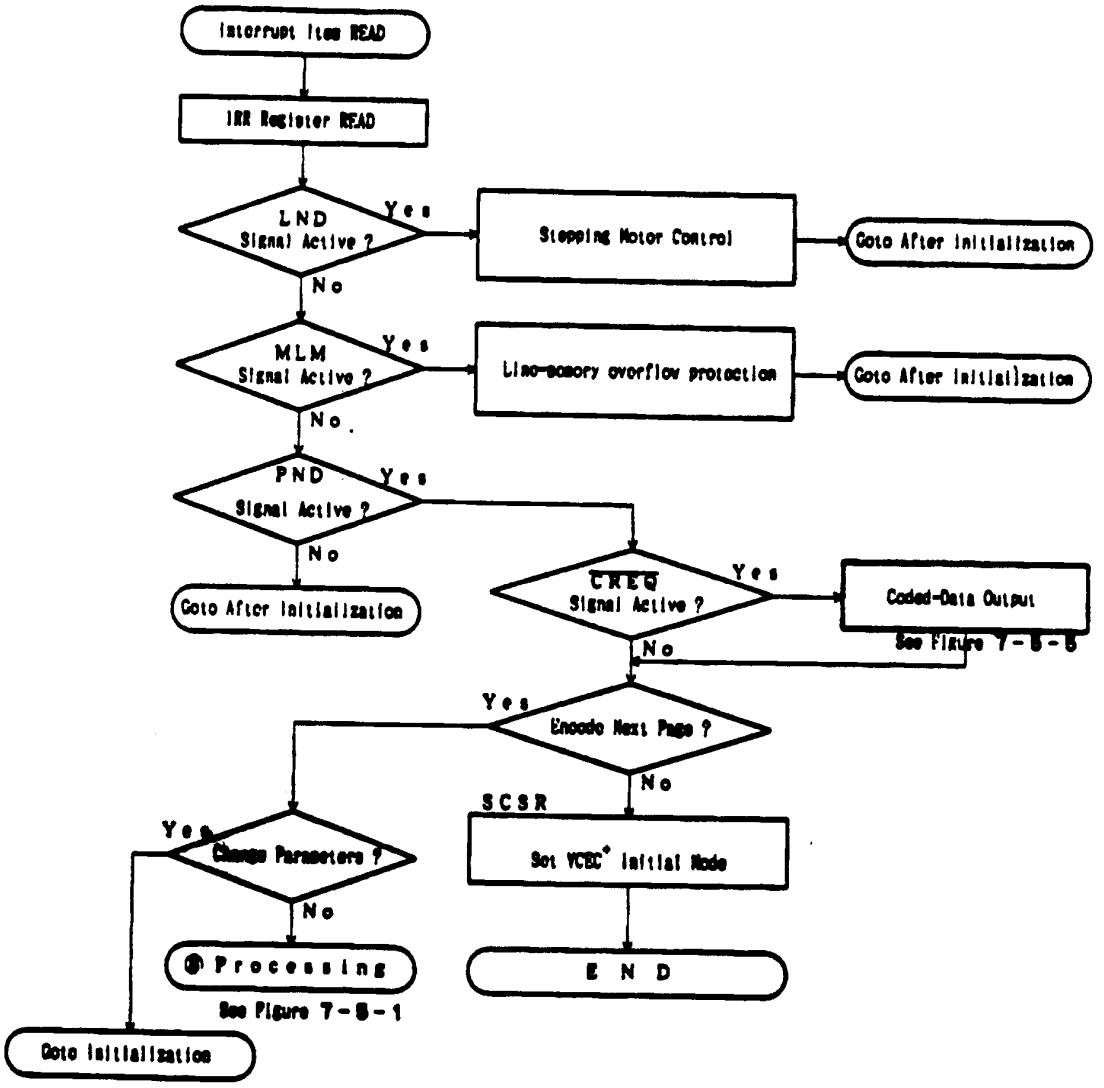


Figure 7-8-4 Interrupt Item Read FLOW

7. 5. 3 After Initialization (Ⅱ) [Encoding]

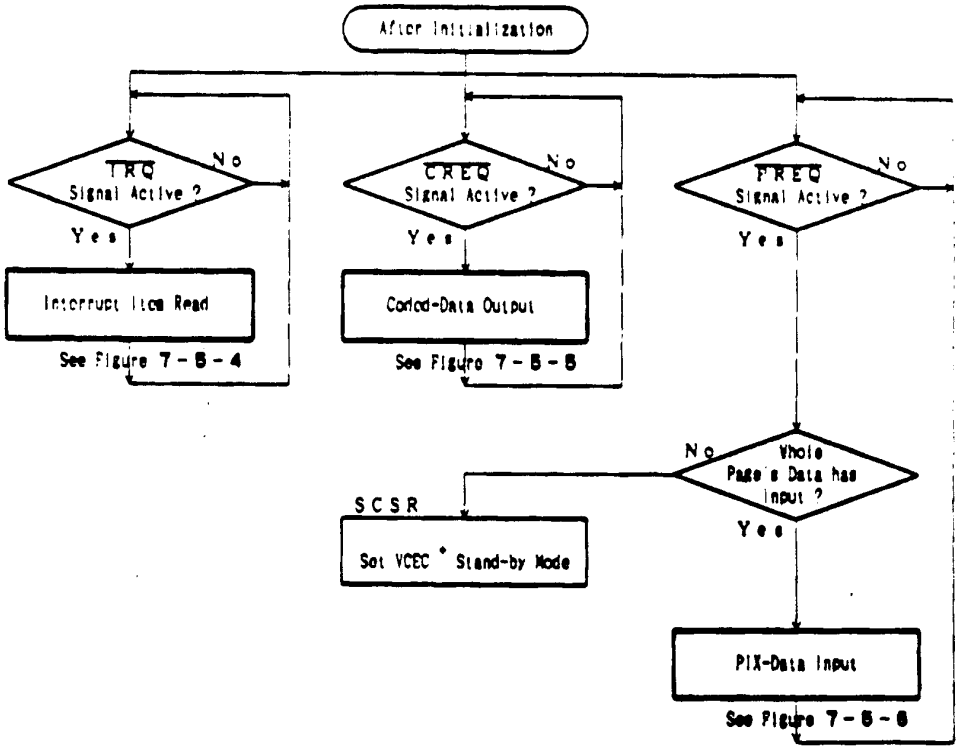


Figure 7-5-3 BUS Separate Type (For High Speed Facsimile) Encoding FLOW

7. 5. 2 After Initialization (I) [Encoding]

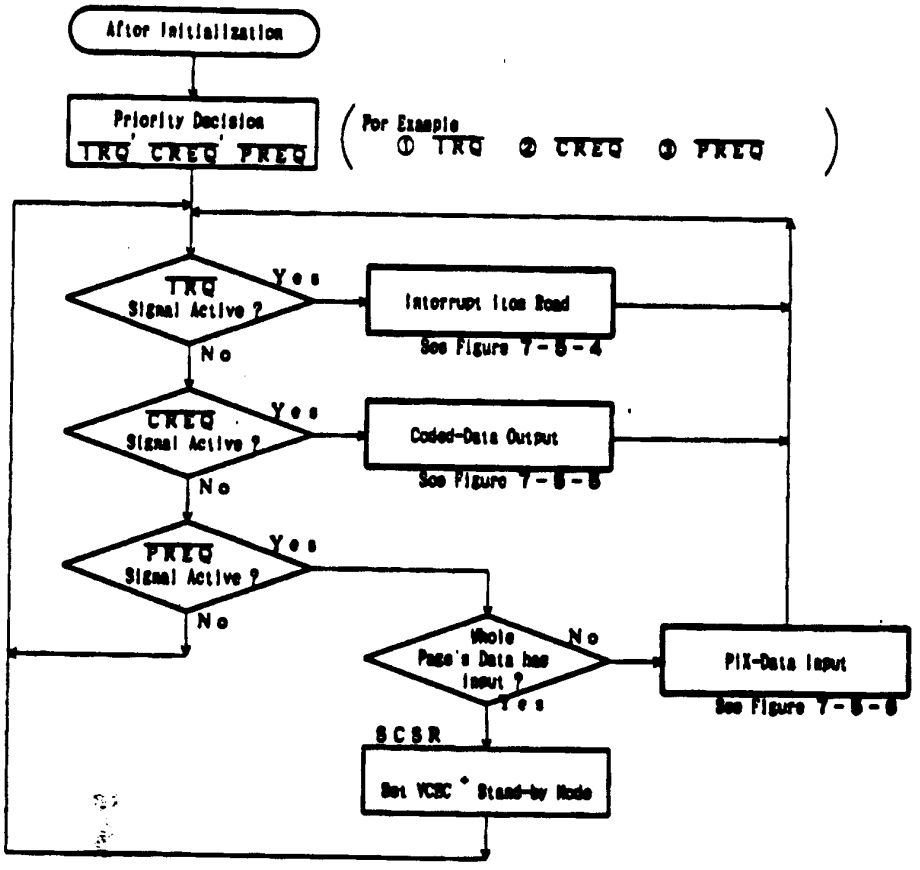


Figure 7-5-2 BUB Combined Type (For Small Size Facsimile) Encoding FLOW

7. 5. 1 Initialization

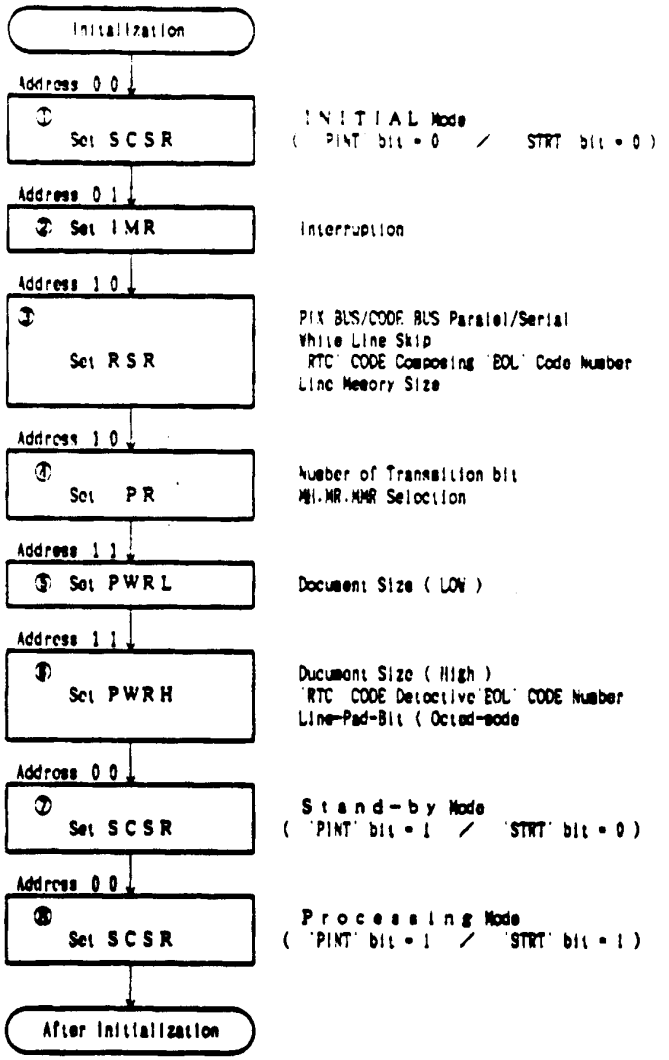
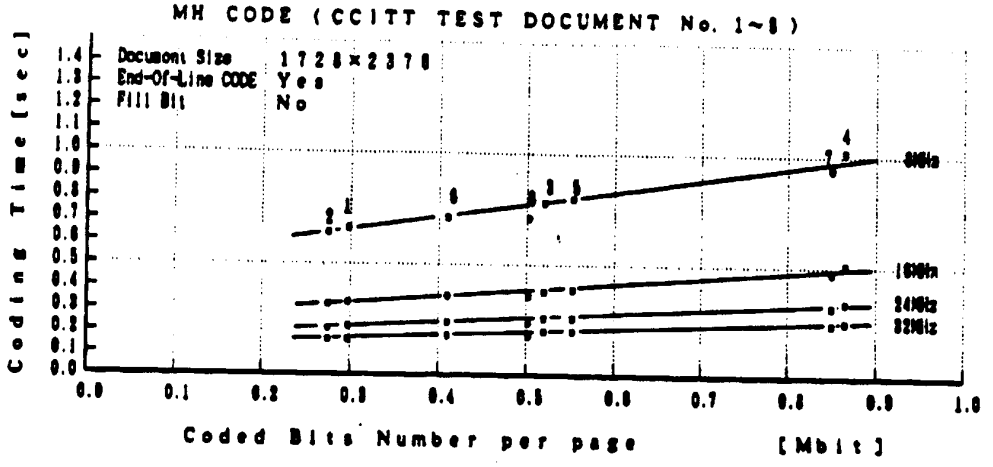
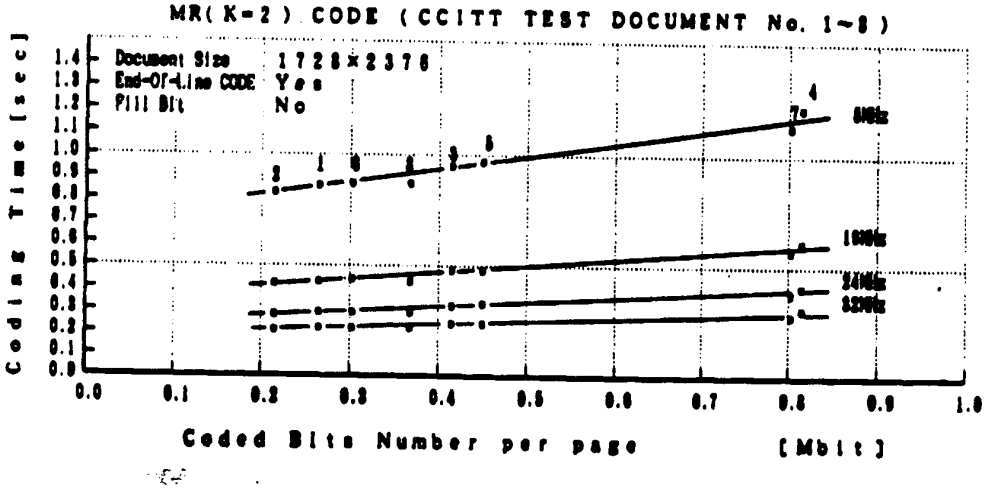


Figure 7 - 8 - 1 Initialization FLOW





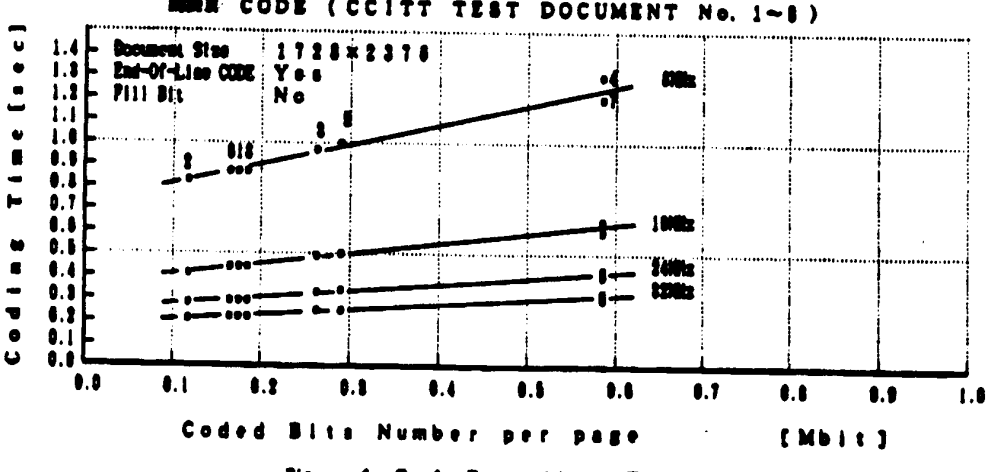
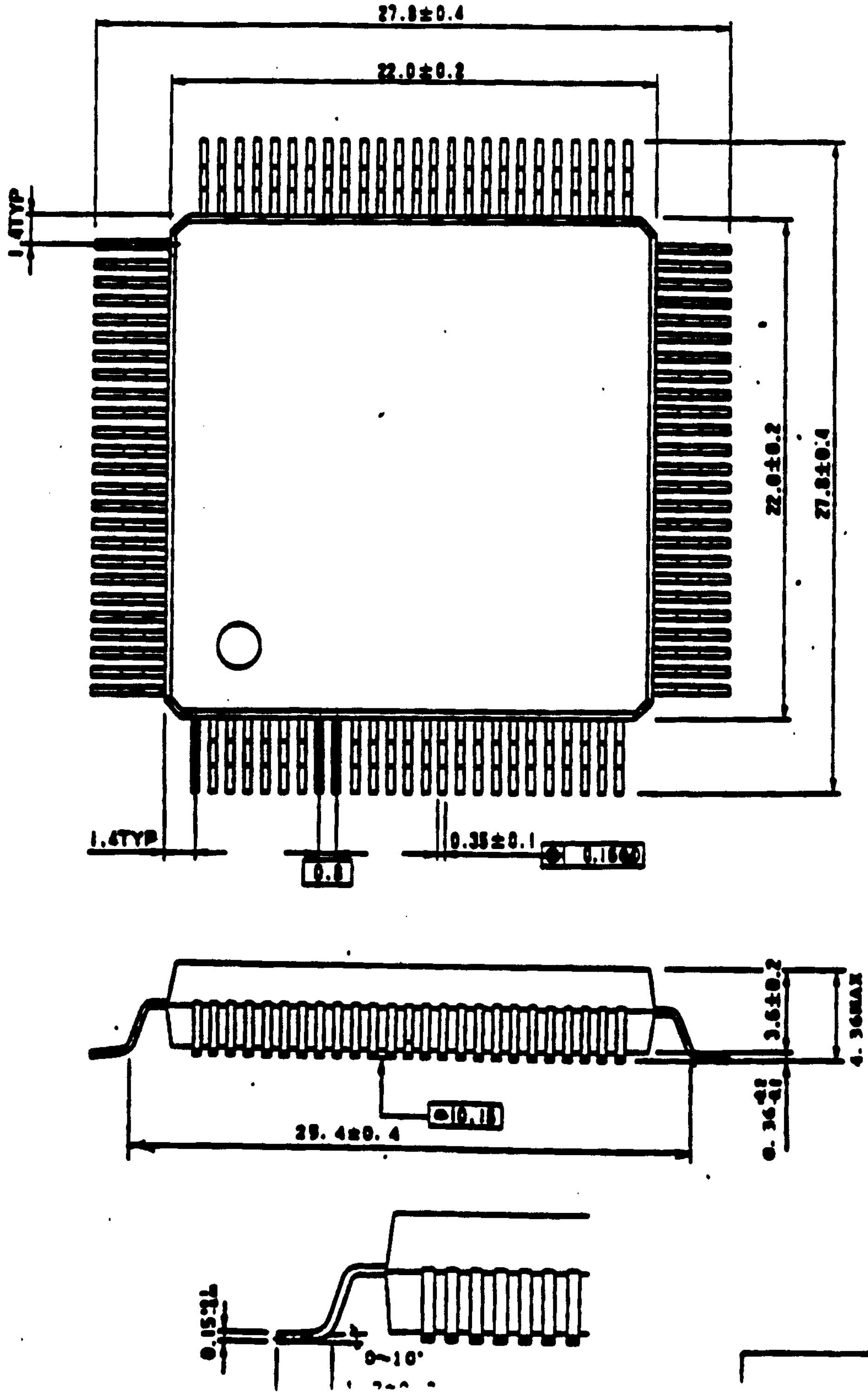


Figure 1-3-1 Encoding Time

TOSHIBA INTEGRATED CIRCUIT TECHNICAL DATA

TC35190F

100 Pin Plastic Flat Package UNIT (mm)



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