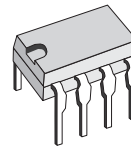


SWITCH MODE POWER SUPPLY SECONDARY CIRCUIT

- INTERNAL PWM SIGNAL GENERATOR
- POWER SUPPLY WIDE RANGE 4.5V – 14.5V
- SOFT START
- REFERENCE VOLTAGE $2V \pm 5\%$
- WIDE FREQUENCY RANGE 250kHz
- MINIMUM OUTPUT PULSE WIDTH 500nS
- MAXIMUM PRESET DUTY CYCLE
- SYNCHRONIZATION WINDOW
- OUTPUT SWITCH
- UNDERVOLTAGE LOCKOUT
- FREQUENCY RANGE WITH SYNCHRONIZATION 64kHz



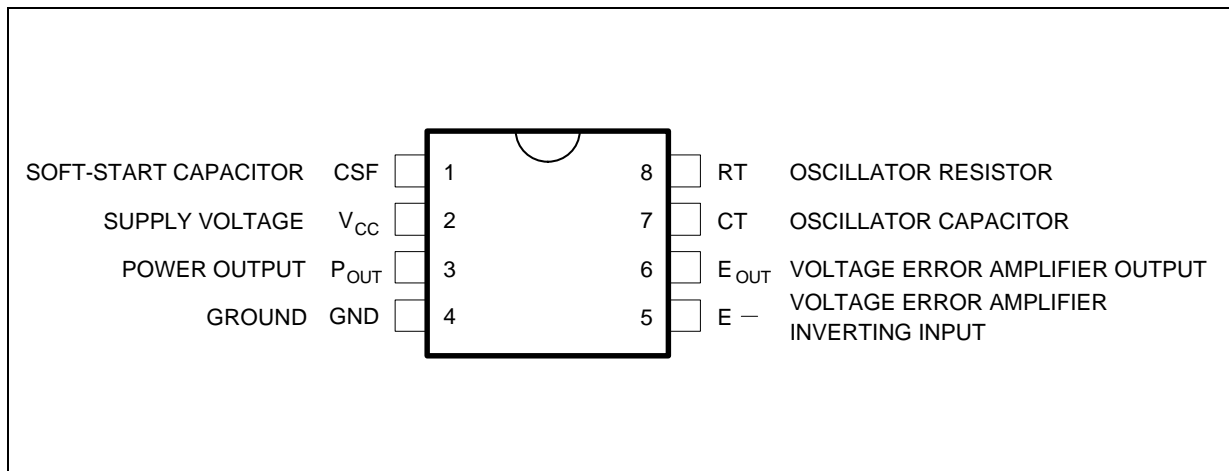
DIP8
(Plastic Package)

ORDER CODE : TEA5170

DESCRIPTION

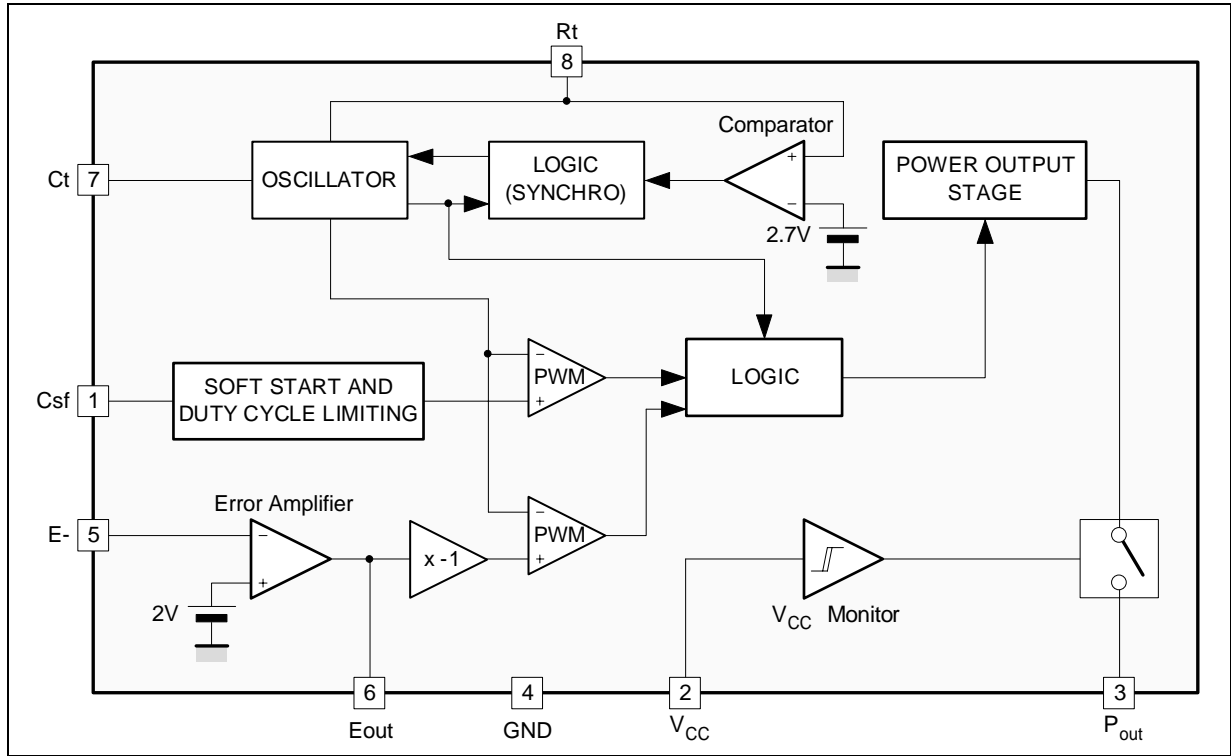
The TEA5170 is designed to work in the secondary part of an off-line SMPS, sending pulses to the slaved TEA2260/61 which are located on the primary side of the main transformer. An accurate regulated voltage is obtained by duty cycle control. The TEA5170 can be externally synchronized by higher or lower frequency signal, then it could be used in applications like TV set ones. For more details, refer to application note AN408/0591.

PIN CONNECTIONS



5170-01.EPS

BLOCK DIAGRAM



5170-02.TBL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	15	V
T _j	Operating Junction Temperature	150	°C
T _{stg}	Storage Temperature Range	- 40, + 150	°C

5170-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th (j-a)}	Junction-ambient Thermal Resistance	90	°C/W

5170-02.TBL

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Power Supply Voltage	5		14	V
R _T	Timing Resistor	47		180	kΩ
C _T	Timing Capacitor	0.12		1.8	nF
F _{osc}	Oscillator Frequency	12		250	kHz
F _{sy}	Synchro Frequency	12		64	kHz
T _{amb}	Operating Ambient Temperature	- 20		70	°C
V _{RT}	Voltage on Pin RT (8)			7	Volt
V _{CT}	Current on Pin CT (1)			100	μA
I _{SOURCE}	Output Current		30	60	mA

5170-03.TBL

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OSCILLATOR						
TA	Free Period	$R_T = 100\text{k}\Omega \pm 0\%$ $C_T = 1.2\text{nF} \pm 0\%$, $V_{CC} = 12\text{V}$	60.40	65.60	70.80	μS
TB		$R_T = 100\text{k}\Omega \pm 0\%$ $C_T = 560\text{pF} \pm 0\%$, $V_{CC} = 12\text{V}$	29.18	31.70	34.22	μS
$\Delta F_{\text{OSC}}(T)$	Frequency drift due to ambient temperature variation from 0°C to 70°C $\frac{F_{\text{OSC}}(70^\circ\text{C}) - F_{\text{OSC}}(0^\circ\text{C})}{70^\circ\text{C} \times F_{\text{OSC}}(25^\circ\text{C})}$	$R_T = 100\text{k}\Omega \pm 0\%$ $C_T = 1.2\text{nF} \pm 0\%$, $V_{CC} = 12\text{V}$		0.01		$\%/^\circ\text{C}$
$\Delta F_{\text{OSC}}(V_{CC})$	Frequency drift due to V_{CC} variation from 5V to 12V $\frac{F_{\text{OSC}}(12\text{V}) - F_{\text{OSC}}(5\text{V})}{7\text{V} \times F_{\text{OSC}}(12\text{V})}$	$R_T = 100\text{k}\Omega \pm 0\%$ $C_T = 1.2\text{nF} \pm 0\%$		0.07		$\%/V$

ERROR VOLTAGE AMPLIFIER ($V_{CC} = 12\text{V}$)

Ibias	Input Bias Current	$E_{in} = 2\text{V}$	0	0.2	1	μA
Gvol	Voltage Gain			80		dB
GB	Gain Bandwidth			2		MHz
	Slew Rate			2		$\text{V}/\mu\text{s}$

INTERNAL VOLTAGE REFERENCE

V_{REF}	Voltage Reference	Using the voltage error amplifier as a follower	1.9	2	2.1	V
$\Delta V_{\text{REF}}(V_{CC})$	Line Regulation $\frac{V_{\text{REF}}(12\text{V}) - V_{\text{REF}}(5\text{V})}{7\text{V}}$	$V_{CC} = 5\text{V}$ to 12V	-3	0.4	3	mV/V
$\Delta V_{\text{REF}}(T)$	V_{REF} drift with temperature $\frac{V_{\text{REF}}(70^\circ\text{C}) - V_{\text{REF}}(0^\circ\text{C})}{70^\circ\text{C}}$	$T_A = 0^\circ\text{C}$ to 70°C		0.2		$\text{mV}/^\circ$

T_{ON MIN}

T _{ONMIN A}	Minimum Duty Cycle	$C_t = 1.2\text{nF} \pm 0\%$ $R_t = 100\text{k}\Omega \pm 0\%$	1.77	2.53	3.29	μs
T _{ONMIN B}	Minimum Duty Cycle	$C_t = 560\text{pF} \pm 0\%$ $R_t = 100\text{k}\Omega \pm 0\%$	1.04	1.49	1.94	μs

POWER OUTPUT STAGE

V_{POUTH}	Output High Level	$I_{\text{load}} = 1\text{mA}$	6.3	6.9	7.5	V
V_{POUTL}	Output Low Level	$I_{\text{load}} = -1\text{mA}$	0.5	0.8	1.1	V
I_{SINK}	Sink Current	$V_{\text{POUT}} = 3\text{V}$	30	60	190	mA
I_{SOURCE}	Source Current	$V_{\text{POUT}} = 3\text{V}$	30	110	190	mA

SYNCHRONISATION

$F_{\text{trig Max}}$	Maximum Synchro Frequency		64			kHz
V_{trig}	Synchro Triggering Threshold			2.7	3	V
T_{trigp}	Synchro Triggering Pulse Width	at $V_{RT} = 2.7\text{V}$ (fig 5)	800			nS
$W_{\text{trig}+}$	Positive Triggering Window $\frac{T_{\text{trig}+} - T_0}{T_0}$	$C_T = 1.2\text{nF} \pm 0\%$ $R_T = 100\text{k}\Omega \pm 0\%$	25	35	40	%
$W_{\text{trig}-}$	Negative Triggering Window $\frac{T_0 - T_{\text{trig}-}}{T_0}$	$C_T = 1.2\text{nF} \pm 0\%$ $R_T = 100\text{k}\Omega \pm 0\%$	9	29	42	%

SOFT START

I_{csf}	*Csf Load Current	$V_{\text{csf}} = 1\text{V}$	2.5	3.7	6	μA
Donmax	Maximum Duty Cycle	$V_{\text{CS}} > 2.5\text{V}$, $V_{\text{CC}} = 12\text{V}$ $C_T = 1.2\text{nF} \pm 0\%$ $R_T = 100\text{k}\Omega \pm 0\%$	60	78	95	%

*Csf is a high impedance capacitor

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$, unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC} MONITOR						
V_{START}	Turn-on Threshold		3.60	4	4.40	V
V_{HYST}	Hysteresis Voltage		100			mV
V_{STOP}	Turn-off Threshold		3.50			V
TOTAL DEVICE						
I_{CC}	Supply Current	$R_T = 100\text{k}\Omega \pm 0\%$, $C_T = 1.2\text{nf} \pm 0\%$ No Load on Pin 3, $V_{CC} = 12\text{V}$	7	12	25	mA

5170-05.TBL

GENERAL DESCRIPTION

The TEA5170 takes place in the secondary part of an isolated off-line SMPS. During normal mode operation, it sends pulses to the slave circuit located in the primary side (TEA2164, TEA2260/61) through a pulse transformer to achieve a very precisely regulated voltage by duty cycle control.

The main blocs of the circuit are :

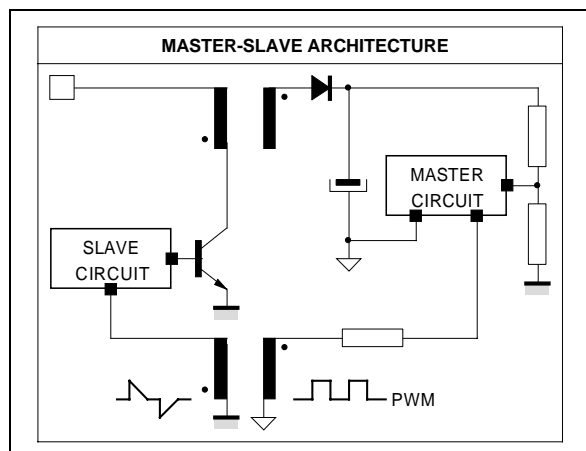
- an error voltage amplifier
- an RC oscillator
- an output stage
- a V_{CC} monitor
- a voltage reference bloc
- a pulse width modulator
- two logic blocs
- a soft start and Duty cycle limiting bloc

PRINCIPLE OF OPERATION

The TEA5170 sends pulses continuously to the slave circuit in order to insure a proper behaviour of the primary side.

- According to this, the output duty cycle is varying between $D_{ON (min.)}$ (0.05) and $D_{ON (max.)}$ (0.75) : then even in case of open load, pulses are still sent to the slave circuit.

Figure 1 : Basic Concept

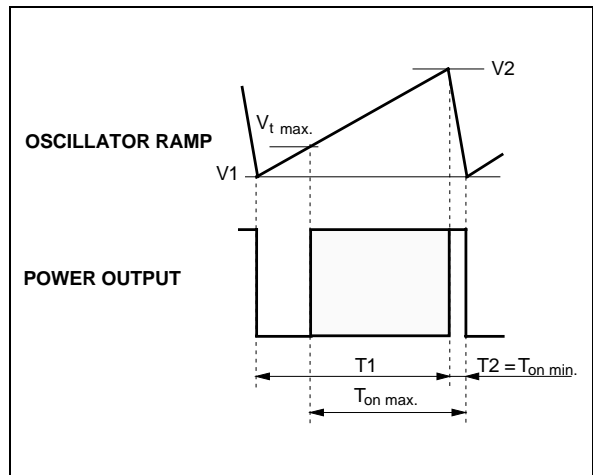


5170-03.EPS

ASYNCHRONIZED MODE (Figure 2)

The regulated voltage image is compared to 2V vol-tage reference. The error voltage amplifier output and the RC oscillator voltage ramp are applied to the internal Pulse Width Modulator Inputs. The PWM logic Output is connected to a logic bloc which behaves like a RS latch, sets by the PWM output and resets when C_t downloading occurs. Finally, the push-pull output bloc delivers square wave signal whom output leading edge occurs during C_t uploading time, and output trailing edge at C_t downloading time end. The duty cycle is limited to 75% of oscillator period as maximum value and to C_t downloading time/oscillator period as minimum value (Figure 2).

Figure 2

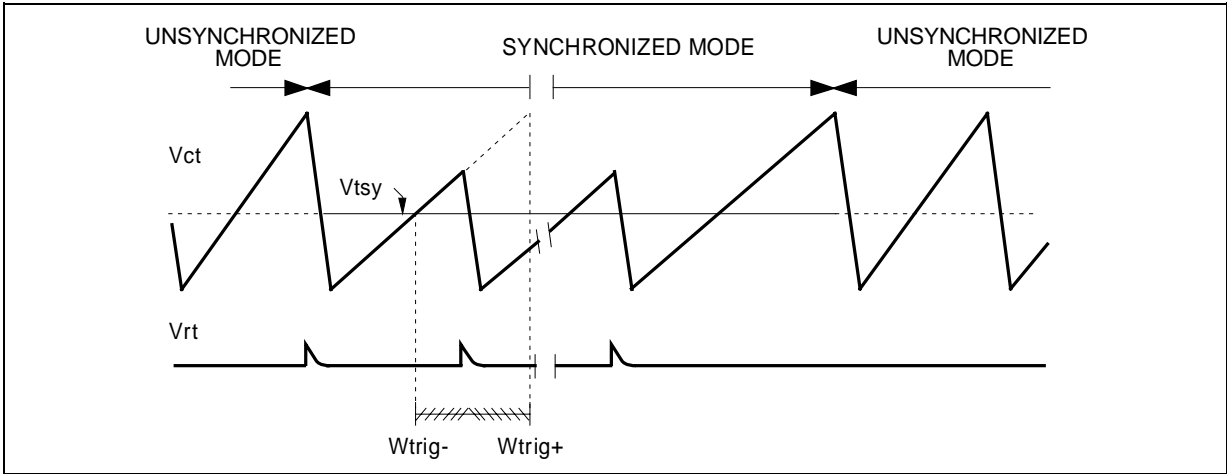


5170-04.EPS

SYNCHRONIZED MODE (see Figure 3)

The TEA5170 will enter the Synchronized Mode when it receives one pulse through R_t during C_t discharge. At that time C_t charging current will be multiplied by 0.75 and period will increase up to $T_o \times 1.26$. A pulse occurring during the synchro window, commands the C_t downloading. If none, the TEA5170 will return to normal mode at the end of the period.

Figure 3



Remark : In case of an application between TEA5170 and TEA2164, to optimize the synchronization windows of these circuits, the following relations have to be used :

$$T_m = \frac{T_{SYNC}}{1.06} T_e = \frac{T_m}{1.223}$$

with T_e : Free period of the TEA2164 oscillator, and T_m : Free period of the TEA5170 oscillator.

BLOCK DESCRIPTION

The error voltage amplifier inverting-input and output are accessible to use different feed-back network and allowing parasitic filtering network. The non-inverting input is internally connected to 2V reference voltage.

The RC oscillator is designed to work at high frequency (up to 250kHz). R_T sets the capacitor charging current $I_o = 2/R_T$.

The capacitor C_T is loaded from $V_1 \approx 1V$ to $V_2 = 2V$ during $T_1 = \frac{C_T R_T}{1.985}$ and then down loaded through an integrated resistor $R_2 \approx 1k\Omega$ during $T_2 = 1300 C_T$. The ramp is used to limit the duty cycle. Then the maximum duty cycle is

$$DONMAX = \frac{1}{T_1 + T_2} (0.73 T_1 + T_2)$$

The output level is V_{CC} independant when V_{CC} is over 8V.

The V_{CC} monitoring switches the circuit on when V_{CC} is over 4V and switches it off when under 3.8V. This function insures a proper starting procedure (made by the primary side circuit).

SYNCHRONIZATION
(see Figures 4 and 5)

Figure 4 : Triggering Schematic

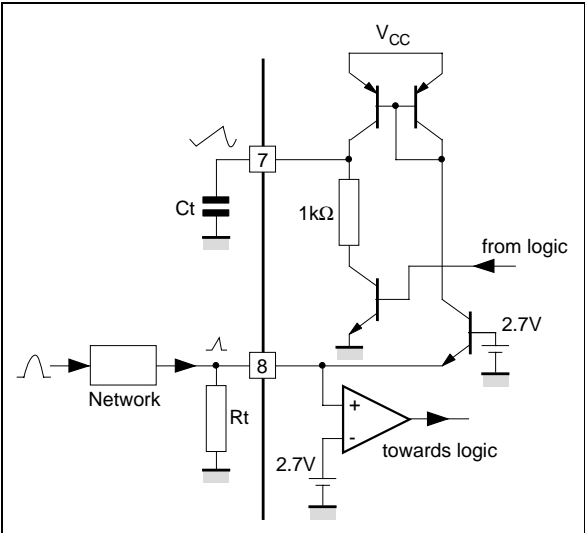
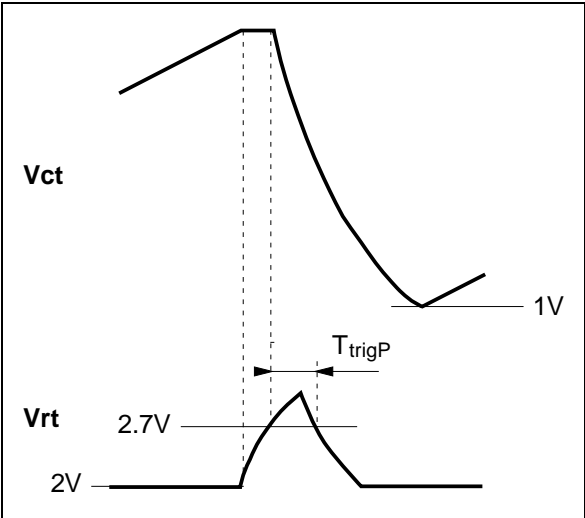


Figure 5 : Typical Waveforms



STARTING

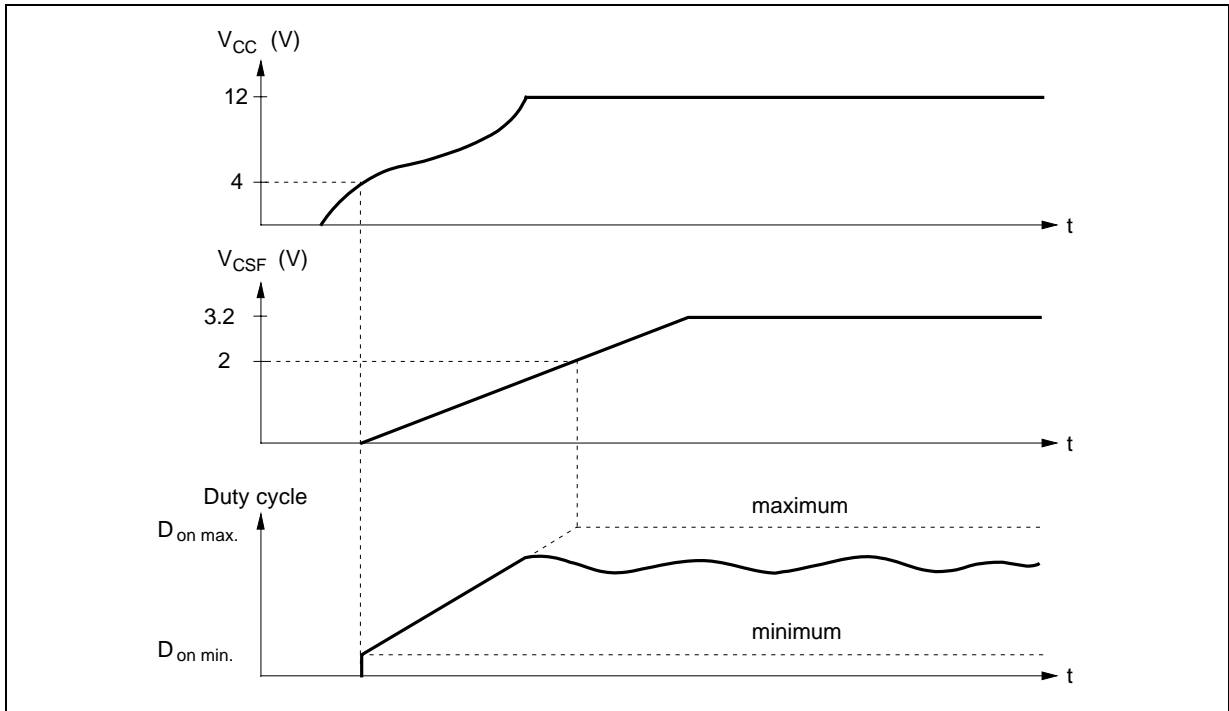
When V_{CC} is under 4V, output pulses are not allowed and the slave circuit keeps its own mode. When V_{CC} is going over 4V, output pulses are sent via the pulse transformer (or an optical device) to the slave circuit which is synchronizing and entering the slaved mode. Output pulses can be shut down only if V_{CC} goes below 3.8 Volt.

SOFT START

Using C_{sf} , it is possible to make a soft start sequence. When V_{CC} grows from 0V to 4V, voltage on C_{sf} equals 0V. When V_{CC} is higher than 4V, C_{sf} is loaded by a $3.7\mu A$ current, then T_{onMAX} (V_{csf}) will vary linearly from T_{onmin} to T_{onmax} according to C_{sf} st bias.

When V_{CC} will go low (3.8 Volt threshold), C_{sf} will be downloaded by an internal transistor.

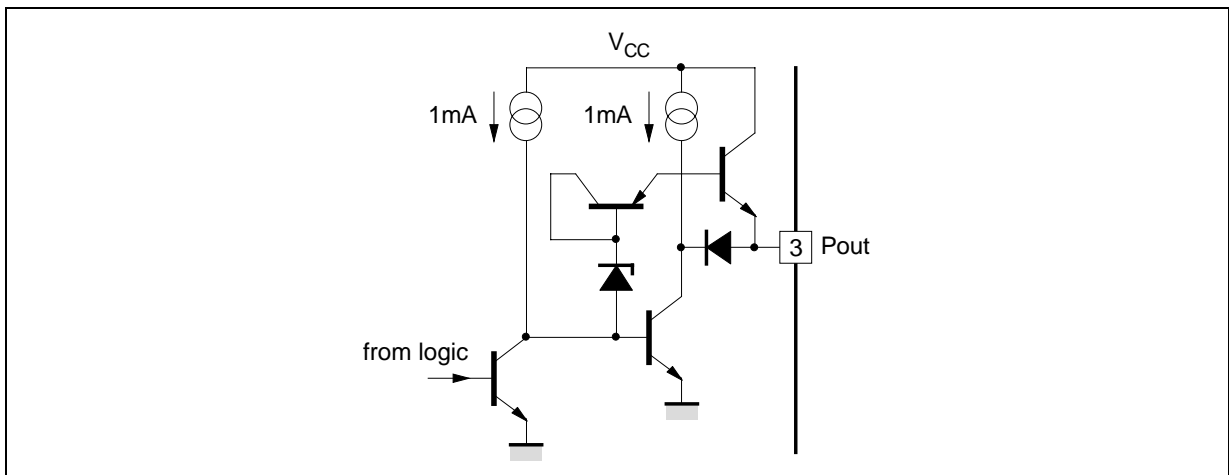
Figure 6 : Soft-Start Sequence



5170-08.EPS

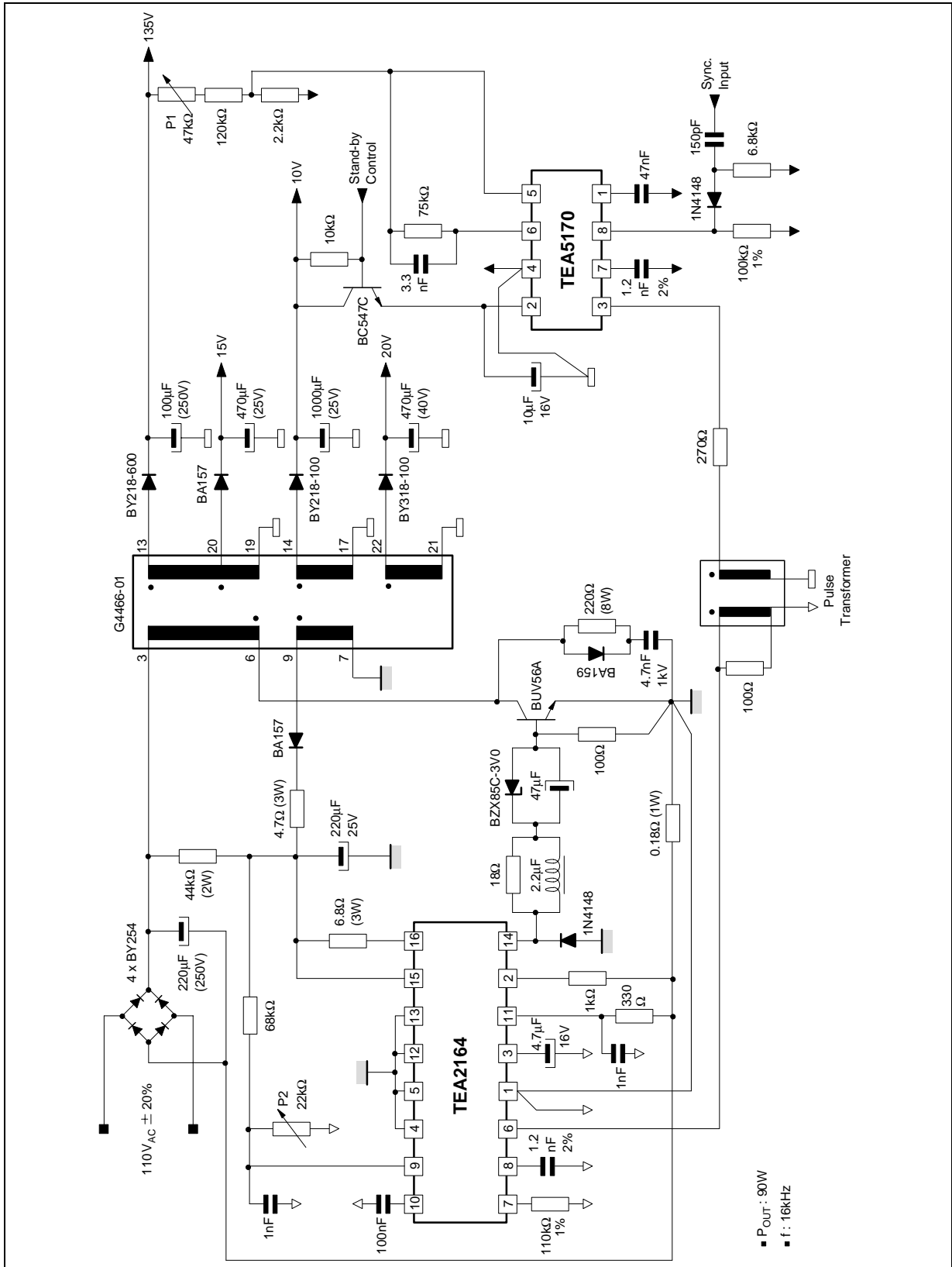
POWER OUTPUT STAGE

Figure 7 : Electrical Schematic



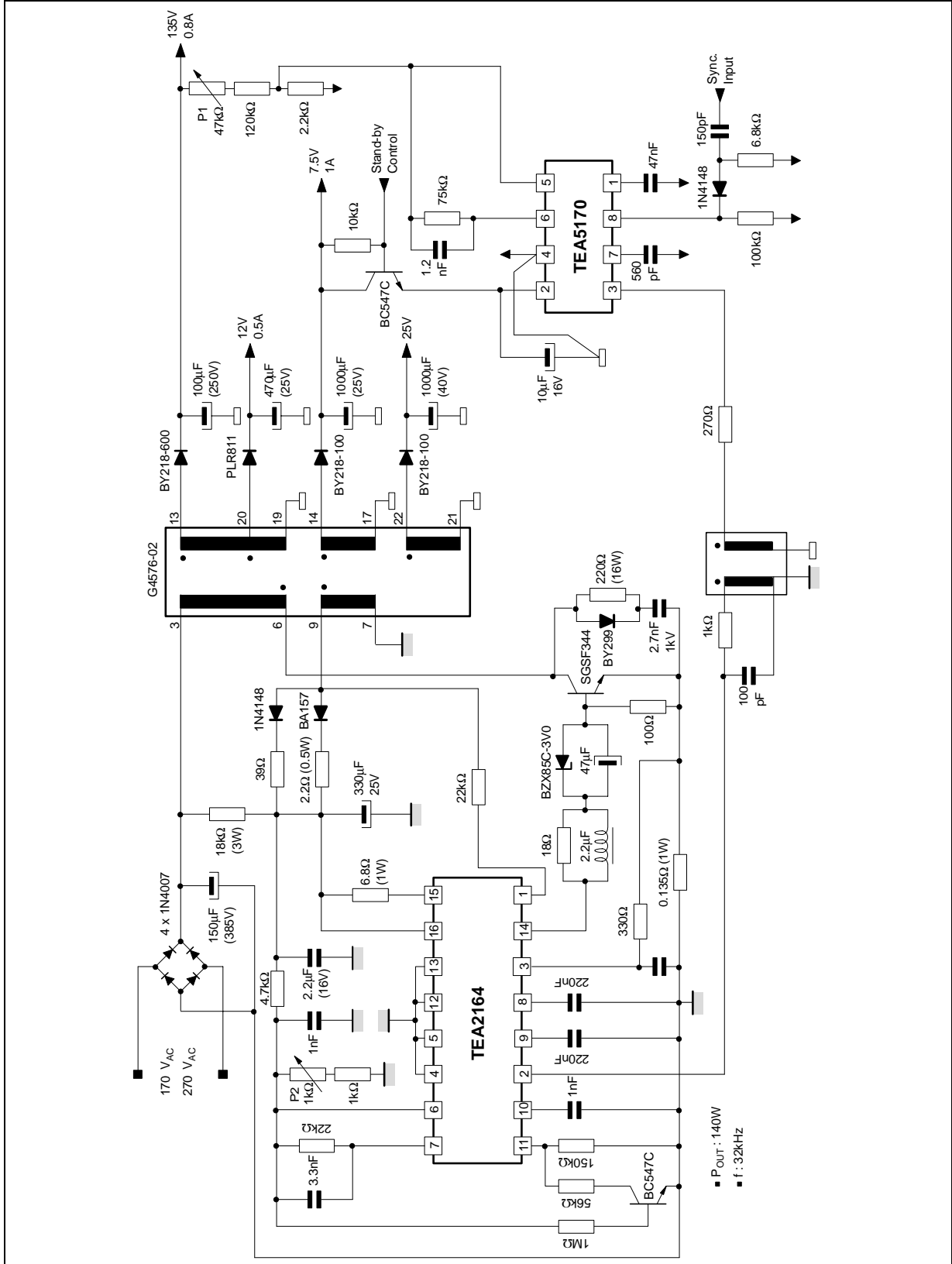
5170-09.EPS

Figure 8

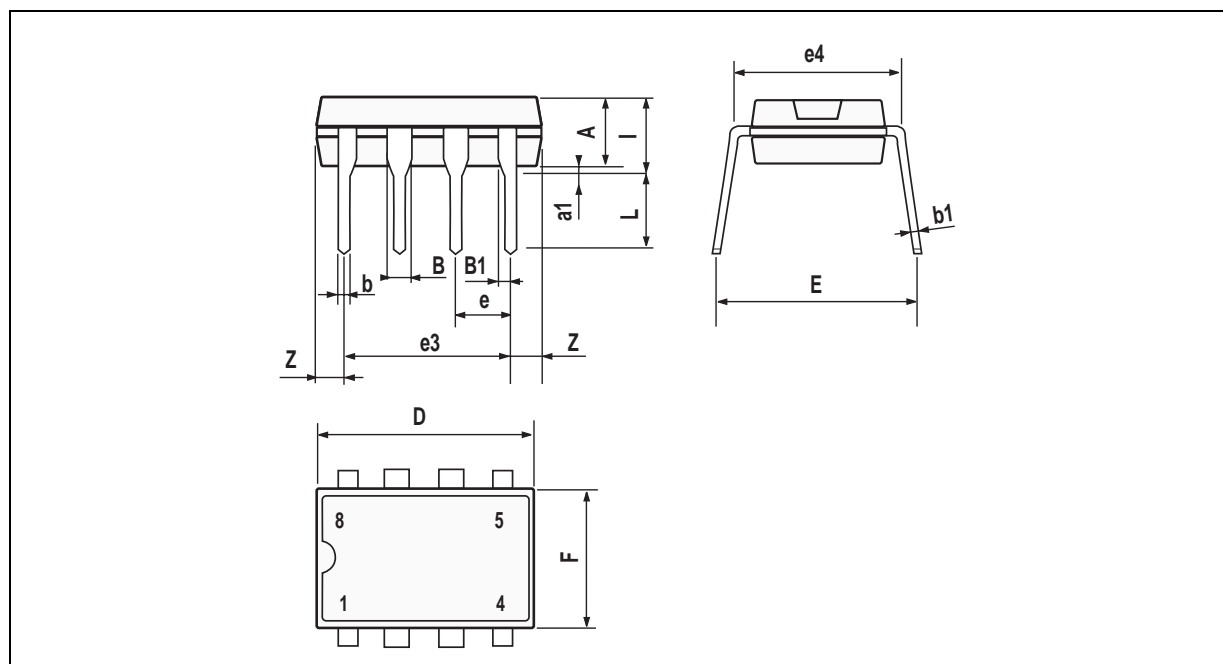


5170-10.EPS

Figure 9



5170-11.EPS

PACKAGE MECHANICAL DATA
 8 PINS - PLASTIC DIP


PM-DIP8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL

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