CMOS 4-BIT MICROCONTROLLER

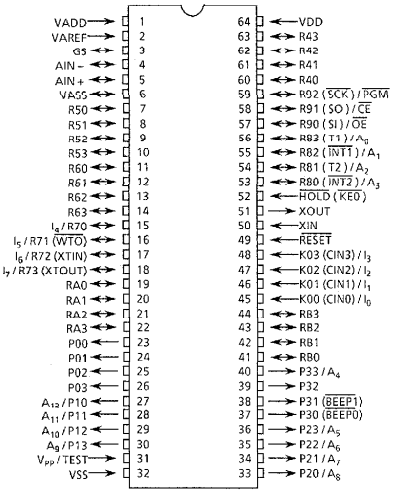
TMP47P850VN
TMP47P850VF

The 47P850V is the OTP microcontroller with 64Kbits PROM. For program operation, the programming is achieved by using with EPROM programmer (TMM2764AD type) and adapter socket (BM1161, BM1165). The function of this device is exactly same as the 47C850.

PART No.	EPROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P850VN	OTP 8192×8-bit	512×4-bit	SDIP64-P-750-1.78	BM1161
TMP47P850VF			QFP64-P-1420-1.00A	BM1165

PIN ASSIGNMENT (TOP VIEW)

SDIP64-P-750-1.78



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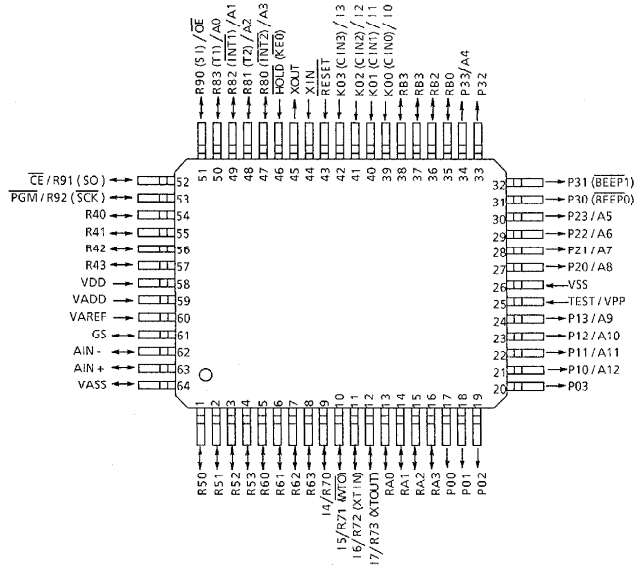

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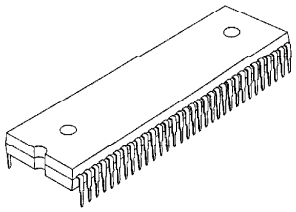

TMP47P850VN

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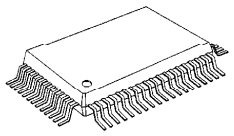


TMP47P850VF

PIN FUNCTION

The 47P850V has MCU mode and PROM mode.

(1) MCU mode

The 47C850 and the 47P850V are pin compatible (TEST pin for out-going test. Be fixed to low level).

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS	PIN NAME(MCU mode)
A12 - A9	INPUT	Address inputs	P10 - P13
A8 - A5			P20 - P23
A4			P33
A3 - A0			R80 - R83
I7 - I4	I/O	Data outputs (Inputs)	R73 - R70
I3 - I0			K03 - K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$			R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
P03 - P00	output	Open	
P32 - P30			
RA3 - RA0	I/O		
RB3 - RB0			
R43 - R40		Be fixed to Low Level	
R53 - R50			
R63 - R60			
$\overline{RESET}$	Input	PROM mode setting pin. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pin	
XOUT	output		
$A_{IN}+$, $A_{IN}-$	Input	Open	
VAREF, GS	output		
VADD	Power supply	+ 5V	
VASS		0V (GND)	

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P850V. The 47P850V is the same as the 47C850 except that an OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P850V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C850, except that the TEST/VPP pin does not have built in pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C850.

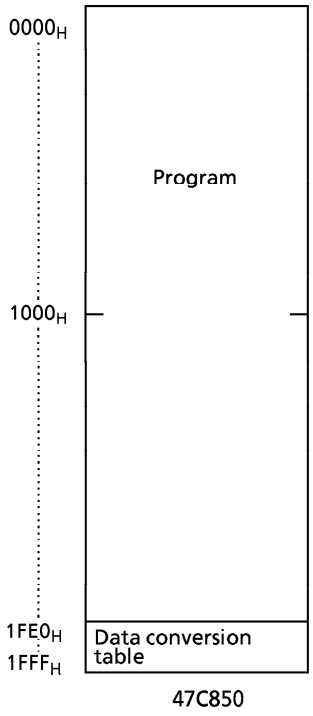


Figure 1-1. Program area

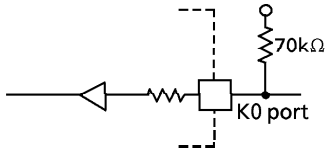
1.1.2 Data Memory

The 47P850V has 512 × 4-bit of data memory (RAM).

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C850 except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit is the same as I/O code WB of the 47C850 except that there is no built-in pull-up resistance for the K0 port.
External resistance, for example, is required when using as evaluator of other I/O codes (WB). (Refer to Figure 1.2)

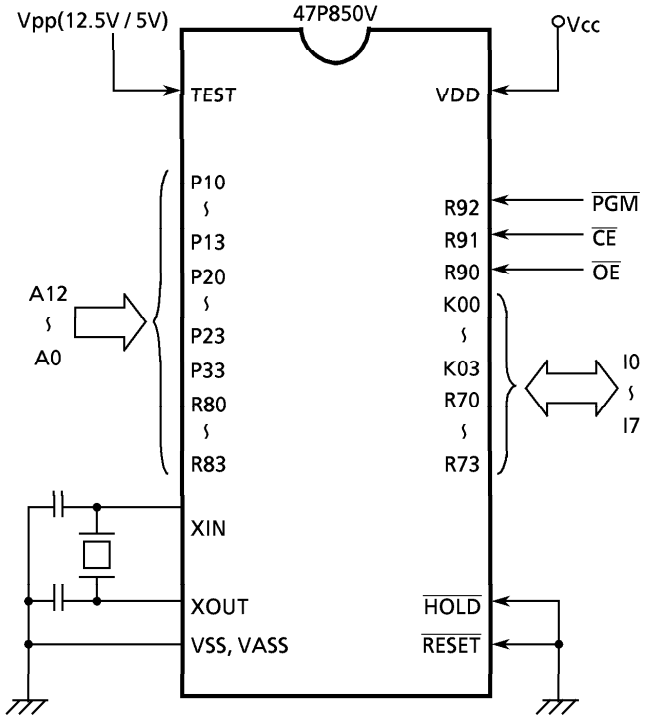


Equivalent to IO code WB

Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$ pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM 2764AD.)



For mode information on pins, refer to the section on pin functions.

Adapter socket

Name	Applicable products
• BM1161	TMP47P850VN
• BM1165	TMP47P850VF

Figure 1-3. Setting for PROM mode

1.2.1 High Speed Programming Mode

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+ 12.5V) is applied to the V_{PP} terminal with V_{CC} = 6V and $\overline{PGM} = V_{IH4}$.

The programming is achieved by applying a single low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 15 times).

After correctly programming the selected address, one additional program pulse with pulse width 4 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

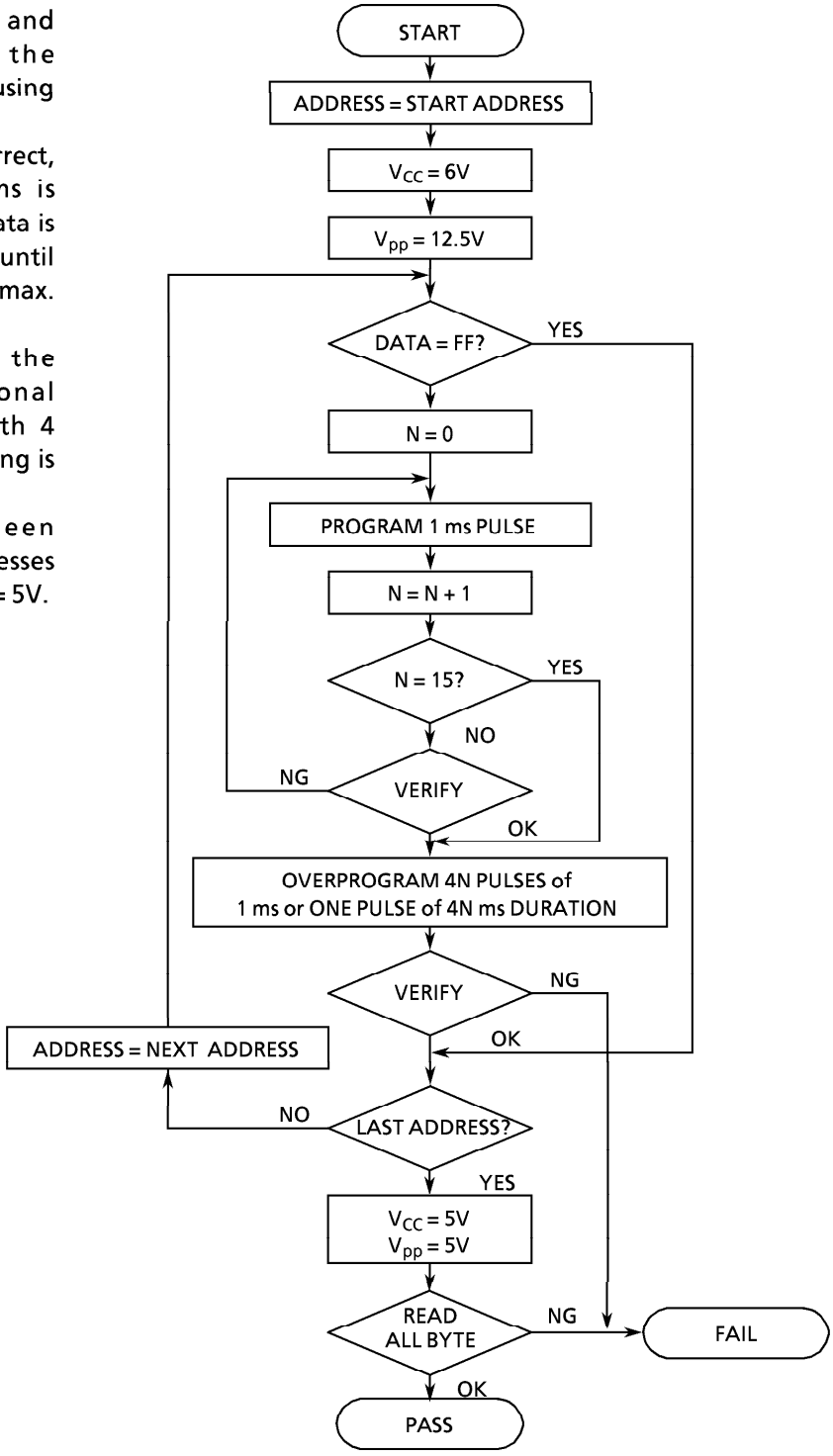


Figure 1-4. FLOW CHART

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Program Voltage	V_{PP}	TEST / VPP pin	– 0.3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Ports P0, P3, R7, RA, RB	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Ports P1, P2, R4, R5, R6, R8, R9	– 0.3 to 10	
Output (Per 1 pin)	I_{OUT1}	Port R	3.2	mA
	I_{OUT2}	Ports P1, P2	30	
Output Current (Total)	ΣI_{OUT2}	P Ports	240	mA
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	℃
Storage Temperature	T_{stg}		– 55 to 125	℃
Operating Temperature	T_{opr}		– 30 to 60	℃

Note. Characteristic of R7 is different from 47C850

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, Topr = – 30 to 60℃)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	5.5	V
			in the SLOW mode	2.7		
			in the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		3.5759	3.5831	MHz
	fs	XTIN, XTOUT		30	34	kHz

A / D CONVERSION CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = – 30 to 60℃)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Input Voltage	V_{AIN}	CIN3 to CIN0		V_{SS}	–	V_{DD}	V
A/D Conversion Error				–	–	$\pm\frac{1}{2}$	LSB

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 30 to 60℃)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis input		—	0.7	—	V
Input Current	I_{IN1}	port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	ports R (open-drain)					
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Low Level Input Current	I_{IL}	ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Output Leakage Current	I_{LO}	ports R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output Level High Voltage	V_{OH}	push-pull ports	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	—	—	V
Output Level Low Voltage	V_{OL}	Except XOUT, P ports	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	
Low Level Output Current	I_{OL2}	P ports	V_{DD} = 4.5V, V_{OL} = 1.0V	—	20	—	mA
Output VREF Voltage	V_{REF}	VAREF pin		2.4	—	2.7	V
Output VREF Resistance	R_{REF}		VREF = 2.55V	—	—	1	kΩ
Supply Current (in the Nomal mode)	I_{DD}	DTMF receiver stopped	V_{DD} = 5.5V fc = 3.58MHz	—	3	6	mA
	I_{DDR}	DTMF receiver moving			7	14	
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0V fs = 32.768kHz	—	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25℃, V_{DD} = 5V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. I_{DD}, I_{DDH}; V_{IN} = 5.3V / 0.2V
The voltage applied to the R port is within the valid range.
I_{DDS}; V_{IN} = 2.8V / 0.2V, low frequency clock is only oscillated (connecting XTIN, XTOUT).

OPERATIONAL AMPLIFIER CHARACTERISTICS (AIN +, AIN – to GS) (V_{SS} = 0V, V_{DD} = 5.0V, T_{opr} = 25℃)

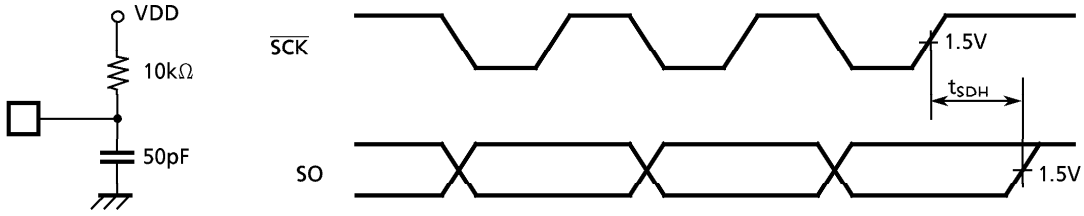
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	V_{IO}		–	± 25	–	mV
Input Offset Current	I_{IO}	$V_{SS} \leqq V_{IN} \leqq V_{DD}$	–	± 100	–	nA
Power Supply Rejection Ratio	PSRR	1kHz	–	60	–	dB
Common Mode Rejection Ratio	CMRR		–	60	–	
Open Loop Gain	A_O		–	65	–	
0 dB Band Width	f_T		–	500	–	kHz
Rated Output Voltage	V_O	GS pin (Load Resistance: 100 kΩ or over)	–	4.5	–	V_{PP}
Load Resistance	R_L	GS pin	–	30	–	kΩ
Capacitive Load	C_L		–	50	–	pF

A.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = – 30 to 60℃)

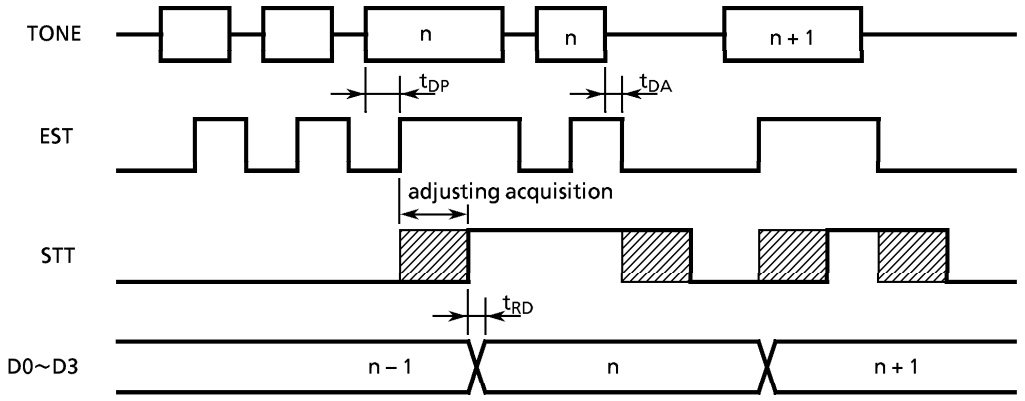
PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode	–	2.23	–	μs
		in the SLOW mode	235	–	267	
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low level Clock Pulse Width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns
Minimum Input Signal Level for Reception		Each tone composite signal	–	– 35	– 30	dBm
EST Output Delay Time	t_{DP}	"L" → "H"	5	11	14	ms
	t_{DA}	"H" → "L"	0.5	4.0	8.5	
DTMF Output Delay Time	t_{RD}		–	6	9	μs

(1) Serial Port (Completion of Transmission)

Note. Shift data Hold Time: External circuit for $\overline{SCK}$ pin and SO pin



(2) DTMF Receiver (Signal Detect Timing)



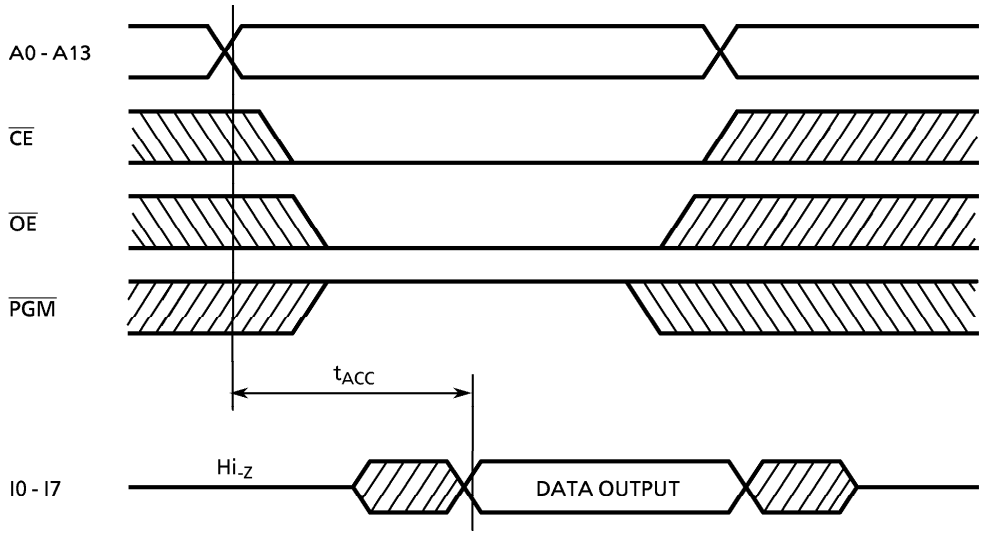
RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = – 30 to 60℃)

Recommended oscillating conditions of the 47P850V are equal to the 47C850's.

DC/AC CHARACTERISTICS (V_{SS} = 0V)

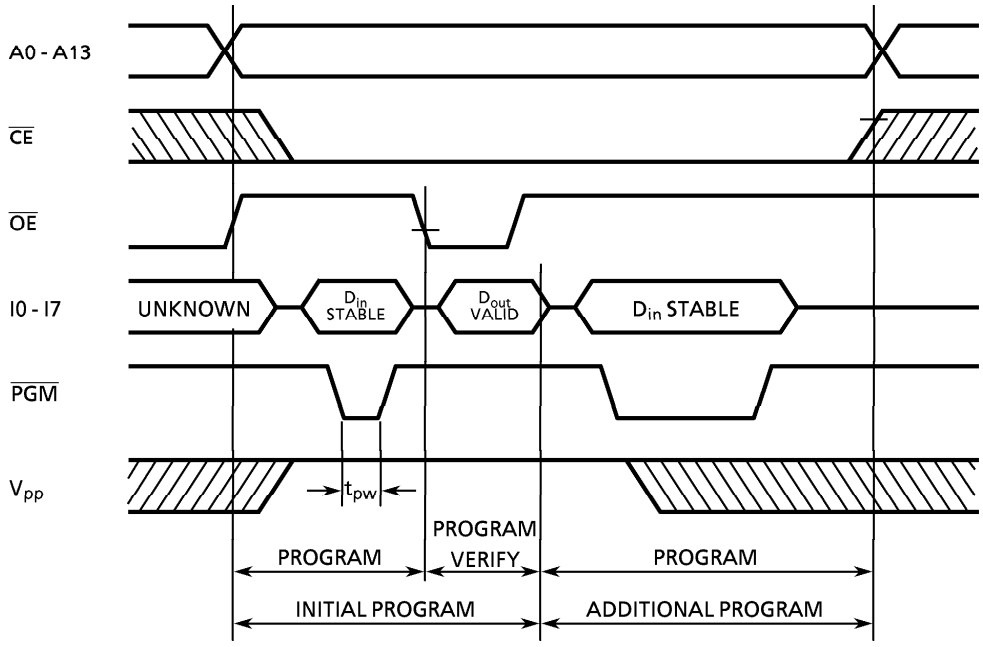
(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	0	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.0	12.50	13.0	V
Programming Pulse Width	t_{PW}	V_{CC} = 6.0 ± 0.25V	0.95	1.0	1.05	ms


A0 - A13
CE
OE
I0 - I7
UNKNOWN
Din STABLE
Dout VALID
Din STABLE
PGM
Vpp
tpw
PROGRAM
PROGRAM VERIFY
PROGRAM
INITIAL PROGRAM
ADDITIONAL PROGRAM

TYPICAL CHARACTERISTICS