CMOS 4-BIT MICROCONTROLLER

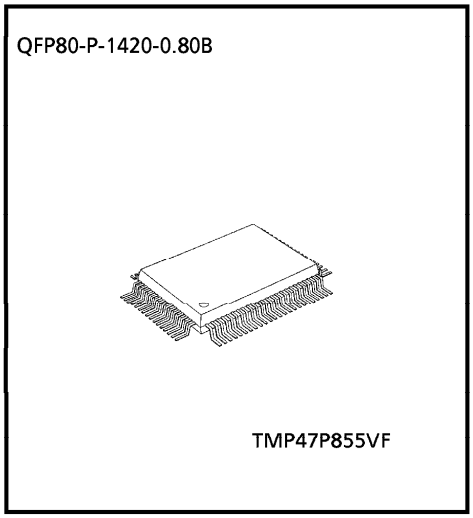
TMP47P855VF

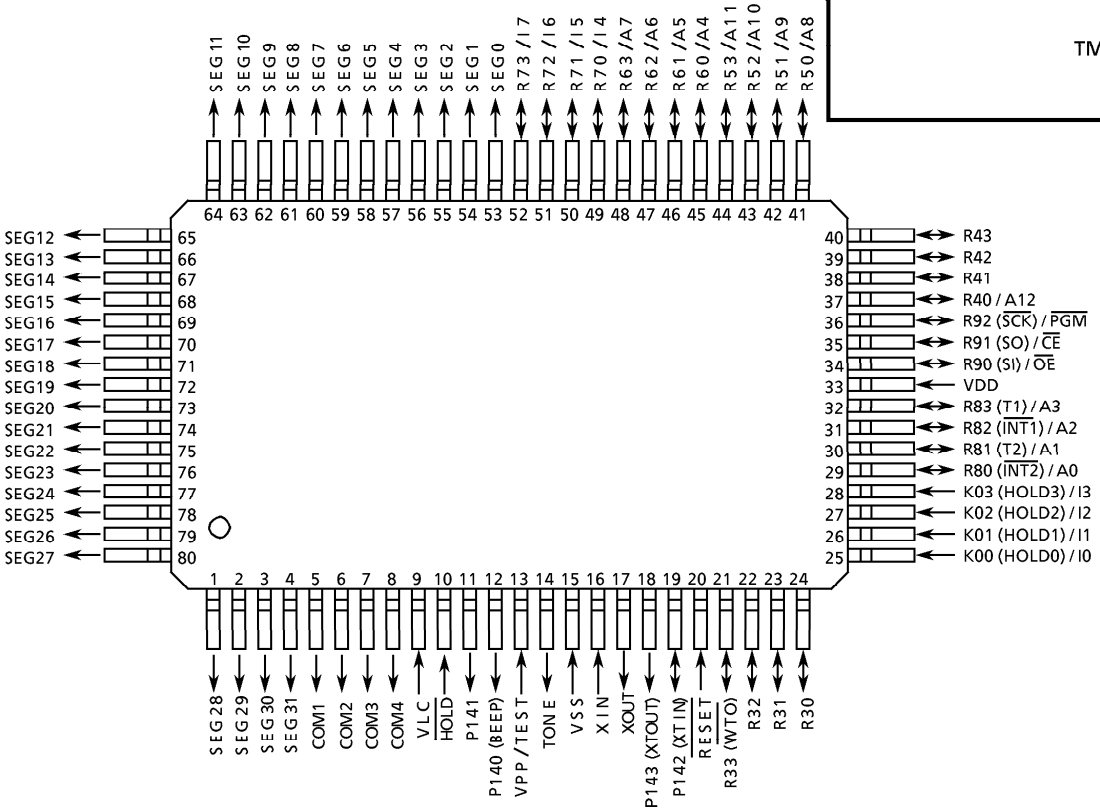
The 47P855V is the OTP microcontroller with 64kbits PROM. For program operation, the programming is achieved by using with EPROM programmer (TMM2764AD type) and adapter socket (BM1123).
A.C./D.C characteristics are equivalent to Mask-programed ROM device.

PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P855VF	OTP 8192 × 8-bit	1024 × 4-bit	QFP80-P-1420-0.80B	BM1123

PIN ASSIGNMENT (TOP VIEW)

QFP80-P-1420-0.80B





PIN FUNCTION

The 47P855V has MCU mode and PROM mode.

(1) MCU mode

The 47C855 and the 47P855V are pin compatible (TEST pin for out-going test, Be fixed to low level).

(2) PROM mode

PIN NAME	Input/Output	FUNCTIONS	PIN NAME (MCU MODE)
A12	Input	Address inputs	R40
A11 - A8			R53 - R50
A7 - A4			R63 - R60
A3 - A0			R83 - R80
I7 - I4	I/O	Data inputs / outputs	R73 - R70
I3 - I0			K03 - K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
SEG31 - SEG0	Output	Open	
COM4 - COM1			
VLC	Power supply		
TONE	Output		
R33 - R30	I/O	Be fixed to low level	
R43 - R41			
P143 - P140	Output	Open	
$\overline{RESET}$	Input	PROM mode setting pins. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	External clock input	
XOUT	Output	Open	

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P855V.
The 47P855V is the same as the 47C855 except that an OTP is used instead of a Mask ROM.

1. OPERATION MODE

The 47P855V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST / VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C655 / 855, except that the TEST / VPP pin does not have pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C855. Data conversion tables must be set in two locations when using the 47P855V to check 47C655 operation.

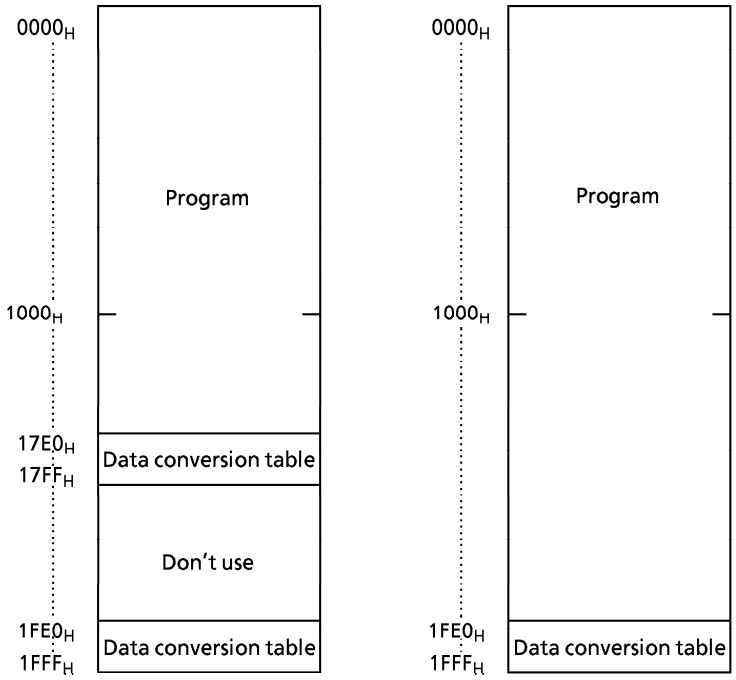


Figure 1-1. Program area

1.1.2 Data Memory

The 47P855V has 1024x4-bit data memory.
When using the 47P855V as a 47C655 evaluator, do not write data to address 80_H and following, even though the DMB1 addresses are 00-FF_H. There is no necessary to take into consideration a special function Shared area because one is built in DMB0.

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C655/855 except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the 47P855 is the same as I/O code WB of the 47C655/855.
External resistance, for example, is required when using as evaluator of other I/O codes (WE, WH) (Refer to Figure 1-2).

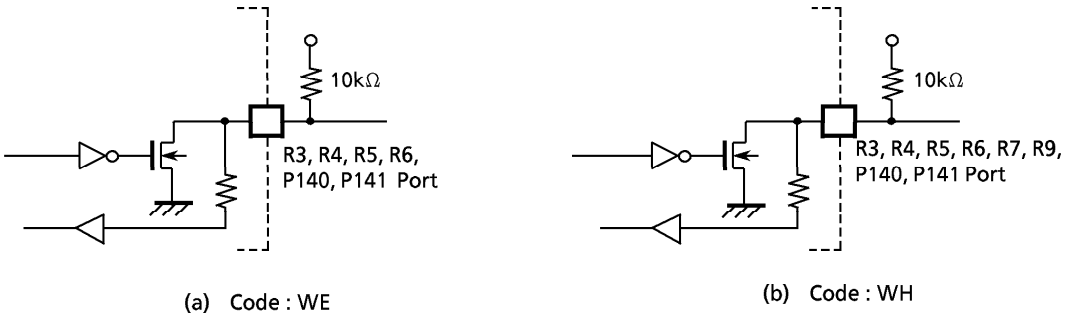


Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$ pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM2764AD).

An adapter socket (part No. BM1123) is available for connecting a PROM writer.

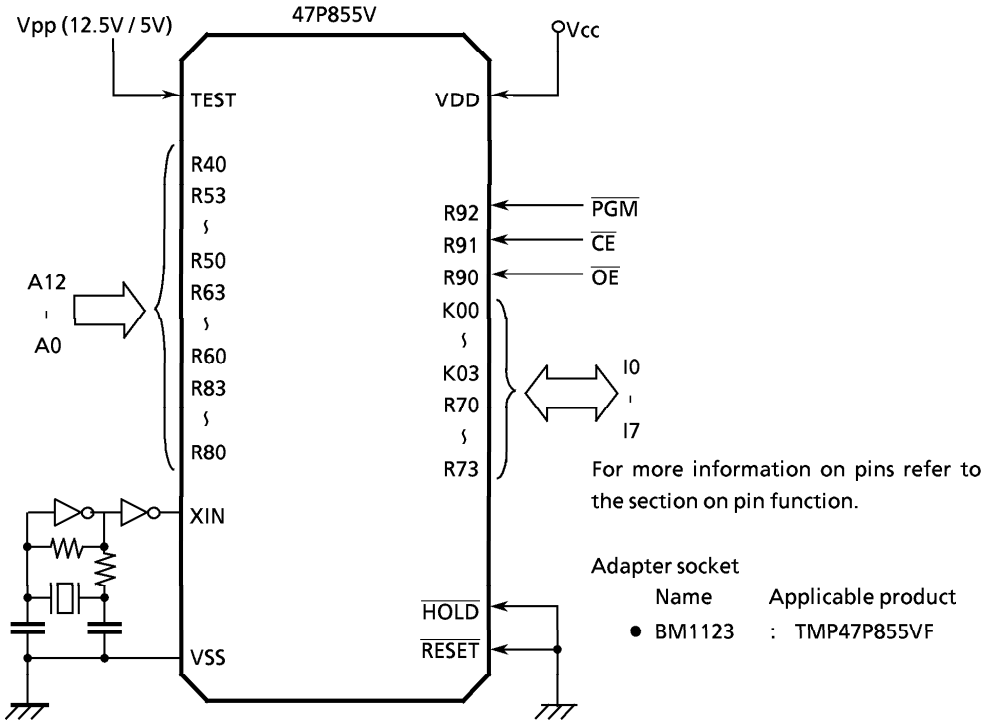


Figure 1-3. Setting for PROM mode

1.2.1 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (12.5V) is applied to the Vpp terminal with Vcc = 6V and $\overline{PGM} = V_{IH4}$. The programming is achieved by applying a Single TTL low level 1 ms, pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 msec is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 15 times). After correctly programming the selected address, one additional program pulse with pulse width 4 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.

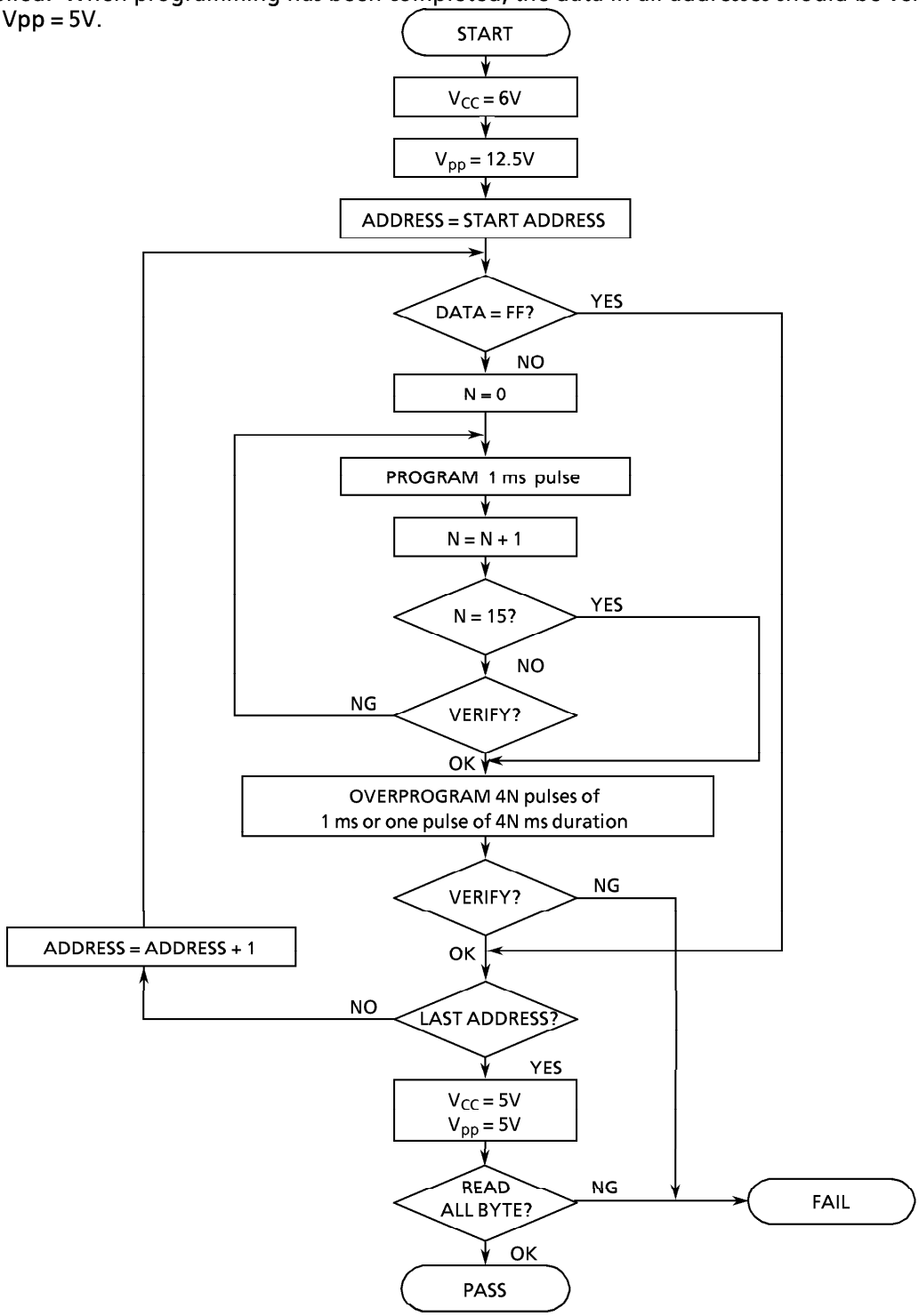


Figure1-4. FLOW CHART

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Program Voltage	V_{PP}	TEST/VPP pin	− 0.3 to 14.0	V
Supply Voltage (LCD drive)	V_{LC}		− 0.3 to V_{DD} + 0.3	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include R7, P142, P143	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except R7, P142, P143	− 0.3 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 70℃]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10s)	℃
Storage Temperature	T_{stg}		− 55 to 125	℃
Operating Temperature	T_{opr}		− 30 to 60	℃

Note. Characteristic of R7 is different from 47C855.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	2.2	6.0	V
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency (High freq.)	fc	XIN, XOUT		480 / 960		kH_Z
Clock Frequency (Low freq.)	fs	XTIN, XTOUT		30.0	34.0	kH_Z

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Low Level Input Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output Level High Voltage	V_{OH}	Ports R (push-pull)	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	—	—	V
Output Level Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	V
Segment Output Resistance	R_{OS}	SEG pin	V_{DD} = 5V, V_{DD} – V_{LC} = 3V	—	20	—	kΩ
Common Output Resistance	R_{OC}	COM pin					
Segment/Common Output Voltage	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Nomal mode)	I_{DD}		V_{DD} = 2.2V, V_{LC} = V_{SS} fc = 960kHz	—	0.6	1.2	mA
	I_{DDT}		V_{DD} = 2.2V, V_{LC} = V_{SS} fc = 960kHz When tone is oscillating	—	2.2	3.5	
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3V, V_{LC} = V_{SS} fs = 32.768kHz	—	15	30	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA
			V_{DD} = 2.2V, T_{OPR} = 25°C	—	—	0.5	

Note 1. Typ. values shows those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Output Resistance Ros, Roc : Shows on-resistance at the level switching.

Note 4. $V_{O2/3}$: Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.
$V_{O1/2}$: Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.
$V_{O1/3}$: Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5. Supply Current I_{DD} : V_{IN} = 2.0V/0.2V
The port K0 is open when the input resistor is contained.
The voltage applied to the port R is within the valid range.

Note 6. Supply Current I_{DDS} : V_{IN} = 2.8V/0.2V. Only low frequency clock is only osillated (connecting XTIN, XTOUT).

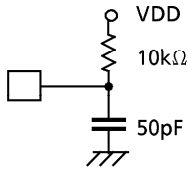
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

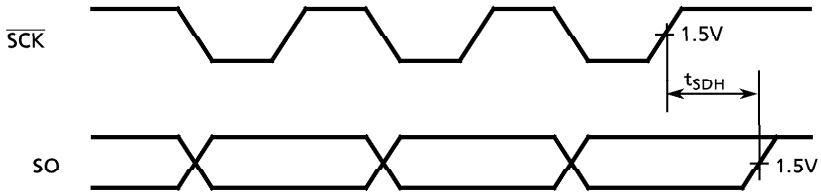
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	In the Normal mode	16.7 / 8.3			μs
		In the SLOW mode	235	—	267	
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	—	—	ns

Note. Shift Data Hold Time :

External Circuit for $\overline{SCK}$ pin and SO pin.



Serial port (completion of transmission)



TONE OUTPUT CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Tone Output Voltage (ROW)	V_{TONE}	RL ≧ 10kΩ, V_{DD} = 2.2V	125	185	250	mVrms
Pre-emphasis High Band (COL/ROW)	PEHB	PEHB = 20log (COL/ROW)	1	2	3	dB
Output Distortion	DIS		—	—	10	%
Frequency Stability	△f	Except error of osc. frequency	—	—	0.7	%

RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 2.2 to 6.0V, T_{opr} = – 30 to 60°C)

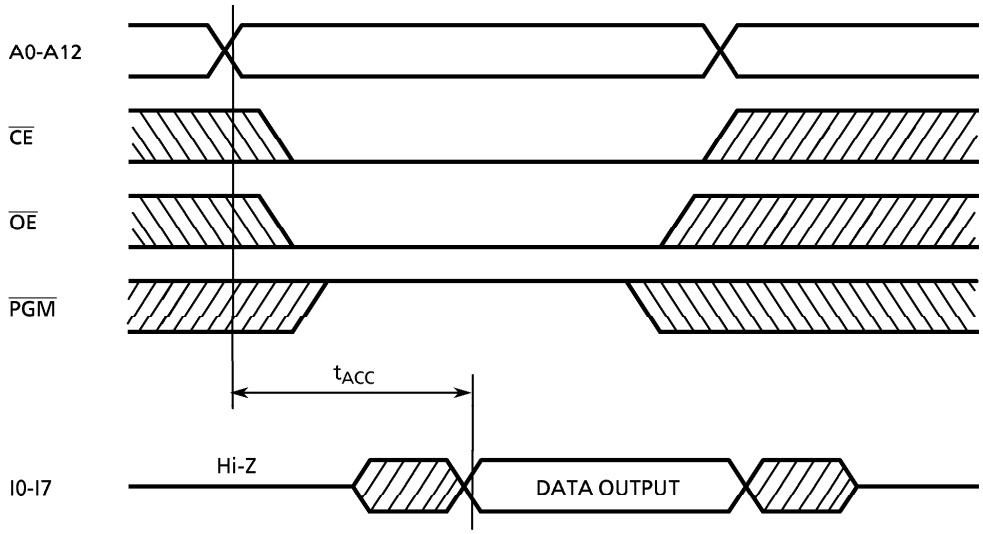
Recommended oscillating conditions of the 47P855V are equal to the 47C855's.

D.C./A.C. CHARACTERISTICS

(V_{SS} = 0V)

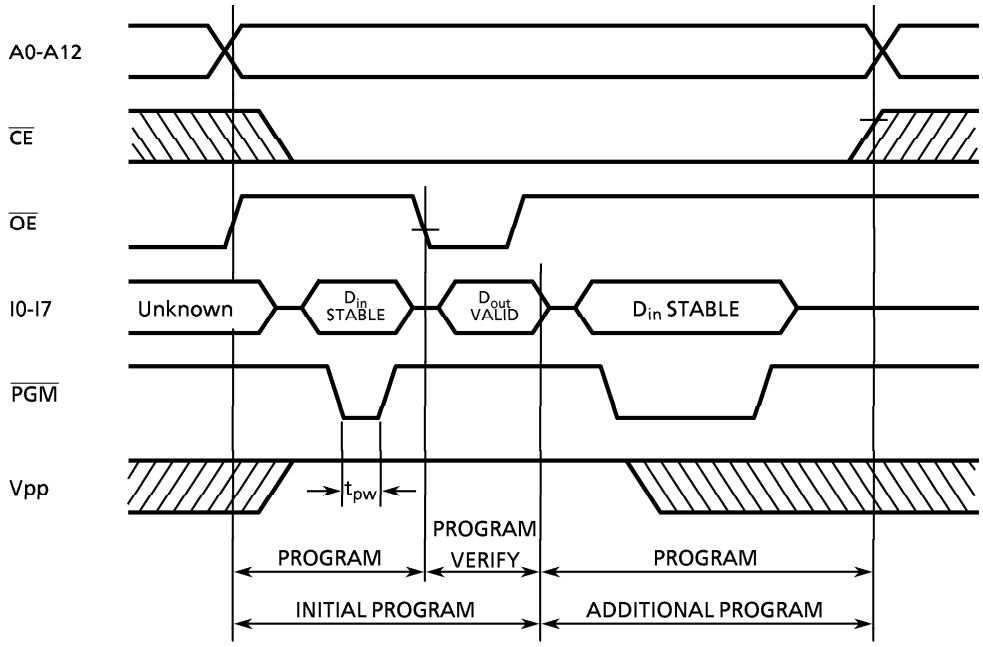
(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	0	–	350	ns



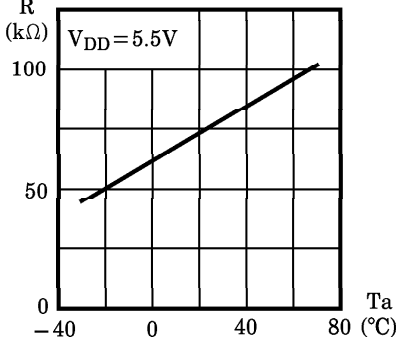
(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Programming Pulse Width	t_{PW}	V_{CC} = 6.0 ± 0.25V	0.95	1.0	1.05	ms

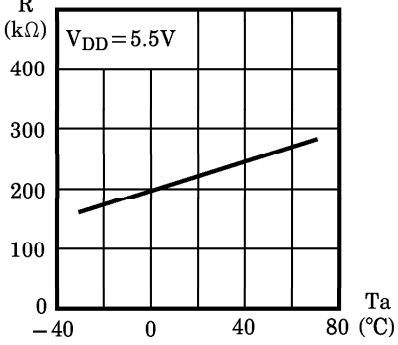


TYPICAL CHARACTERISTICS

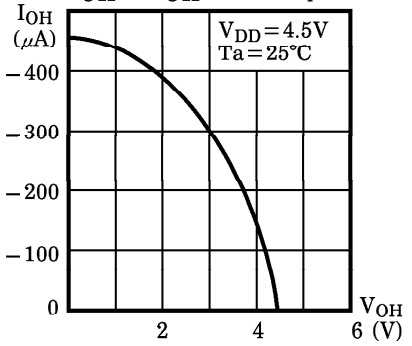
R – Ta K0 port



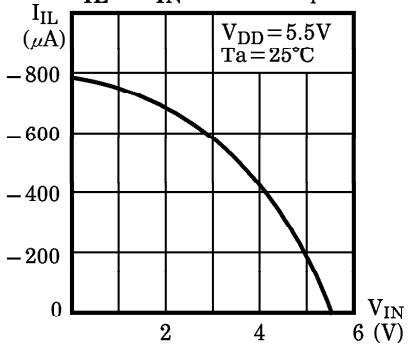
R – Ta $\overline{\text{RESET}}$ pin



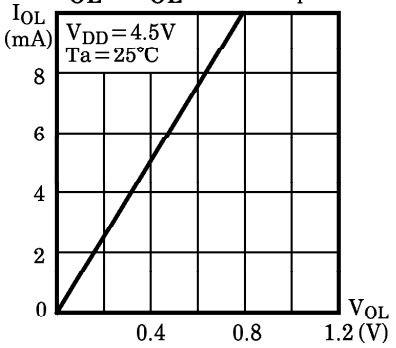
I_{OH} – V_{OH} CMOS R port



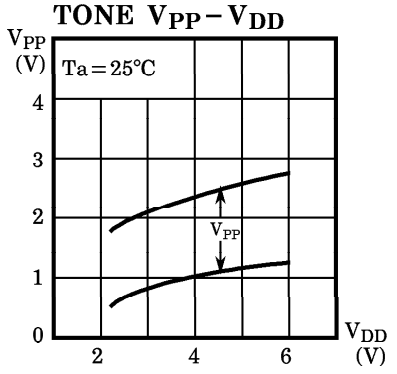
I_{IL} – V_{IN} CMOS R port



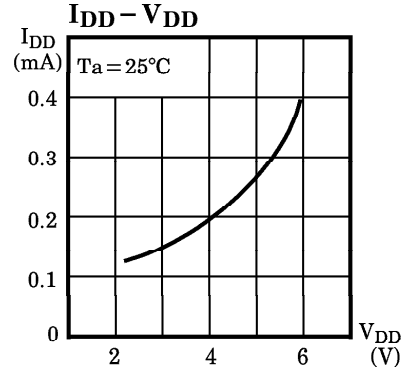
I_{OL} – V_{OL} R port



TONE V_{PP} – V_{DD}



I_{DD} – V_{DD}



I_{DDT} – V_{DD}