Winbond Electronics Corp.

DIRECT SEQUENCE SPREAD SPECTRUM TRANSCEIVER

GENERAL DESCRIPTION

The W9310 is a multi-purpose communication device designed to support either voice or data communication. For operation in voice mode, the W9310 provides all the baseband functions required for an FCC Part 15 compliant cordless phone and includes the signals required for interfacing to a 32 Kbps ADPCM codec. For operation in data mode, the W9310 supports both full-duplex and semi-duplex operations.

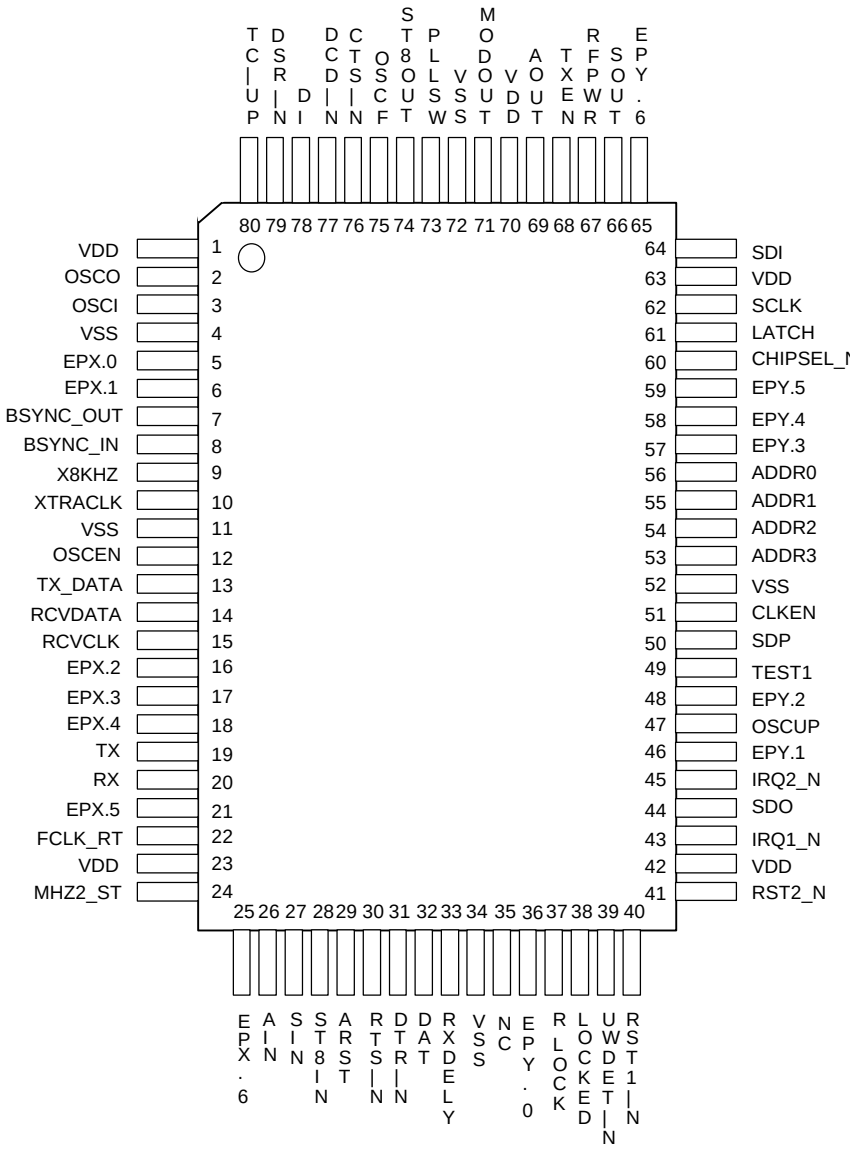
In voice mode and for full-duplex operation in data mode, communication is achieved using a time-division duplex (TDD), or ping-pong (PP), burst structure. In half-duplex data mode, no assumptions about the higher-level protocol are made. Instead, the W9310 is designed to be flexible and can be configured for a variety of requirements.

The modem engine itself is a synchronous data modem.The W9310 supports full-duplex data rates of up to 64 Kbps and half-duplex data rates of up to 160 Kbps. When operating as a cordless phone, the W9310 interfaces with a 32 Kbps ADPCM vocoder. The W9310 also includes a serial microprocessor/ microcontroller interface.

FEATURES

- Designed for spread spectrum wireless communication systems
- Voice mode:
  - 32 Kbps ADPCM
- Data Mode
  - Full-duplex data rate up to 64 Kbps
  - Half-duplex data rate up to 160 Kbps
- TDD switch control
- Serial bus interface
- Simplified FCC part 15 compliance
- Simple BPSK/MSK modulation
- CMOS technology
- Packaged in 80-pin PQFP

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN	I/O	FUNCTION
Power Supply Signals			
VDD	1, 23, 42, 63, 70	I	DC power supply.
VSS	4, 11, 34, 52, 72	I	Ground.
Oscillator and Clock Signals			
OSCI	3	I	Oscillator input. Input to the on-chip crystal oscillator. When a crystal is used, it should be connected across pins OSCI and OSCO. If a crystal clock oscillator or external clock source is used, then OSCI should be connected to the clock source and OSCO left open. The external clock source (or crystal clock oscillator) should have a 50 ±0.25% duty cycle and ±50 ppm accuracy.
OSCO	2	O	Oscillator output. Output from the on-chip crystal oscillator. Should be connected to one side of a crystal or left open if an external clock source or crystal clock oscillator is used.
OSCF	75	O	Buffered oscillator output. Inverted buffered output of the on-chip crystal oscillator output.
OSCEN	12	I	Oscillator enable. Enables the on-chip crystal oscillator when asserted; otherwise, the on-chip crystal oscillator is disabled.
OSCUP	47	O	Microprocessor clock. This is a clock signal generated internally from the master oscillator; it is the divide-by-4 version of the master oscillator. For example, when a 16.384 MHz master oscillator is used the OSCUP pin delivers a 4.096 MHz clock. The main purpose of OSCUP is to reduce the number of clock signals required for the system.
Voice/Data Port Signals The voice/data port signals can be divided into the following three categories: 1. General control – control signals that configures the W9310 2. Handshaking – modem interface signals in data mode 3. Data I/O – data input and output from the W9310			
General Control Signals			
DAT	32	I*	Data select. Selects data or voice operation. The W9310 operates in data mode when DAT is set to high (binary "1"), and in voice mode when it is low (binary "0"). Default condition is voice mode (pull-down on the input).

Pin Description, continued

SYMBOL	PIN	I/O	FUNCTION
SDP	50	I	Semi-duplex select. When set to high, selects half-duplex operation. When set to low, selects full-duplex operation. Valid only in data mode. Default condition is full-duplex mode (pull-down on the input).
RXD ELAY	33	I*	Receive data delay. When asserted, inserts an 8-bit delay between the time when DCD_N is asserted and when valid received data are delivered on RX pin (RX remains high until valid data are delivered). Otherwise, valid received data are available on the RX pin on the falling edge of FCLK_RT clock following DCD_N assertion.
Hand Shaking Signals (Note: these signals are not applicable in voice mode)			
RTS_N	30	I	Request to send. The terminal (DTE) asserts this signal when it has data to send. In the full-duplex mode, data are transmitted only after the W9310 asserts CTS in response to terminal RTS assertion (see CTS description below).When RTS is negated, the W9310 finishes transmitting the data already in the transmit FIFO and then transmits all high's. In half-duplex mode, the W9310 starts transmitting data as soon as $\overline{\text{RTS}}$ is asserted and stops immediately when $\overline{\text{RTS}}$ is negated.
CTS_N	76	O	Clear to send. after terminal (DTE) asserts RTS_N, the W9310 (DCE) asserts CTS_N when ready for data input from the DTE. In the full-duplex mode, CTS_N is asserted only after (1) RTS has been asserted, and (2) LOCKED condition has been achieved (the W9310 has detected the four UWs transmitted by the far-end W9310). $\overline{\text{CTS\_N}}$ is negated when RTS is negated or when the W9310 releases the lock. In the half-duplex mode, CTS_N follows RTS_N directly. In either half or full-duplex mode, once CTS_N is asserted, the W9310 expects valid data to be available on the TX line on the next rising edge of the transmit clock.

Pin Description, continued

SYMBOL	PIN	I/O	FUNCTION
DCD_N	77	O	Data carrier detected. Used by the W9310 to signal DTE that it has received valid data. In the full-duplex mode, DCD_N is asserted when the W9310 has achieved LOCK and stored received data in the RCVFIFO. It is negated when the link goes down or when RCVFIFO is empty. When DCD_N is negated, RX remains high. In half-duplex mode, DCD_N is asserted when the W9310 has locked onto the remote W9310 and is negated when the signal disappears. The time interval between W9310 achieving lock and DCD_N assertion and that between W9310 releasing lock and DCD_N negation are user-programmable through the microprocessor interface. In either mode, valid received data are available on the RX pin on the same falling edge of the FCLK_RT clock as DCD_N assertion.
DTR_N	31	I*	Data terminal relay. The W9310 will neither transmit nor receive data when DTR_N is negated.
DSR_N	79	O	Data set ready. In the full-duplex mode, the W9310 asserts this signal when LOCKED condition has been achieved. The W9310 negates DSR_N when the communication link is lost. In the half-duplex mode, DSR_N is asserted as soon as the W9310 is powered and enabled.
Data I/O			
TX	19	I	Transmit data. Data on the TX are transmitted by the W9310 when the DTR_N, DSR_N, RTS_N, and CTS_N signals are asserted; otherwise, TX remains high. Valid data should be available on the TX line before the rising edge of the MHZ2_ST transmit clock after CTS_N has been asserted. In voice mode, the TX pin accepts ADPCM sample input.
RX	20	O	Receive data. Outputs data from the W9310 to the DTE when DTR_N, DSR_N, and DCD_N signals asserted; otherwise, RX remains high. Depending on RXDELAY setting, valid data may be available on the RX pin on the same falling edge of the FCLK_RT clock as DCD_N assertion. In voice mode, the W9310 delivers received ADPCM samples on this pin.
Clock Signals			
MHZ2_ST	24	O	Transmit clock/Bit clock. In synchronous mode, MHZ2_ST is used to synchronously clock in the transmit data on the TX on the rising edge of the clock. Also known as ST or TXC. In voice mode, the MHZ2_ST pin delivers the 2.048 MHz bit rate clock signal to the ADPCM codec.

Pin Description, continued

SYMBOL	PIN	I/O	FUNCTION
FCLK_RT	22	O	Receive clock/Framing clock. In synchronous mode, FCLK_RT is used to synchronously clock out the received data on the RX on the falling edge of the clock. Also known as RT or RXC. In voice mode, the FCLK-RT pin delivers the 8 KHz framing clock to the ADPCM codec.
Transceiver Signals			
BSYNC-OUT	7	O	Burst synchronization output. Burst synchronization pulse. Can be used in a PBX environment, where several radios are co-located, to synchronize the burst timing, thereby reducing "near end" interference.
BSYNC_IN	8	I	Burst synchronization input. To be externally looped back to BSYNC_OUT or to an external burst timing source.
CLKEN	51	I	Clock enable. When negated, disables the internal clock generator circuit, thereby disabling the W9310 except for the OSCUP and the SBI circuit.
TX_DATA	13	O	Burst rate transmit data. Output of the TDD circuit to the transmitter logic. It is the burst-rate baseband transmit signal prior to spreading operation. Intended for use in testing only.
RCVDATA	14	O	Burst rate receive data. Output of the receive module. It is the burst-rate baseband receive clock. Intended for use in testing only.
RCVCLK	15	O	Recovered clock. Output of the received clock from the receiver module. It is the burst-rate receive clock. Intended for use in testing only.
RLOCK	37	O	Remote lock. When asserted, RLOCK indicates that the acquisition process has been completed. Refer to the operational section for details.
LOCKED	38	O	Locked signal. When asserted, LOCKED indicates that initial acquistion burst has been received. Refer to the operational section for details.
UWDET_N	39	O	Unique word detect. Active low signal that goes low whenever a valid UW has been detected.
RFPWR	67	O	RF power switch. Designed to switch transmitter on when asserted and off when de-asserted. Discussed in more detail in the operational section.
PLLSW	73	O	Phase-locked loop switch. Design to switch the transceiver synthesizer between TX and RX frequencies. It is asserted for TX and de-asserted for RX. See operational section for details.
TXEN	68	O	Transmitter enable. Designed to switch the antenna to the receiver and to switch the receiver on when low. When asserted, connects the antenna to the transmitter and switches the receiver off.

Pin Description, continued

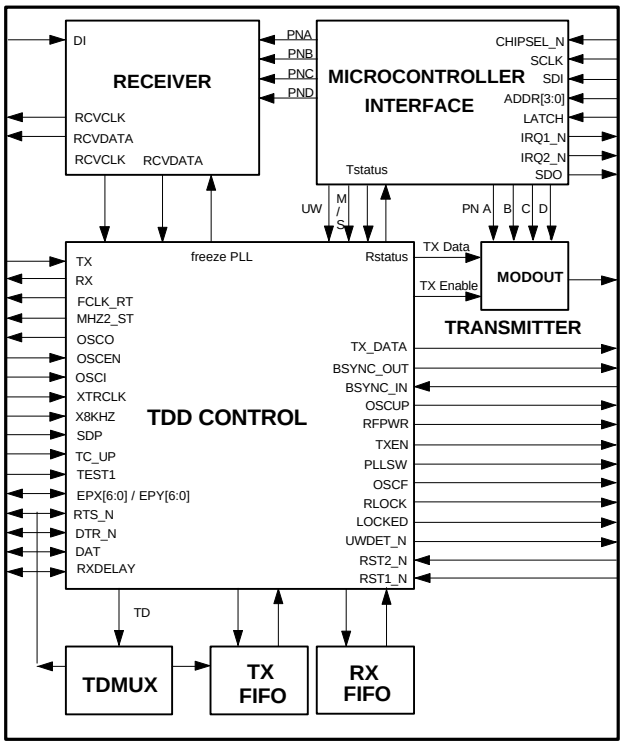
SYMBOL	PIN	I/O	FUNCTION
MODOUT	71	O	Modulation output. Spread spectrum modulated chip output. A tri-state output that is in high impedance when TXEN is low.
DI	78	I	Received data input. CMOS compatible input from analog receiver.
RST1_N	40	I	Reset 1. When low, resets the storage elements in the W9310 and freezes all clocks except the master oscillator.
RST2_N	41	I	Reset 2. Resets the entire W9310 except the SBI.
SBI Circuit Signals			
SDI	64	I	SBI data input. Used by the microprocessor to write data into the W9310.
SDO	44	O	SBI data output. Tri-state output pin. It is in high-impedance state unless CHIPSEL_N is low and ADDR is set to 0 or 1.
SCLK	62	I	SBI clock. Serial clock delivered to the W9310 by the microprocessor when reading or writing. When idle, it should be kept high.
LATCH	61	I	SBI latch. Latch signal used by the microprocessor to latch in the serial input data or to reset the interrupts
CHIPSEL_N	60	I	Chip select. When low, validates the address on the address bus. When high, the W9310 ignores all activity on the address bus.
ADDR[0:3]	56, 55, 54, 53	I	SBI address bus. MSB is bit 3, LSB is bit 0. Used to select the SBI register for reading or writing. When SBI is not being accessed, ADDR should be set to an unused address (for example, hex 15).
IRQ1_N	43	O	SBI Interrupt 1. Indicates that a status nibble is available for reading.
IRQ2_N	45	O	SBI Interrupt 2. Indicates that S/N data are available for reading.
Test Circuit Signals			
EPX[0:6]	5, 6, 16, 17, 18, 21, 25	I, O	Exponent X. When set as outputs, delivers the output of the correlators A & B (time multiplexed). When set as inputs, replaces correlators A & B as data source to acquisition section of the receive module. Bit 6 is MSB, bit 0 is LSB.
EPY[0:6]	36, 46, 57, 58, 59, 65	I, O	Exponent Y. When set to outputs, delivers the output of the correlators C & D (time multiplexed). When set to inputs, replaces correlators C & D as data source to acquisition section of the receive module. Bit 6 is MSB, bit 0 is LSB.
X8KHZ	9	I	Extra 8 KHz. External clock input for testing use.
XTRACLK	10	I	Extra clock. External clock input for testing use. It clocks the test counter among other modules.

Pin Description, continued

SYMBOL	PIN	I/O	FUNCTION
TC_UP	80	I	Test counter up/down control. When high, the test counter counts up; when low, the test counter counts down.
TEST1	49	I	Test 1 control. Places the W9310 in test mode when high. Must be set to low during normal operation.
AIN	26	I*	Test only. Must be set to LO during normal operation
SOUT	66	O	Test only
SIN	27	I*	Test only. Must be set to LO during normal operation
AOUT	69	O	Test only.
ST8IN	28	I*	Test only. Must be set to LO during normal operation
ST8OUT	74	O	Test only.
ARST	29	I*	Test only. Must be set to LO during normal operation

Note: An asterisk ("*") denotes pins that are bidirectional. These pins are configured as inputs in normal operation (TEST1 = 0) and as outputs during testing (TEST1 = 1).

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The W9310 is made up of six functional modules. These include the serial bus interface (SBI), the receiver, the transmitter, the time-division duplex (TDD) controller, the transmit and receive FIFOs, and the master clock generator. The SBI module supports bidirectional communication with a microprocessor such as the Winbond W921F880 or equivalent. The receiver module performs all the digital signal processing required by the spread spectrum receiver, including de-correlation and demodulation. The transmit module generates the spread spectrum binary sequence for output to an RF modulator. The TDD controller includes logic implementing the ping-pong protocol and various handshaking and interface signals. The transmit and receive FIFOs are used to buffer the transmit and receive data in full-duplex voice and data mode. The master clock generator generates clock signals required to drive the various modules of the W9310.

Each of these modules is described in more detail below.

SBI

The serial bus interface (SBI) allows the W9310 to communicate bidirectionally with a microprocessor. At power on, the W9310 receives programming information from the microprocessor. In TDD operation, the SBI can generate two interrupts, one for remote signaling by the microprocessor, the other for delivering the internally accumulated signal-to-noise (SN) measure to the microprocessor.

Receiver

The receiver samples the incoming baseband signals at two samples per PN chip. The samples are correlated with four possible PN sequences in 64-bit parallel correlators. The de-correlated signal is demodulated via a digital phase locked loop. The receiver is powered down while the W9310 is transmitting.

In addition, the receiver consumes peak power only during the brief period of the initial acquisition. After acquisition, the receiver goes into tracking/detection mode, and the power consumption of the receiver module is reduced by two orders of magnitude.

Transmitter

The transmitter logic encodes two consecutive bits of data into one of four possible 32-bit PN sequences. The PN sequences are programmed by the microprocessor through the SBI. The transmitted PN sequence is further randomized by modulus-2 addition with a 2047-bit PN sequence. This operation smoothes the output spectrum of the transmitted signal and eliminates discrete spectral components.

During ping-pong operation, to reduce power consumption, the transmitter remains idle when the W9310 is in receive mode. The transmitter outputs a tri-state buffer and is in high-impedance state during this idle time.

TDD Controller

The time-division duplex (TDD) controller implements the ping-pong protocol that allows a full-duplex link to be emulated by a half duplex radio. The TDD controller also generates appropriate clock and control signals to other modules of the W9310. In full-duplex mode, the TDD controller multiplexes and de-multiplexes the overhead bits with the real data. It also uses a digital locked loop to maintain an equal read and write rate to the FIFOs to prevent FIFO overflow or underflow. In addition, the TDD controller contains logic to generate the proper handshaking signals for both voice and data communication.

FIFOs

The W9310 includes a 30-byte transmit FIFO and a 30-byte receive FIFO to buffer the input and output data. The FIFO control is generated by the TDD controller. Note that during half-duplex data operation, the data are in flow-through mode and thus are not buffered by the FIFOs.

Master Clock Generator

The master clock generator generates the various clock signals required by the modules described above. It can be disabled to reduce power consumption.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}–V_{SS}	-0.3 to +6.5	V
Input/Output Voltage	V_{IL}	V_{SS} -0.5	V
	V_{IH}	V_{DD} +0.5	V
	V_{OL}	V_{SS} -0.5	V
	V_{OH}	V_{DD} +0.5	V
DC Current, Any Pin (except V_{DD} and V_{SS})	I	±10	mA
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to 150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

ELECTRICAL CHARACTERISTICS

I/O Characteristics

(V_{DD} = 5 V. T_A = 25° C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
"H" Input Current 1 (Note 1)	I_{IH1}	V_{IH} = 0.7 V_{DD}–V_{DD}	-275	-	-45	µA
"L" Input Current 1 (Note 1)	I_{IL1}	V_{SS} = V_{SS}–0.3 V_{DD}	-	-	40	µA
Pull-down Resistance	R_{PD}	-	-	11	-	KΩ
"H" Input Current 2 (Note 2)	I_{IH2}	V_{IH} = 0.7 V_{DD}–V_{SS}	-10	-	-	µA
"L" Input Current 2 (Note 2)	I_{IL2}	V_{IL} = V_{SS}–0.3 V_{DD}	-	-	10	µA
"H" Input Current 3 (Note 3)	I_{IH3}	V_{IH} = 0.7 V_{DD}–V_{DD}	-40	-	-	µA
"L" Input Current 3 (Note 3)	I_{IL3}	V_{IL} = V_{SS}–0.3 V_{DD}	45	-	290	µA
Pull-up Resistance	R_{PU}	-	-	18	-	KΩ

I/O Characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
"H" Output Current 1 (Note 4)	I_{OH1}	V_{OH} = 2.4V–V_{DD}	0	-	2	mA
"L" Output Current 1 (Note 4)	I_{OL1}	V_{OL} = V_{SS}–0.4V	-2	-	0	mA
"H" Output Current 2 (Note 5)	I_{OH2}	V_{OH} = 2.4V–V_{DD}	0	-	1	mA
"L" Output Current 2 (Note 5)	I_{OL2}	V_{OL} = V_{SS}–0.4V	-1	-	0	mA
"H" Output Current 3 (Note 6)	I_{OH3}	V_{OH} = 2.4V–V_{DD}	0	-	4	mA
"L" Output Current 3 (Note 6)	I_{OL3}	V_{OL} = V_{SS}–0.4V	-4	-	0	mA
Output Low Voltage	V_{OL}	-	0	-	0.4	V
Output High Voltage	V_{OH}	-	2.4	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V

Notes:

1. Pins 5, 6, 9, 10, 16, 17, 18, 21, 25, 32, 33, 36, 46, 48, 49, 50, 57, 58, 59, 65, and 80.
   Input buffer has pull-down resistor and will be at V_{SS} when left open.
2. Pins 3, 8, 19, 40, 41, 51, 52, 53, 54, 55, 56, 60, 61, 62, 64, and 78.
3. Pins 26, 27, 28, 29, 30, 31, and 79.
   Input buffer has pull-up resistor and will be at V_{DD} when left open.
4. Pin 2.
5. Pins 7, 13, 14, 15, 20, 22, 24, 26, 27, 28, 29, 30, 31, 37, 38, 39, 43, 45, 47, 66, 67, 68, 69, 74, 75, 76, 77, and 79.
6. Pins 44, 71, and 73.
   Output buffer is tri-state (pin 73 is not included).

OPERATIONAL DESCRIPTION

The operation of the W9310 in various operating modes is described below.

Full-duplex Operation

Although the W9310 actually uses only a simplex channel for communication with the remote device, full-duplex is provided by using the time-division duplex (TDD), or ping-pong (PP), protocol.

The TDD protocol configures the W9310 alternately as a transmitter and as a receiver. When two devices are communicating with each other, one is programmed to be the master, while the other is programmed to the slave. The TDD protocol ensures that while the master is transmitting, the slave is receiving and vice versa. The result is that as far as the user is concerned, the communication link is full-duplex. In order to achieve this, it is necessary for the W9310 to transmit at a higher rate than the actual user data rate. Ideally, for TDD operation, with 100% efficiency and 0% overhead, the W9310 must transmit the data at twice the user data rate since the W9310 has only half the time to transmit the user data (during the other half period, the W9310 is receiving from the remote station). Overhead such as the preamble unique word (UW) and other signaling information bits result in the W9310 transmitting at 2.6 times the user data rate. The size of the FIFOs on the W9310 is designed to provided sufficient buffer during both transmit and receive operations so that underflow or overflow of the FIFOs does not occur.

When communication between two devices first commences, the microprocessors program one of the devices as the master and the other device as the slave. The master device transmits periodic bursts as soon as the reset signal, RST2_N, is released. The burst timing of the master is derived from its internal master clock oscillator and can be computed from Eq. (1) below

$$f_{burst} = \frac{f_{mosc}}{192} \quad (1)$$

In Eq. (1), f_{burst} is the burst rate and f_{mosc} is the master oscillator frequency. For a voice device using the 32 Kbps ADPCM codec, the required master oscillator frequency is 16.384 MHz with a burst rate of 85.333 Kbps or a burst period of 11.719 μsec. Note that this burst rate is the actual bit rate at which the W9310 is transmitting during TDD operation, and 2.667 times the user bit rate (32 Kbps). As the transmitter uses a quadrature modulation scheme, the chip rate is 16 times the burst rate or

$$f_{chip} = \frac{f_{mosc}}{12} = 16 \times f_{burst} \quad (2)$$

where f_{chip} is the chip rate and f_{mosc} is the master oscillator frequency. The spread spectrum transceiver operates at 16 chips/bit or 32 chips/symbol, where each symbol is composed of 2 bits.

The total number of bits per burst is fixed and equal for the master and the slave. The slave derives its burst timing from the master by detecting the UW pulse transmitted by the master.

TDD (Ping-pong) Protocol

Initially, the two communicating devices need to establish "sync." The TDD protocol achieves this by using a special handshaking protocol. The master first transmits an acquisition burst containing 32 bits of preamble (binary 0's), followed by 226 bits of zeros stuffing and four 22-bit unique words (UW). When the slave receives the acquisition burst from the master correctly (by decoding the 4 consecutive UWs), it sends an acquisition burst in response. When the master receives the acquisition burst, it sends an "empty burst." An empty burst contains a 32-bit preamble followed by a single 22-bit unique word and 292 bits of "1" (one stuffing). In response to the master's empty burst, the slave also sends an empty burst back to the master. When the master receives the empty burst from the slave, the communication link is considered to have been established and the "sync" condition achieved. On the following burst, both the master and the slave start genuine data transmission by sending out data bursts. Each of the data bursts contains a 32-bit preamble, followed by a 22-bit UW, a 4-bit status nibble (ST), and 288 bits of user data (be it ADPCM voice samples or data). The three different types of burst frame structures are shown in Figure 1.

Preamble	Zero Stuffing	UW	UW	UW	UW

Acquisition Burst Frame Structure

Preamble	UW	One Stuffing

Empty Burst Frame Structure

Preamble	UW	ST	Data

Data Burst Frame Structure

FIELD	BITS

Preamble	32
Unique Word (UW)	22
Status Nibble (ST)	4
Data	288

Figure 1. Burst Frame Structures

Each actual burst cycle also includes two guard times to allow for both propagation and RF transceiver switching time. G_1 is 32-bit delay between the time when the master stops transmission and when the slave commences transmission; G_2 is a 32-bit delay between the time when the slave stops transmission and when the master commences transmission. These guard times allow for a 375 μS delay (for a master oscillator frequency of 16.384 MHz). The total burst cycle is 768 bits long, including a 12-bit internal delay (the transmitter turns off 6 bits after the last data bit is latched to the transmitter; the master and the slave therefore contribute a total of a 12-bit internal delay).

During the ping-pong operation, the receiver goes through several stages. Initially, when the 4 UWs of the acquisition burst have been received and decoded correctly, the receiver (either master or slave) declares "locked" (the LOCK signal output is asserted). After an empty burst has been decoded, the receiver declares "locked" (the RLCOK signal output is asserted), signifying that the remote device has locked. The behavior of the receiver after establishing the RLOCK condition depends on whether the internal state machine is turned on (determined by the setting of the configuration word, bit CI12). When the state machine is turned off, transmission will be turned off whenever the UW is not detected. The slave then waits for a new acquisition burst while the master will start the acquisition cycle again by transmitting an acquisition burst. Note that the master will continue to broadcast acquisition bursts until it has received a proper acquisition burst from the slave in response. The master will always revert back to the initial acquisition mode (broadcasting acquisition bursts), whenever it fails to detect the proper UWs from the slave.

If the state machine is turned on, then the receiver will not declare LOCK loss right after UW failed to be detected. Instead, it will allow for UW errors in up to two further bursts before declaring LOCK loss. The state diagram for this lock state machine is shown in Figure 2. In the figure, UW4DET indicates the condition when the four UWs have been detected during the acquisition burst, and UWDET indicates the condition where the single UW is empty and data bursts have been detected. M_SB is the programmed bit (CI8), which is a binary "1" when the W9310 is programmed to be the master and a binary "0" when it is programmed as a slave. NMODE is a signal generated by the receive logic and is asserted when the digital phase locked loop in the receiver has achieved lock. NMODE is similar to an RSSI signal. Note that the NMODE signal is independent of the UW detection. Physically, when NMODE is asserted, it indicates that PN acquisition has been achieved. The LOCKED and RLOCK states are as described above.

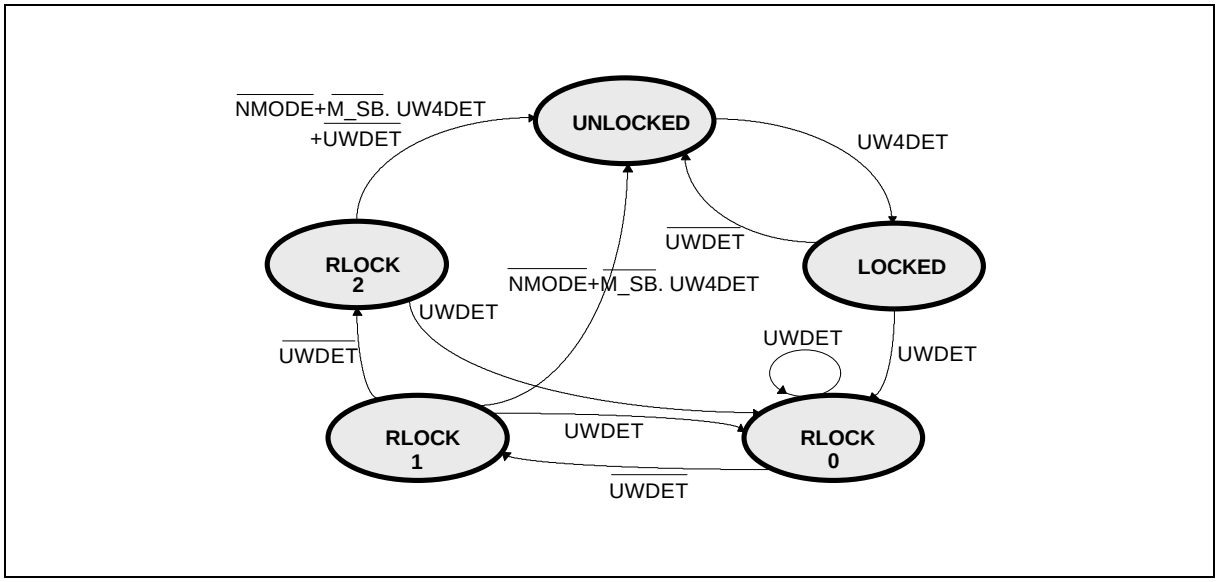


Figure 2. Receiver Lock State Machine

System Delay

To calculate the delay through the system (see Figure 3), assume that the transmit FIFO is almost empty at the end of a burst. Then the next bit that enters the transmit FIFO will experience a system delay (excluding propagation delay but including the internal logic delay) of approximately

$$T_{delay} = 2\times(T_G+T_{PR}+T_{UW}+T_{ST})+T_{DAT}+T_{\Delta} \quad (3)$$

where T_G is the time delay due to guard time (note that G = G1 = G2 = 32 bits), T_{PR} is the time delay due to the preamble, T_{UW} is the time delay of the UW, T_{ST} is the time delay for status nibble transmission, T_{DAT} is the time delay for data transmission, and T_{Δ} is the internal logic delay. For a 32 Kbps ADPCM voice signal, with a master oscillator (MO) of 16.384 MHz, this system delay translates into 5.625 mS, which is sufficiently short that no echo-canceller is required.

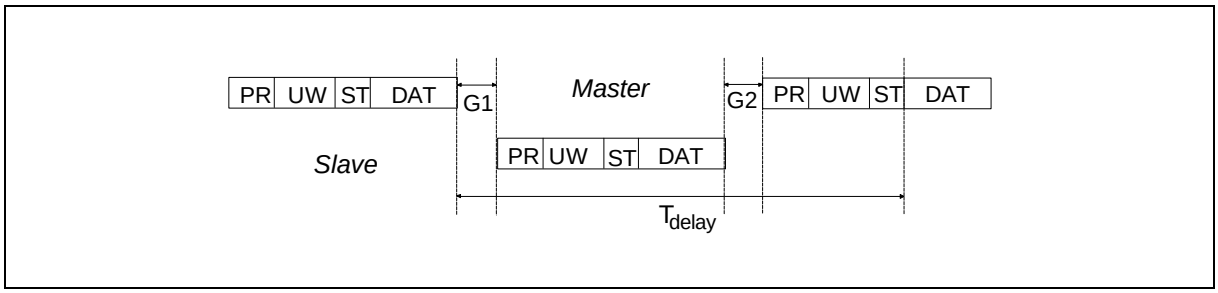


Figure 3. System Delay

Voice Mode Timing Information

For full-duplex voice mode operation, the W9310 generates the appropriate clock signals for interfacing with a 32-Kbps ADPCM voice codec such as the Winbond W9320S CCITT G.721 ADPCM codec. In particular, with an MO of 16.384 MHz, the MHz2_ST pin delivers the 2.048 MHz bit clock

and the FCLK_RT pin delivers the 8 KHz framing or sync clock to the ADPCM codec. The timing diagram for the ADPCM interface is shown in Figure 4 below. Details concerning the timing specifications are presented in the timing section.

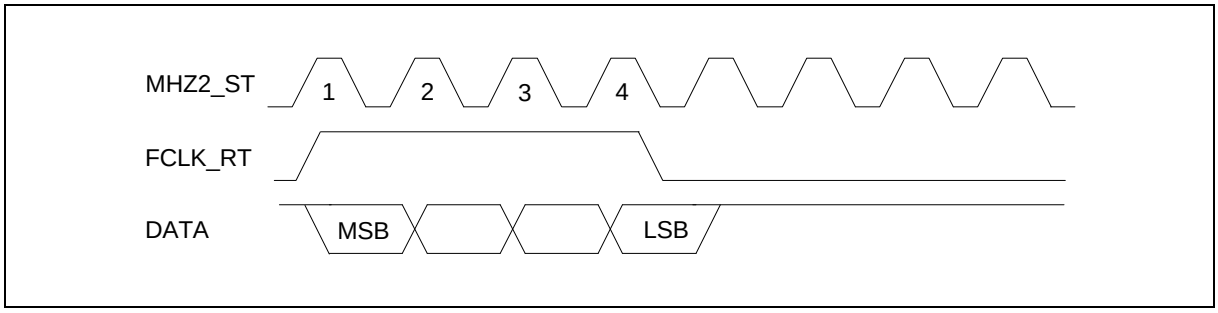


Figure 4. ADPCM Interface Timing

Data Mode Timing Information

When operating in the full-duplex data mode, the W9310 supports full-duplex data at rates up to 64 Kbps. For both voice and data mode full-duplex operation, it is necessary to lock the average rate of writing data into the FIFOs to the average rate of reading data from the FIFOs. Since the number of data bits per burst is fixed, as is the burst rate, this can be achieved by locking the sample clock onto the burst rate.

For voice mode operation, the 8 Kframes/sec clock is locked onto the burst rate by a digital phase-locked loop in the TDD control module. The phase-locked loop fine tunes the 8 Kframes/sec clock delivered to the ADPCM codec, so that exactly 72 frame pulses are delivered per burst. During each frame pulse, the ADPCM interface delivers and receives one nibble (4 bits) of data to and from the ADPCM codec.

For data mode operation, an MO of 32.768 MHz is required for a full-duplex data rate of 64 Kbps. Since the FIFOs are 8 bits wide, the framing clock for the 64 Kbps full-duplex data rate is 8 Kframes/sec. The PLL inside the TDD module adjusts the framing pulses so that exactly 36 frame pulses are delivered per burst. During each frame pulse, the FIFO delivers and receives 1-byte of data to an internal serial/parallel converter which receives and delivers the 1-bit serial data stream in a continuous fashion.

In either data or voice mode operation, when no data are available, the W9310 delivers a continuous binary "1" to the modulator and to the RX output.

For data mode, handshaking signals or modem control signals are fully implemented according to RS-232C documentation. Specifically, the user must assert both ready-to-send (RTS_N) and data-terminal-ready (DTR_N) signals before the W9310 will commence any data communication. Once both RTS_N and DTR_N have been asserted, the W9310 starts communicating with the remote W9310. After the preliminary acquisition process where the master and slave exchange acquisition and empty bursts, the W9310 asserts a clear-to-send (CTS_N) signal to indicate to the user that the W9310 is ready to accept data on the TX pin for transmission. Similarly, after the initial burst of actual data transmission (after CTS_N has been asserted), a data-carrier detect (DCD_N) signal is asserted to indicate to the user that valid data have been received and are available on the RX pin.

For synchronous communication, the W9310 provides the user both transmit and receive clock timing on MNZ2_ST (Send Timing) and KHZ8-RT (Receive Timing). During data transmission, the W9310 samples the TX pin data on the rising edge of the MHZ2_ST. Consequently, the user should supply the TX pin data in such a way that the transition data on the TX pin occur during the falling edge of

the MHZ2_ST clock signal. Similarly, the W9310 delivers the received data to RX on the falling edge of the FCLK_RT clock. This means that the RX data transition occurs on the falling edge of FCLK_RT and the user should use the rising edge of the FCLK_RT clock signal to latch the RX data. Both RTS_N and DCD_N transitions are synchronous with the appropriate clock edge (i.e., RTS_N changes on the rising edge of MHZ2_ST and CTS_N changes on the falling edge of FCLK_RT). After CTS_N assertion, the W9310 assumes that valid data will be available on the TX pin on the following rising edge of the MHZ2_ST. For this reason, the user is advised to hold the TX pin at a binary "1" prior to the first valid data bit. For the receive side, a special control pin, RXDELAY, can be used to set the timing between the DCD_N assertion and valid RX output.

When RXDELAY is set to a binary "0" (default condition), the W9310 starts delivering valid received data on the RX pin on the first falling edge after DCD_N assertion. When RXDELAY is set to a binary "1," the W9310 delivers valid RX output on the eighth falling edge after DCD_N assertion. Prior to valid RX output, the RX output is clamped at a binary "1."

The timing relationship between the data, clock, and handshaking signals is shown in Figure 5. Detailed timing specifications are presented in the timing section. A typical start-up of the data link is also shown in Figure 6; note that the same diagram would also apply for voice mode operation, with the exception that the handshaking signals are not applicable and the relationship between the MHZ2_ST and FCLK_RT timing is as shown in Figure 4 above.

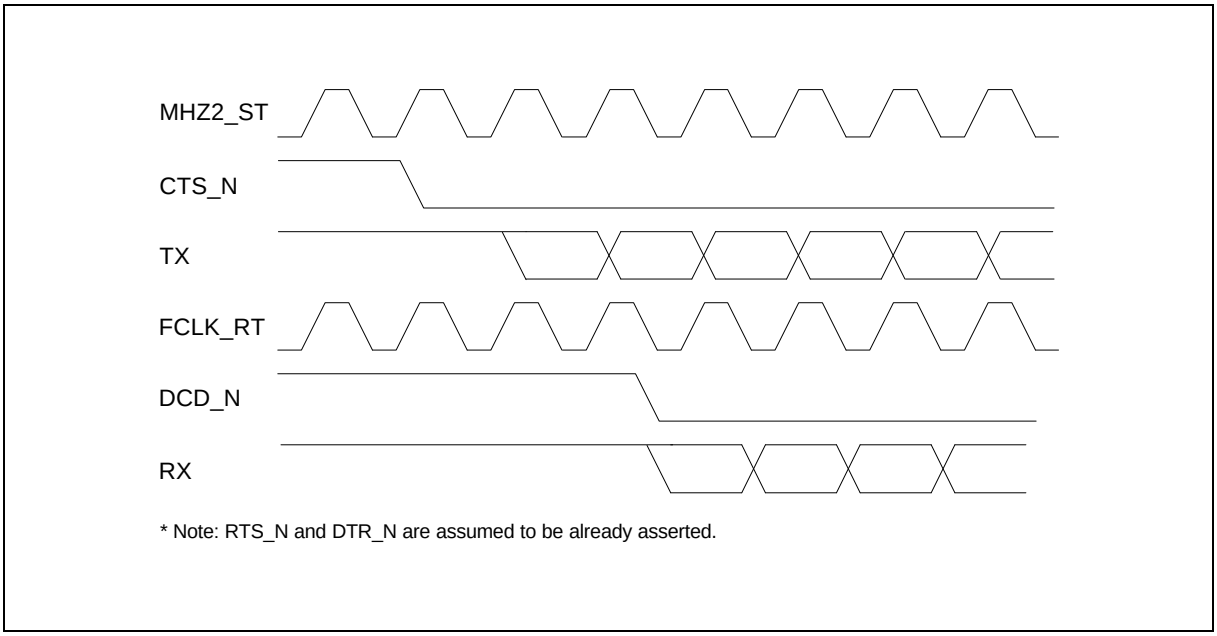
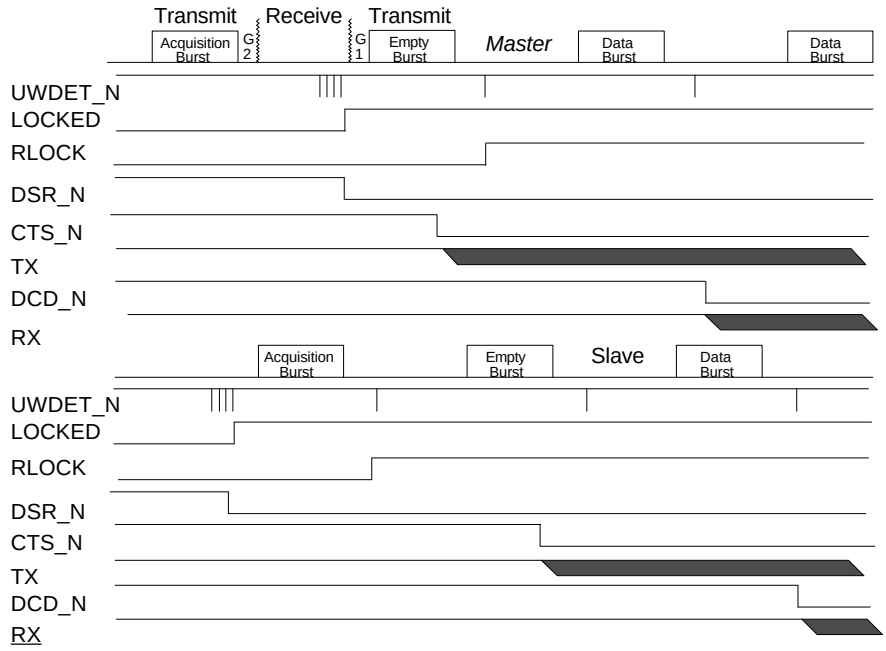


Figure 5. Full-duplex Data Interface Timing

Half-duplex Operation

The half-duplex data mode is suitable for applications such as packet radio. The W9310 does not make any assumptions about the higher-level protocol used; it relies on the higher-level protocol to provide the necessary framing, error correction, preamble, and so forth. The W9310 will transmit and deliver the data stream without multiplexing any special overhead bits, as in the case of full-duplex operation. It is the user's responsibility to ensure that each packet transmitted contains enough preamble bits so that acquisition can be achieved prior to actual data delivery. Similarly, although the W9310 delivers an equivalent DCD_N signal to the user, the user needs to be aware that invalid received data will be present at the output because of the hysteresis of the digital phase-locked loop. Thus the user must also be able to detect the end-of-packet from the data received rather than relying on the W9310 to signify loss of signal.



* Drawing not to scale and CTS_N and DTR_N assumed to be asserted.

Figure 6. Typical Communication Link Start-up

Because no overhead in multiplexing is required, in full duplex mode the highest data rate supportable is equivalent to the burst rate of the half-duplex mode. For the W9310, this is set at 160 Kbps using an MO of 30.72 MHz. The relationship between the data rate and the required MO is as follows:

$$f_{data} = \frac{f_{mosc}}{192} \quad (4)$$

The relationships between CTS_N and MHZ2_ST and that between DCD_N and FCLK_RT remain the same as in full-duplex operation. In typical half-duplex operation, the W9310 is assigned to be a transmitter or receiver, depending on the status of the RTS_N signal. When RTS_N is negated, the W9310 is configured as a receiver and will wait for a valid spread spectrum signal to arrive. When RTS_N is asserted, the W9310 is configured as a transmitter and starts transmitting right away. In the transmit mode, CTS_N follows RTS_N directly. Nominally, it will take approximately 60 bit-times for the receiver to complete the acquisition process and assert DCD_N. It is the user's responsibility to transmit enough preamble bits so that the receiver can acquire the remote signal prior to actual data transmission. Prior to DCD_N assertion, the RX output remains at binary "1." The transmitter stops transmission as soon as RTS_N is de-asserted. Because of the hysteresis of the digital phase-locked loop, however, the receiver will not de-assert the DCD_N signal until approximately 40-bit times after the signal has disappeared. It is up to the user to include and detect end-of-packet information so that invalid data are not erroneously perceived as valid data. Finally, note that there is no provision for CSMA/CD type avoidance in the hardware; it is up to the user or the modem system to implement any desired collision avoidance schemes either in hardware or software. A typical timing diagram for half-duplex operation is shown in Figure 7.

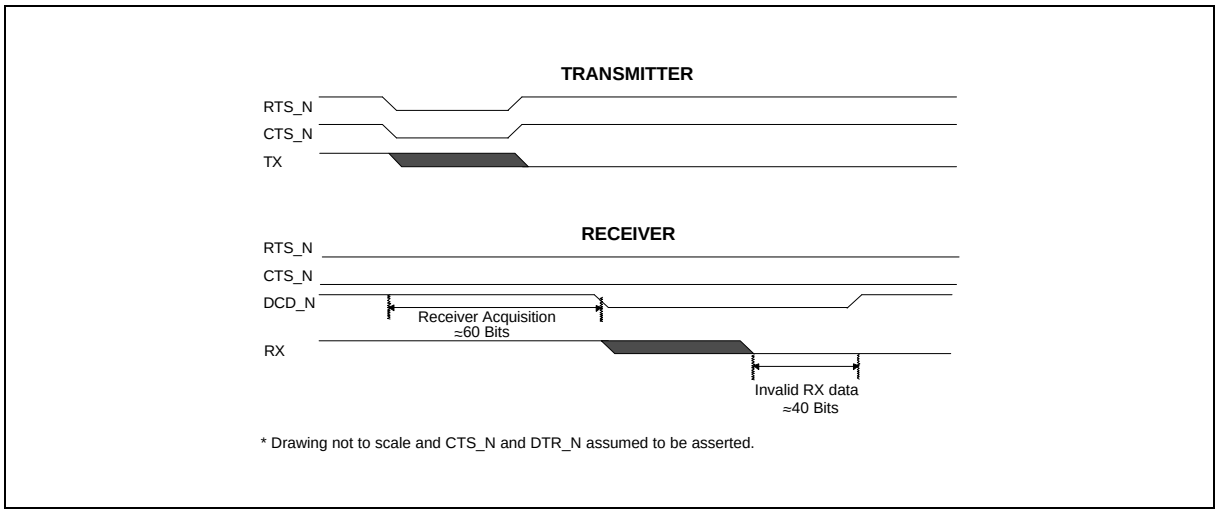


Figure 7. Timing for Half-duplex Operation

Note that there is a key difference between full-duplex and half-duplex operation. In full-duplex mode, when the W9310 is programmed as a master, it starts transmission as soon as DTR_N is asserted and reset RST2_N is released. As long as the master is powered on and DTR_N remains asserted, the W9310 will send out the acquisition burst and try to establish a communication link with a remote slave. Thus, the communication channel is occupied as soon as the master is powered on and DTR_N is asserted, and this can occur before any data become available for transmission. Once the communication link is established, even if there are no data to be transmitted, the master and slave will remain in communication with each other (sending out "1" in the data field) indefinitely or until the master is disabled. On the other hand, in half-duplex operation, there is no master or slave, and the W9310 will start transmitting only when it has data to send, which is indicated by the user asserting the RTS_N signal. By default, the W9310 will remain in the receive mode, and thus the communication channel will remain free until a user has data to transmit.

Programming the Serial Bus Interface

The serial bus is designed to interface with generic microprocessors such as the Winbond W921F880 or an equivalent product. It supports loading of the W9310 from the microprocessor and generates two interrupts for remote signaling and delivering S/N data. These operations are discussed in more detail below.

Serial Loading of W9310 Programmable Data

The microprocessor configures the W9310 by serially loading the W9310 with programmable information, including PN sequences, unique word, configuration information bits, and status nibble. The W9310 is loaded by means of the following steps:

1. The microprocessor sets the appropriate address for the intended register using the 4-bit ADDR line.
2. The microprocessor selects the W9310 by setting CHIPSEL_N to low.
3. The microprocessor puts the data on the SDI pin and toggles the SCLK clock the required number of clock cycles (note: 3 for Address 12 configuration bits loading, 8 for Address 13 status nibble loading and 5 for Address 14 testing bits loading. The remainding, from 2 to address 11, are 16 for SDI clocking into W9310). Note that the SDI data are clocked into the W9310 on the rising edge of the SCLK clock pulse and that loading is done MSB first (except for the configuration information bits; see Table 1.).
4. The microprocessor latches the serial data into the appropriate register by clocking the LATCH clock once.
5. The microprocessor sets the address to an unused address (for example, hex 15), and releases CHIPSEL_N.

Note: When the microprocessor programs the address 2 to 12 and 14 for W9310, It must first assert (HIGH) the RST1_N and de_assert (LOW) RST2_N of W9310 and then performs the procedures as above. But for address 13, both RST1_N and RST2_N are set HIGH first.

An example of the serial loading timing is shown in Figure 8.

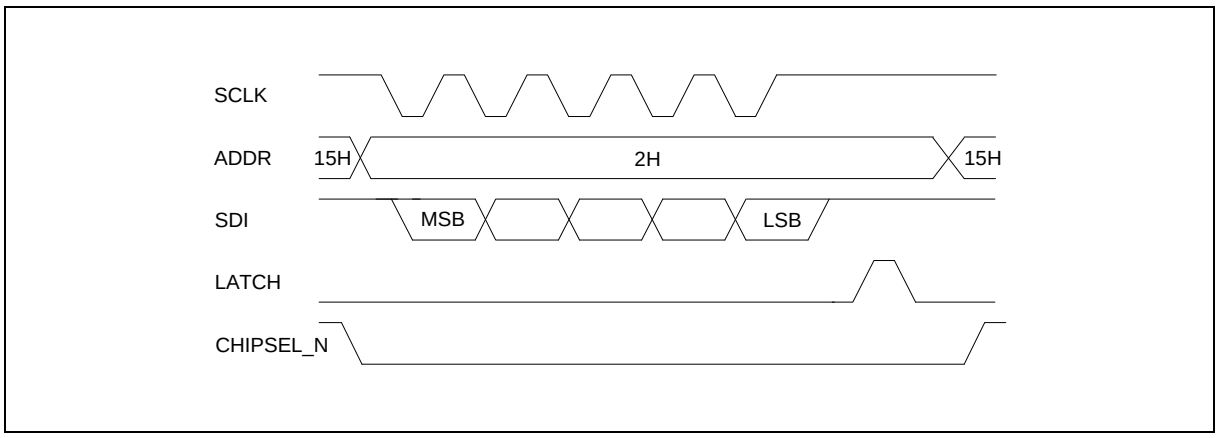


Figure 8. Timing for Serial Bus Loading

Reading the Status Nibble and S/N Data from SBI

The status nibble (TXSTAT) and S/N register data are updated periodically by the W9310. Once a status nibble or an S/N value has been loaded onto the register by the W9310, interrupts IRQ1_N or IRQ2_N are asserted. Once an interrupt has been asserted, no new data will be loaded onto the register until the interrupt has been serviced and cleared by the microprocessor. The status nibble is updated once every burst (if IRQ1_N is serviced every burst). The S/N data are calculated from the AGC circuit inside the W9310 once every 128 data bits (including overhead bits).

To read the status nibble and the S/N value, the following actions need to performed:

1. The microprocessor sets the address of the register to be read (0 for status nibble, 1 for S/N data) on the ADDR pins.
2. The microprocessor selects the W9310 by asserting the CHIPSEL_N pin.
3. The microprocessor clocks the SCLK pin the appropriate number of clock cycles (4 for status nibble, and 8 for S/N data). The status nibble or the S/N data byte is clocked out serially on the SDO pin.

   The data (from MSB to LSB) are clocked out of the W9310 on the falling edge of the SCLK clock.
4. The microprocessor clears the appropriate interrupt by toggling the LATCH signal once.
5. The microprocessor sets the address of the register to an unused address and releases CHIPSEL_N signal.

An example of the interrupt service timing is shown in Figure 9.

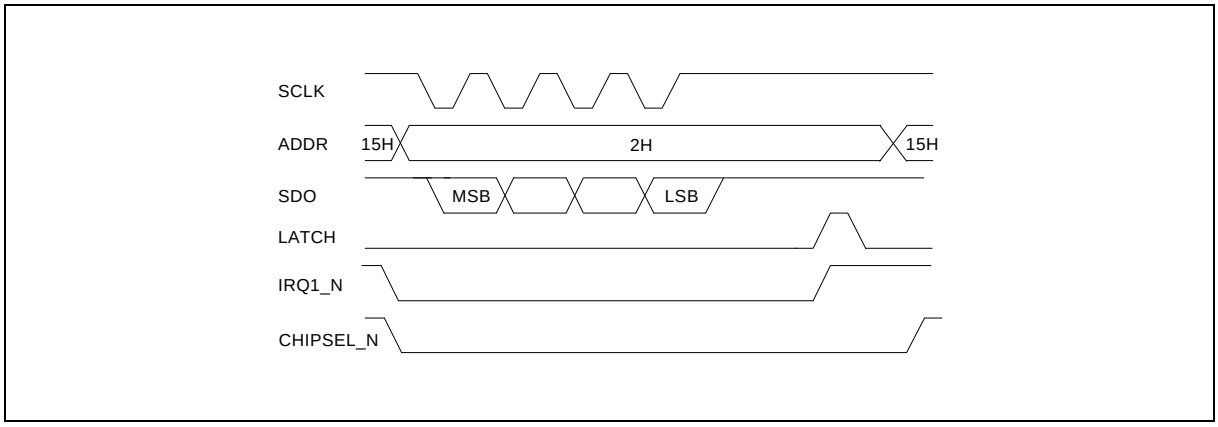


Figure 9. Interrupt Service Timing

Note that the SDO pin is a tri-state output pin and will remain in high impedance state until either address 0 or 1 is selected and CHIPSEL_N is asserted. Also note that the SBI are not affected by the reset signals, the only exception being status nibble, which cannot be loaded when the reset signal, RST2_N, is asserted.

SBI Registers

A total of fifteen registers are available for storing programming information through the SBI. These registers are listed below:

ADDRESS	DESCRIPTION
0	Read TXSTAT nibble register/Reset IRQ1_N
1	Read S/N register (one byte)/Reset IRQ2_N
2	Load upper 16 bits of PN sequence A
3	Load lower 16 bits of PN sequence A
4	Load upper 16 bits of PN sequence B
5	Load lower 16 bits of PN sequence B
6	Load upper 16 bits of PN sequence C
7	Load lower 16 bits of PN sequence C
8	Load upper 16 bits of PN sequence D
9	Load lower 16 bits of PN sequence D
10	Load upper 16 bits of UW
11	Load lower 6 bits of UW, followed by lower 10 bits of configuration information bits (CI0 leading, CI9 trailing)
12	Load upper 3 bits of configuration information bits (CI10 first, CI12 last).
13	Load TXSTAT nibble
14	Load test bits

Address	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
0	RST3	RST2	RST1	RST0												
1	SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0								
2	PNA31	PNA30	PNA29	PNA28	PNA27	PNA26	PNA25	PNA24	PNA23	PNA22	PNA21	PNA20	PNA19	PNA18	PNA17	PNA16
3	PNA15	PNA14	PNA13	PNA12	PNA11	PNA10	PNA9	PNA8	PNA7	PNA6	PNA5	PNA4	PNA3	PNA2	PNA1	PNA0
4	PNB1	PNB30	PNB29	PNB28	PNB27	PNB26	PNB25	PNB24	PNB23	PNB22	PNB21	PNB20	PNB19	PNB18	PNB17	PNB16
5	PNB5	PNB14	PNB13	PNB12	PNB11	PNB10	PNB9	PNB8	PNB7	PNB6	PNB5	PNB4	PNB3	PNB2	PNB1	PNC0
6	PNC31	PNC30	PNC29	PNC28	PNC27	PNC26	PNC25	PNC24	PNC23	PNC22	PNC21	PNC20	PNC19	PNC18	PNC17	PNC16
7	PNC15	PNC14	PNC13	PNC12	PNC11	PNC10	PNC9	PNC8	PNC7	PNC6	PNC5	PNC4	PNC3	PNC2	PNC1	PNC0
8	PND31	PND30	PND29	PND28	PND27	PND26	PND25	PND24	PND23	PND22	PND21	PND20	PND19	PND18	PND17	PND16
9	PND15	PND14	PND13	PND12	PND11	PND10	PND9	PND8	PND7	PND6	PND5	PND4	PND3	PND2	PND1	PND0
10	UW21	UW20	UW19	UW18	UW17	UW16	UW15	UW14	UW13	UW12	UW11	UW10	UW9	UW8	UW7	UW6
11	UW5	UW4	UW3	UW2	UW1	UW0	CI0	CI1	CI2	CI3	CI4	CI5	CI6	CI7	CI8	CI9
12	CI10	CI11	CI12													
13	TST3	TST2	TST1	TST0	0	0	0	0								
14	TEST4	TEST3	TEST2	TEST1	TEST0											

Table 1. SBI Registers

Configuration Information Bits

The configuration information bits are used to set various programmable parameters in the W9310:

CI0 Set W9310 to normal (low) or test (high) mode. Should be set to low during normal operation.

CI1 Test TDD (ping-pong) circuits when set to high. Set to low during normal operation.

CI2, 3 PLSL. Sets the width of the ESD window. CI2 is LSB, CI3 is MSB.

PLSL	WIDTH OF ESD WINDOW
0	8 samples wide
1	10 samples wide
2	12 samples wide
3	14 samples wide

CI4 CNTLR. Sets the width of the "Central Region." (Note: CNTLR size must be ≤ PLSL size).

CNTLR	WIDTH OF CENTRAL REGION
0	10 samples wide
1	12 samples wide

CI5 ACC1RES. DPLL Accumulator 1 reset.

ACC1RES	ACCUMULATOR 1 RESET
0	ACC1 NOT reset.
1	Reset ACC1.

CI6, 7 WSL. Sets the width of the "Detection Window." CI6 is LSB, CI7 is MSB.

WSL	WIDTH OF DETECTION WINDOW
0	4 samples wide
1	6 samples wide
2	8 samples wide
3	10 samples wide

CI8 M/SB. Set the W9310 to be a master (high) or slave (low).
Note: CI8 must be set to low in half-duplex data mode.

CI9. 0, 11 T. Number of errors allowed in the UW. CI9 is LSB, CI11 is MSB.

T	ALLOWABLE UW ERRORS
0	0 bit

Continued

1	1 bit
2	2 bits
3	3 bits
4–7	4 bits

CI12 LockSMon. Enables Locking State Machine when set to high (see Figure 2 for Locking State Machine state diagram).

Test Bits

The test bits (5 bits) are used to internally program several multiplexers for use during testing. During normal operation, they should be set to 0.

Reset and Disable Controls

The W9310 contains two clock enable and three reset control signals. The enable signals, OSCEN and CLKEN, are used to enable the master clock oscillator and the internal clock generator, respectively. When OSCEN is set to low, the on-chip clock oscillator will be disabled and consequently the W9310 will be disabled also. When CLKEN is set low, the internal clock generator is disabled, thus disabling most of the W9310's functions. However, the OSCUP clock output and the SBI module are not affected by the CLKEN signal. This allows the SBI to function even when the W9310 is disabled by the CLKEN signal. The three reset signals, ARST, RST1_N, and RST2_N, are used to reset various parts of the W9310. When set to low, the ARST signal resets the asynchronous/synchronous converter. In addition, when set to low, the ARST signal also disables the ST8OUT clock. If the asynchronous/synchronous converter is not used, the ARST signal should be set low so that the synchronous/synchronous converter is completely disabled and will not consume any power. When set to low, the RST1_N reset signal resets storage elements in the W9310 and disables all clocks except the master oscillator. The RST2_N reset signal resets the storage elements and disables all clocks except those of the master oscillator and the SBI.

RF/IF Analog Interface

The W9310 interfaces with the RF/IF analog radio through the DI, MODOUT, PLLSW, and RFPWR pins. DI is a CMOS-level input fed by the analog receiver. MODOUT is a tri-state output to the analog transmitter. It is in high-impedance state when the W9310 is in the receive mode (TXEN is low). PLLSW is used to switch the PLL of the analog radio and RFPWR is used to power the transmitter power amplifiers on and off. The timing for PLLSW and that for RFPWR are shown in Figure 10 and Figure 11, respectively. Note that the RFPWR timing is valid for both full-duplex and half-duplex modes. The PLLSW timing shown is for the full-duplex mode; for half-duplex operation, the PLLSW timing follows that of RFPWR. The BURST_CLK shown in Figure 10 is the burst rate clock, which is 2.667 times the data rate in full-duplex operation and is equal to the data rate in half-duplex operation. For example, for a master oscillator of 16.384 MHz, the full-duplex burst rate is 85.333 KHz. Thus, the RFPWR signal will be asserted one burst clock cycle or 11.72 µsec after TXEN assertion and will be de-asserted one burst clock cycle or 11.72 µS prior to TXEN de-assertion.

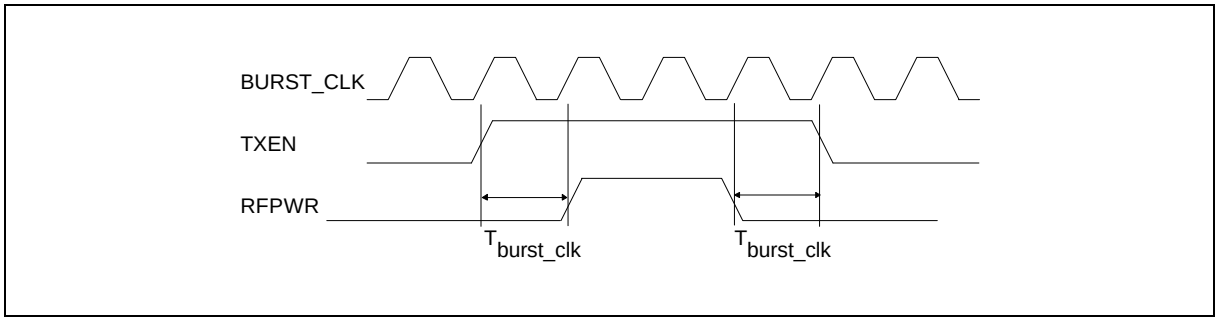


Figure 10. RFPWR Timing

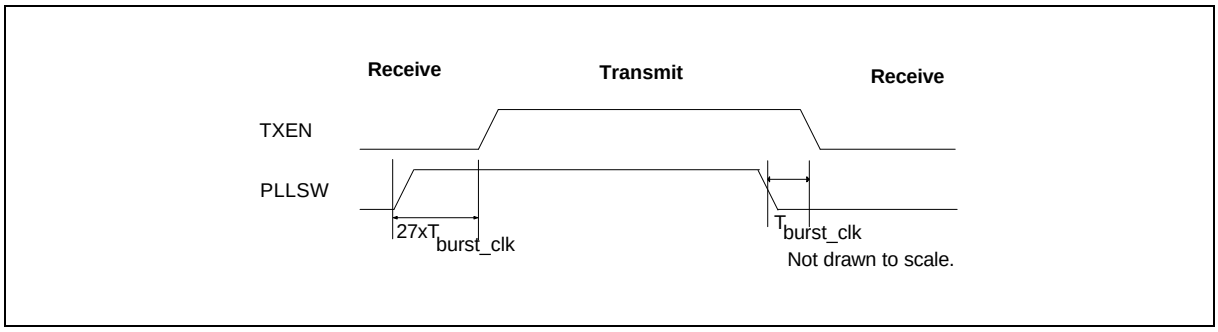
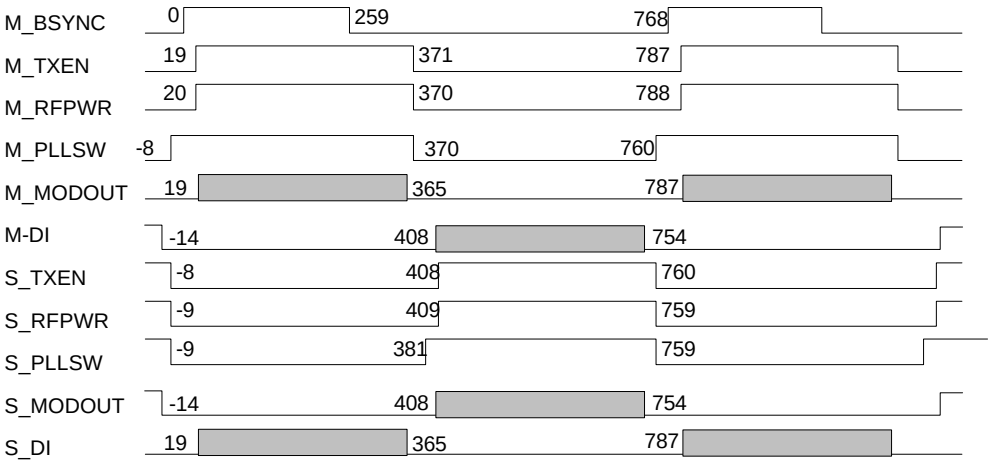


Figure 11. PLLSW Timing (Full-duplex Mode)

The PLLSW is asserted 27 burst clock cycles(duration of G1) prior to TXEN assertion and is de-asserted 1 burst clock cycle prior to when TXEN is de-asserted. Thus, for a master oscillator of 16.384 MHz (corresponding to a burst rate of 85.333 KHz or a burst period of 11.72 μS), the PLLSW signal will be asserted 316.44 μS (27*11.72 = 316.44) prior to TXEN assertion.

The RFPWR switch timing is designed to avoid damage to the sensitive analog receiver. When switching from receive to transmit, RFPWR is delayed relative to TXEN (which can be used for switching the antenna between transmit and receive chain) to ensure that the receiver has been turned off before the transmitter is turned on. Similarly, when switching from transmit to receive, RFPWR is turned off before TXEN to allow for extra time for the transmitter to turn off prior to turning on the receiver circuits.

The PLLSW signal is designed to switch the RF PLL when different frequencies are used for transmit and receive operations. In this instance, PLLSW is turned on at the end of receive operation and prior to TXEN assertion to allow the RF PLL to stabilize. Similarly, the PLLSW changes to a low as soon as transmission is finished and before reception commences.



Notes:
1. The timing is expressed as numbers of bits
2. The total number bits of per burst is fixed and equal for master and slave
3. The timing is assumed that there is no air propagation delay between master and slave

Test Circuits

The W9310 includes two multiplexers intended primarily for factory testing. The W9310 can be placed in test mode by setting the TEST1 pin high and the CI0 bit high. In the test mode, the two muxes, one 16 × 6 and the other 2 × 8, are used to observe the content of a set of registers. The 16 × 6 MUX is controlled by a 4-bit counter which can be incremented or decremented through the use of XTRACLK clock and TC_UP (test counter up/down control) inputs. The 2 × 8 MUX is controlled by the LSB bit of the test counter.

To reduce pin count, the test MUX pins are multiplexed with normal functional pins as shown in Table 2 and Table 3. For the 2 × 8 MUX, bit-directional buffers are used; during test mode, they are configured as output pins, while during normal operation, they are configured as input pins. In the test mode, the master oscillator can be frozen and the XTRACLK clock activated to scan the content of internal storage elements. Alternatively, the master oscillator can run normally while the TESTCLK is frozen so the output of the test muxes can be observed over time.

In addition to the XTRACLK, an additional test-only clock, X8KHZ, can be used to clock sub-modules of the W9310 at a higher than normal clock rate (by bypassing the normal internal clock) during testing.

Finally, two 7-bit bi-directional buses, EPX and EPY, are used for receiver testing. When set to output mode, the two buses allow the correlator outputs to be observed. In the input mode, the correlators are bypassed and external data can be applied through the EPX and EPY pins to test the remainder of the receiver logic independent of the correlator.

TEST PIN	NORMAL PIN
TOMUX.0	SOUT
TOMUX.1	AOUT
TOMUX.2	ST8OUT
TOMUX.3	CTS_N
TOMUX.4	DCD_N
TOMUX.5	DSR_N

Table 2. 16 × 6 Test MUX Multiplexed Pins

TEST PIN	NORMAL PIN
TOREC.0	AIN
TOREC.1	SIN
TOREC.2	ST8IN
TOREC.3	ARST
TOREC.4	RTS_N
TOREC.5	DTR_N
TOREC.6	DAT
TOREC.7	RXDELAY

Table 3. 2 × 8 Test MUX Multiplexed Pins

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN.	NOM.	MAX.	UNIT
DC Supply Voltage	V_{DD}	3.5	5.00	5.25	V
Power Dissipation	P_{DIS}	55	75	100	mW
Master Oscillator	F_{OSC}	-	5–40	96*	MHz
Frequency Tolerence	F_{TOL}	-	-	50	ppm
Clock Duty Cycle	F_{DUT}	40	50	60	%
Clock Rising Time	T_R	-	50	-	nS
Clock Falling Time	T_F	-	50	-	nS

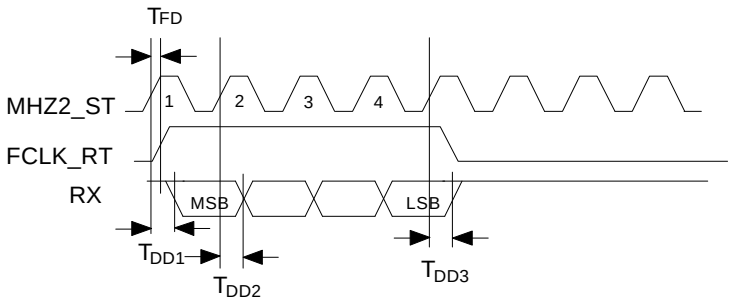
Table 4. Recommended Operating Conditions

* Denotes estimated value.

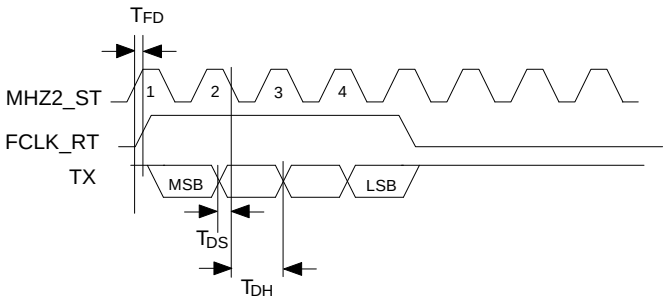
AC CHARACTERISTICS

A. 32 Kbps ADPCM Interface Timing

1. Transmit Side



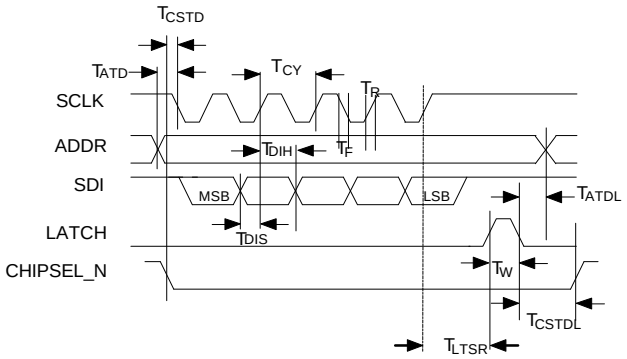
2. Receive Side



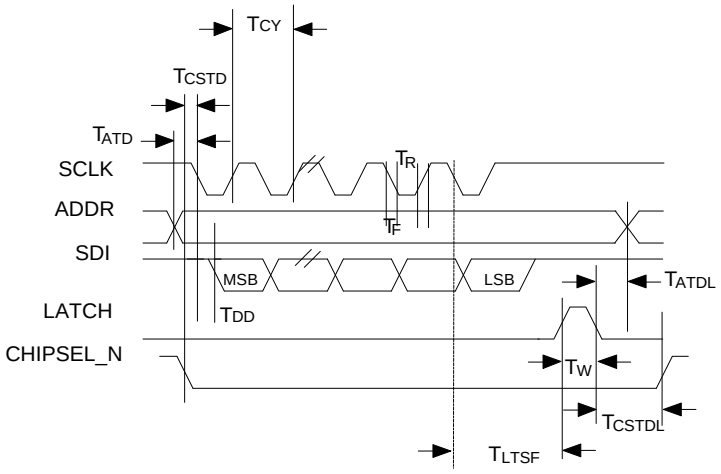
PARAMETER	SYMBOL	MIN.	TYPICAL	MAX.	UNIT
Sync Clock Frequency, (FCLK_RF)	FFCLK	-	8	-	KHz
Bit Clock Frequency	FMHZ2	-	2.048	-	MHz
Clock Duty Ratio	Dc	-	50	-	%
Digital Output Delay	TDD1, TDD2, TDD3	10	-	100	nS
Data Set Time	TDS	50	-	-	nS
Data Hold Time	TDH	50	-	-	nS
Frame Delay to Clock	TFD	0	-	50	nS

B. SBI Bus Interface Timing

1. Timing for Serial Bus Loading



2. Timing for Serial Bus Interrupt Service



PARAMETER	SYMBOL	MIN.	TYPICAL	MAX.	UNIT
ADDR Time Delay to SCLK	TATD	TCY	-	-	nS
CHIPSEL_N Time Delay to SCLK	TCSTD	TCY	-	-	nS
SCLK Rising Time	TR	-	-	50	nS
SCLK Falling Time	TF	-	-	50	nS
SCLK Clock Frequency	FSCLK = 1/TCY	-	-	1	MHz

Continued

LATCH Pulse Width	TW	-	-	100	nS
ADDR Time Delay to LATCH	TATDL	Tcy	-	-	nS
CHIPSEL_N Time Delay to LATCH	TCSTDL	Tcy	-	-	nS
SDI to SCLK Setup Time	TDIS	50	-	-	nS
SDI to SCLK Hold Time	TDIH	50	-	-	nS
SDO Output Delay to SCLK	TDD	-	-	200	nS
LATCH Time Delay to SCLK (rising edge)	TLTSR	2 TCY	-	-	nS
LATCH Time Delay to SCLK (falling edge)	TLTSF	2 TCY	-	-	nS

SYSTEM PERFORMANCE

A significant number of the system performance parameters depend heavily on the RF/Analog circuits. The information presented here therefore represents onlyt an estimate of these parameters.

PARAMETER	ESTIMATED PERFORMANCE
Oscillator Stability	Depends primarily on the analog circuit but <15 ppm over terperature range and aging (for 1 dB sensitivity degration) should be achievable
Acquisition Time	<100 bits average <200 bits for 99.9% probability of acquisition at S/N of 2 dB (applies for first burst only)
Interference Immunity in Channel (±1.365 MHz)	-6 dB J/S worst case CW Jammer to Signal power ratio
Sensitivity in White Noise (Semi-duplex mode)	19 dB E_b/N_0 for BER = 10^{-5} 17.5 dB E_b/N_0 for BER = 10^{-4} 16.5 dB E_b/N_0 for BER = 10^{-3}
Estimated Current (Power) Consumption (5 Volt operation)	25 mA (125 mW) in acquisition mode. 18 mA (90 mW) average in ping-pong mode. 13 mA (65 mW) in transmit mode. (MO = 16.384 MHz)

APPLICATION INFORMATION

In this section, several issues concerning the application of the W9310 are discussed.

Notes on Half-duplex Operation

In the half-duplex mode, because of the hysteresis of the digital PLL, the DCD_N signal is not de-asserted right away. On average, it takes from 21 to 30 symbols (or 42 to 60 bits) before DCD_N is de-asserted. During this time, the W9310 will deliver random data on the RX pin. The receiver will not declare lock (asserting DCD_N) until the initial acquisition process has been completed. This process typically takes from 60-110 bits depending on the condition of the radio link. It is imperative, therefore, for the packet to carry framing information so that the beginning and end of the packet can be detected (for example, a high-speed synchronous data link protocol such as HDLC provides its own framing structure in the packets it transmitted). In addition, sufficient preamble bits must be transmitted prior to actual data transmission so that the receiver will be locked and ready to deliver data when actual data arrive.

Selecting the Master Oscillator Frequency

A complete clock generator has been included on the W9310 to reduce the system clocking requirement. Nominally, only a single crystal or clock oscillator is required for powering the entire W9310. The required crystal or clock oscillator frequency is dependent on the data rate and in general can be calculated from the following equations:

$$f_{osc} = 2048 \times f_{frame} = 8 \times f_{bclk} \quad \text{for full-duplex voice}$$
$$f_{osc} = 512 \times f_{data} \quad \text{for full-duplex data} \qquad (5)$$
$$f_{osc} = 192 \times f_{data} \quad \text{for half-duplex data}$$

Where f_{osc} is the master oscillator frequency, f_{frame} is the framing clock of the ADPCM codec, f_{bclk} is bit-rate clock of the ADPCM codec, and f_{data} is the data rate. For example, for a 32 Kbps ADPCM voice, f_{frame} = 8 KHz, f_{bclk} = 2.048 MHz, and the required f_{osc} is 16.384 MHz. For 64 Kbps full-duplex data, f_{data} = 64 Kbps and the required master oscillator frequency is 32.768 MHz. For 160 Kbps half-duplex data, f_{data} = 160 Kbps and the required master oscillator frequency is 30.72 MHz.

Programming the W9310

This section briefly discusses how to program the W9310 for various operating modes. First, loading of PN sequences A, B, C, and D is required for operation in all modes. These are loaded from MSB to LSB. For full-duplex operation, the 22-bit UW is loaded into the SBI from MSB to LSB. The CI bits must be loaded for any operating mode. Note that the loading order of the CI bits is the *opposite* of that for the PN and UW sequences, which are loaded from LSB to MSB. The CI bits configure the various programmable parameters in the receiver. In general, for normal operation, CI0 and CI1 must be set to low.

The programming of PLSL, CNTLR, ACC1RES, and WSL depends on several environmental and system-related factors. For example, the size of the PLSL and CNTLR windows affects the dynamic performance of the PLL. In general, if a smaller window size is used, the PLL will behave as if it has a smaller loop bandwidth with higher noise filtering but at the expense of slower dynamic response. If a larger window size is used, the PLL will respond quicker dynamically but its performance will be degraded because more noise is allowed to enter the system. *Note that the width of the central zone must be smaller than or equal to the size of the ESD window* (this means that the ESD window size must not be set to 8, a value included for testing purposes only). Similarly, the width of the detection

window, WSL, should be large enough to take advantage of multipath combining but should not be so large that excessive noise is allowed into the receiver, thus causing the sensitivity of the receiver to degrade. In general, these parameters can be optimized for a particular environment through experimental trial and error. Otherwise, it is recommended that these parameters be programmed to values in the middle of the programmable range (for example, set PLSL to 12 samples wide, CNTLR to 10 samples wide, and WSL to 8 samples wide). In the full-duplex or ping-pong mode, ACCRST1 should normally be set to "0" for no ACC1 reset during each "freeze PLL" period. The only instance where ACCRST1 should be set "1" to reset ACC1 is if the frequency offset between the transmitter and receiver is known to be very small. In this case, the performance of the PLL will be slightly enhanced if ACC1 is reset during each "freeze PLL" period. In half-duplex operation. ACC1RES should be set to "1" to always reset ACC1.

CI8 is used to set the W9310 to be either a master or a slave. Typically, in a cordless phone application, the unit that initiates the signaling process (either the handheld or the base station) should be programmed to be the master. Thus, when dialing into the PSTN, the handheld unit is configured to be the master. When a phone call is received, on the other hand, the base station is configured as the master. Note that for half-duplex operation, CI8 *must* be set to low (e.g., as a slave). There is no master or slave in half-duplex operation. Instead, the W9310 enters transmit mode when RTS_N is asserted and stays in receive mode otherwise. The number of allowable errors in UW depends on the application. For example, applications that can tolerate a larger BER can usually allow more UW errors while still maintaining a reasonable communication link, as is the case with voice applications. Finally, CI12 enables or disables the locking state machine. When used in conjunction with the programmable allowable UW errors, the locking state machine gives the system designer the flexibility to tailor the W9310 for a particular operating environment. Typically, if the locking state machine is enabled and more UW errors allowed, the W9310 will continue to operate normally even in a marginal communication link channel without repeatedly loosing the lock and going into acquisition. The disadvantage of this strategy is the corresponding increase in data errors, which might be intolerable in some critical applications. In this case, the number of allowable UW errors can be reduced and the locking state machine turned off.

Sample System Block Diagram

Sample system block diagrams for cordless phone and data modem applications are shown below. In addition, a sample MSK RF/analog front-end for the W9310 is also presented.

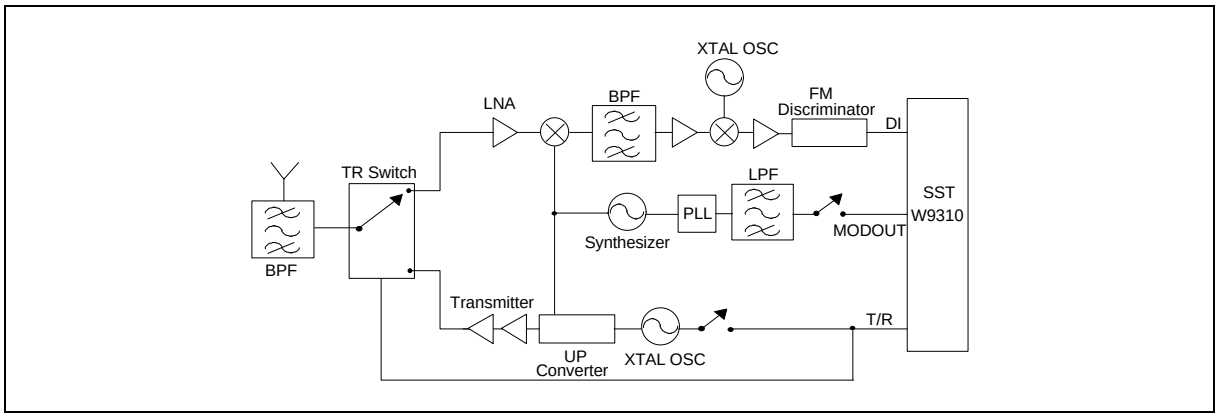


Figure 12. Sample MSK Radio RF/Analog Front End

Note: In Figure 12, T/R is taken as a combination of the PLLSW, RFPWR, and TXEN signals, depending on the requirements of the analog/RF circuit.

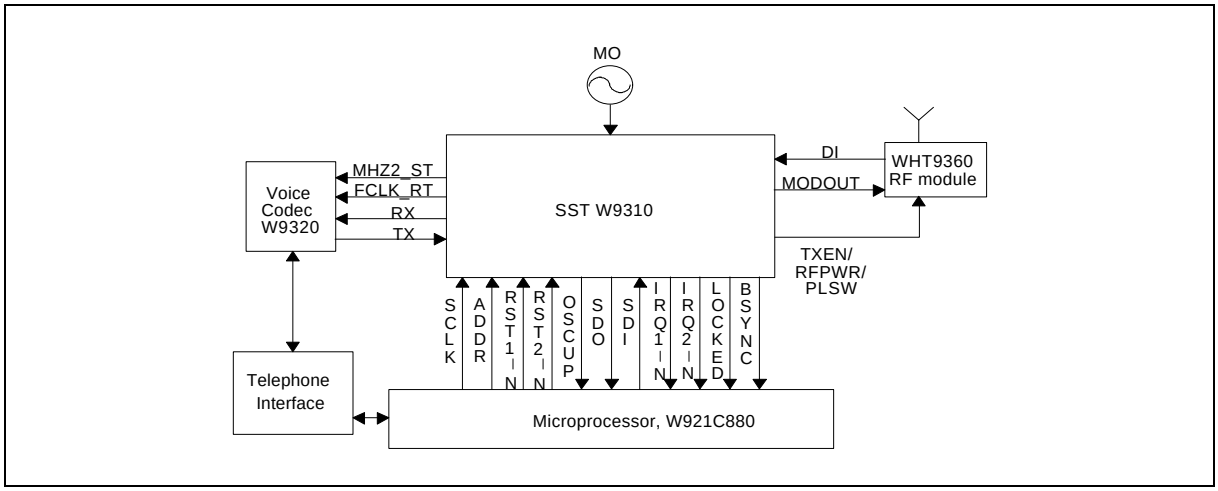


Figure 13. Sample Block Diagram for a Cordless Phone System

In Figure 13, a simple cordless phone system block diagram is shown. Note that the setup in the base station will be slightly different than that for the handset. For simplicity, only a generic block diagram is shown.

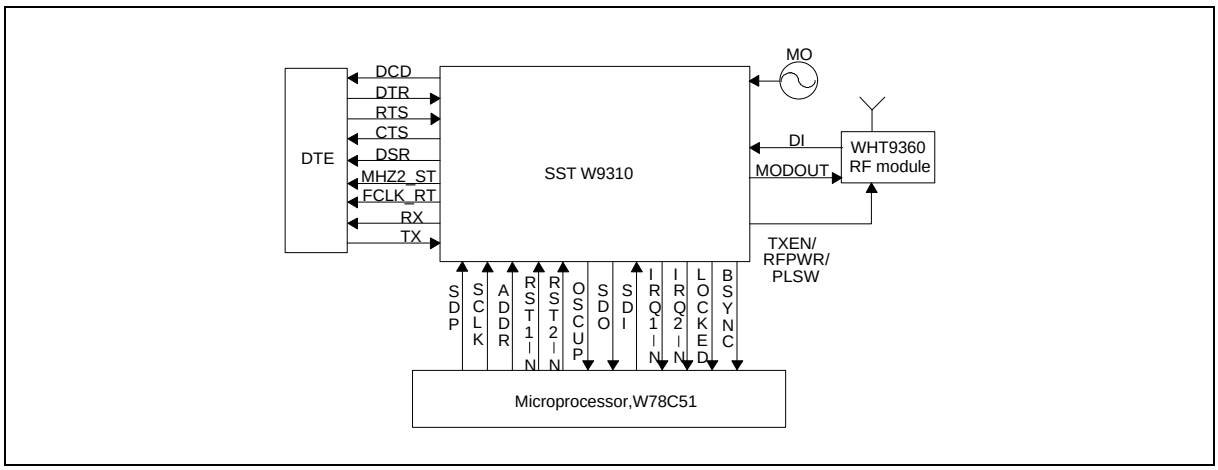


Figure 14. Sample Block Diagram for a Data Modem

In Figure 14, a sample block diagram for a data modem is shown. Note that the block diagram shown is for a synchronous data modem; for an asynchronous data modem, a external rate adaption circuitry is required to converter the asynchronous rate to synchronous rate.

PN SEQUENCE AND UW SELECTION

Four 32-bit PN (Pseudo Noise) sequences and one 22-bit Unique Word (UW) are required for each spread spectrum communication device. Together, they can constitute a "security code" or "identification code" which can be use to distinguish different users and ensure privacy. In addition, the PN sequences and UW participate in the signal acquisition and burst synchronization processes.

To ensure good system performance, the PN sequences and UW must be selected with care. Guidelines for choosing the PN sequences and UW are presented below.

PN Sequence Selection

The four PN sequences are used to represent a di-bit symbol in the W9310. To ensure the transmitted symbol is decoded correctly at the receiver, follow the principles below when choosing the four PN sequences.

1. The four PN sequences should be orthogonal to each other. Two PN sequences A and B are orthogonal to each other if

$$\sum_{i=0}^{31} a_i . b_i = 0 \tag{6}$$

where PN sequence A = [A_{31}, A_{30}, A_{29}, ..., A_1, A_0], a_1 = -1 for A_i = 0, and a_i = 1 for A_i = 1. A similar relation holds for B.

2. The PN sequences should be even, i.e., each sequence should have the same number of zeros and ones.

3. The PN sequences should not have more than four consecutive identical bits.

With the three criteria outlined above, it is possible to generate a large set of valid PN sequences. Two additional and optional criteria can be used to further identify PN sequences for reduced self- and cross-interference.

1. The auto-correlation side lobes of the PN sequences should be at least 4 less than the auto-correlation of the main lobe.

2. The cross-correlation of PN sequences between sets (one set being the four orthogonal PN sequences for one spread spectrum W9310) should also be at least 4 less than the auto-correlation of the main lobe.

UW Selection

The UW is used in the receiver in full-duplex mode to establish synchronization. To avoid interference, the UW must be chosen such that it has a good auto-correlation and cross-correlation properties. The auto-correlation of a sequence A, denoted by S_N, is defined as

$$S_N = \sum_{i=0}^{L} a_i . a_{i-N} \tag{7}$$

where L is the length of the sequence A, -L < N < L, N ≠ 0, a_i = -1 for i < 0, and a_i = a_{i-22} for i ≥ L. A "window" version of S_N can also be defined according to Eq. (7) with the exception that 0 < N < W, where W is the window size. The desired auto-correlation property is that the maximum value of the auto-correlation S_N (with or without the window where the window size is the size of the detection window, WSL) be less than L - 2 × T, where T is the allowable number of UW errors programmed into the W9310.

The cross-correlation of two sequences A and B, denoted by R_N, is defined as

$$R_N = \sum_{i=0}^{L} a_i . b_{i-N} \tag{8}$$

where L is the length of the sequence, $0 \le N \le L$, and $b_i = b_{i+22}$ for $i < 0$. As before, the desired cross-correlation property is that the maximum value of the cross-correlation R_N is less than $L - 2 \times T$, where L and T are as defined previously.

Requirements for choosing good UWs can be thus summarized by the following equations:

$$S_N < L - 2 \times T$$
$$R_N < L - 2 \times T \quad (9)$$

For example, when T is programmed to be 4, S_N and R_N should be less than 14, since L is 22.

Generating the PN and UW Sequences

There are many ways of generating the PN and UW sequences, including a brute-force search of the complete code space. A more efficient but probably suboptimal way of generating the PN and UW sequences is to perform the following steps:

1. Generate the M and Gold sequences of order N, where

$$N = \log_2 L \quad (10)$$

   and where L is the length of the PN or UW sequence.

2. Because M and Gold sequences are only $2_N - 1$ bits long, it is necessary to append an additional bit to these sequences so that they are 2_N bits long. The additional bit should be chosen such that the modified M or Gold sequence is even.
3. Apply the criteria outlined in the previous sections to pick out a good set of PN and UW sequences.

Some Examples of PN and UW Sequences

NO.	PNA	PNB	PNC	PND
1	9A42BB1E	1F348576	763E690A	0AEC7CD2
2	8DD4259E	9F1BA84A	4B3E3750	50967C6E
3	B8AD0C9E	9F715A18	193EE2B4	B4327DC4
4	B386A45E	5F670D48	48BECE1A	1A917D9C

NO.	UW	NO.	UW	NO.	UW	NO.	UW
1	96C55C	6	9D85BC	11	996E7C	16	9707B4
2	987ABC	7	9C2F34	12	9723DC	17	99A0F4
3	9E875C	8	993CF4	13	9817AC	18	9CC97C
4	98A17C	9	998794	14	9C53F4	19	98D3E4
5	9A83EC	10	9A887C	15	9E42F4	20	983EB4

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