



**AD120**

**Preliminary**

**3-Level / 258 Outputs TFT LCD Gate Driver**

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**Document Title**

**3-Level / 258 Outputs TFT LCD Gate Driver**

**Revision History**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
0.0	Initial issue	August 10, 2001	Preliminary

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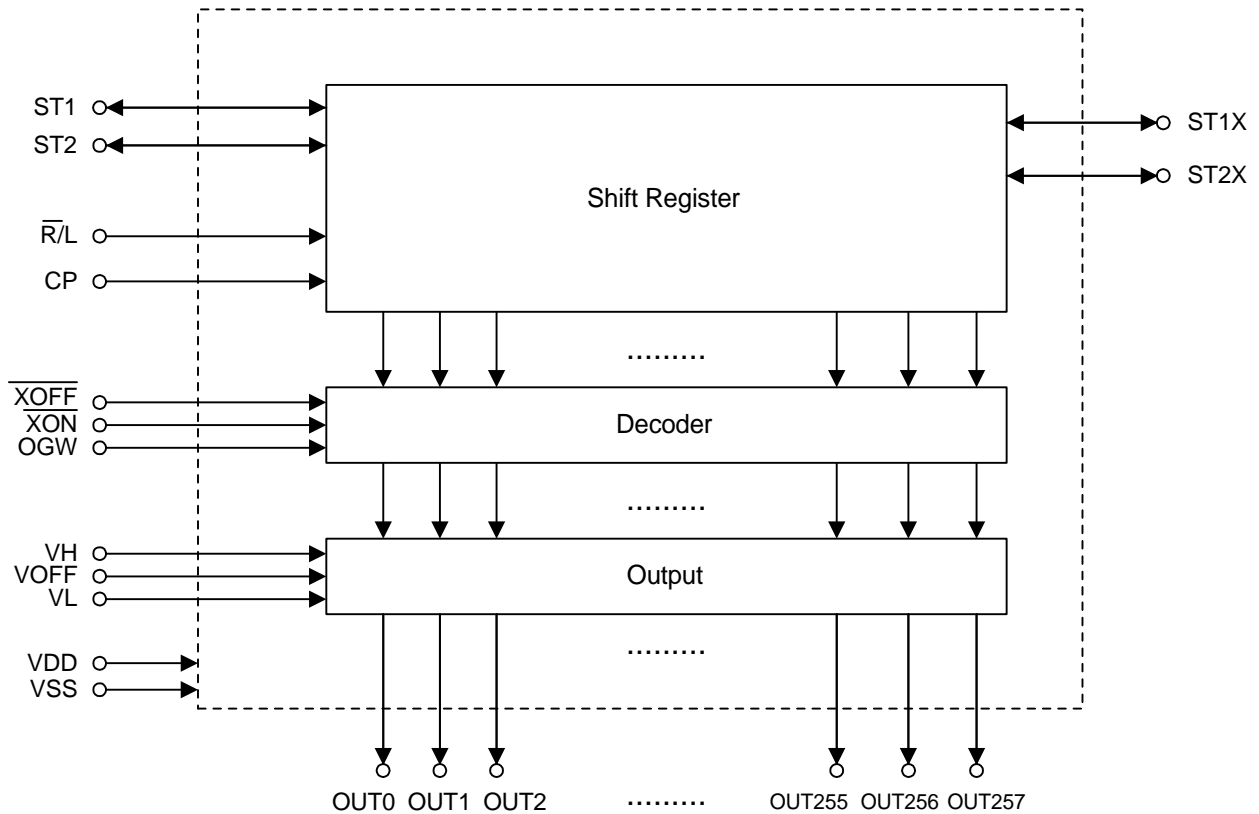


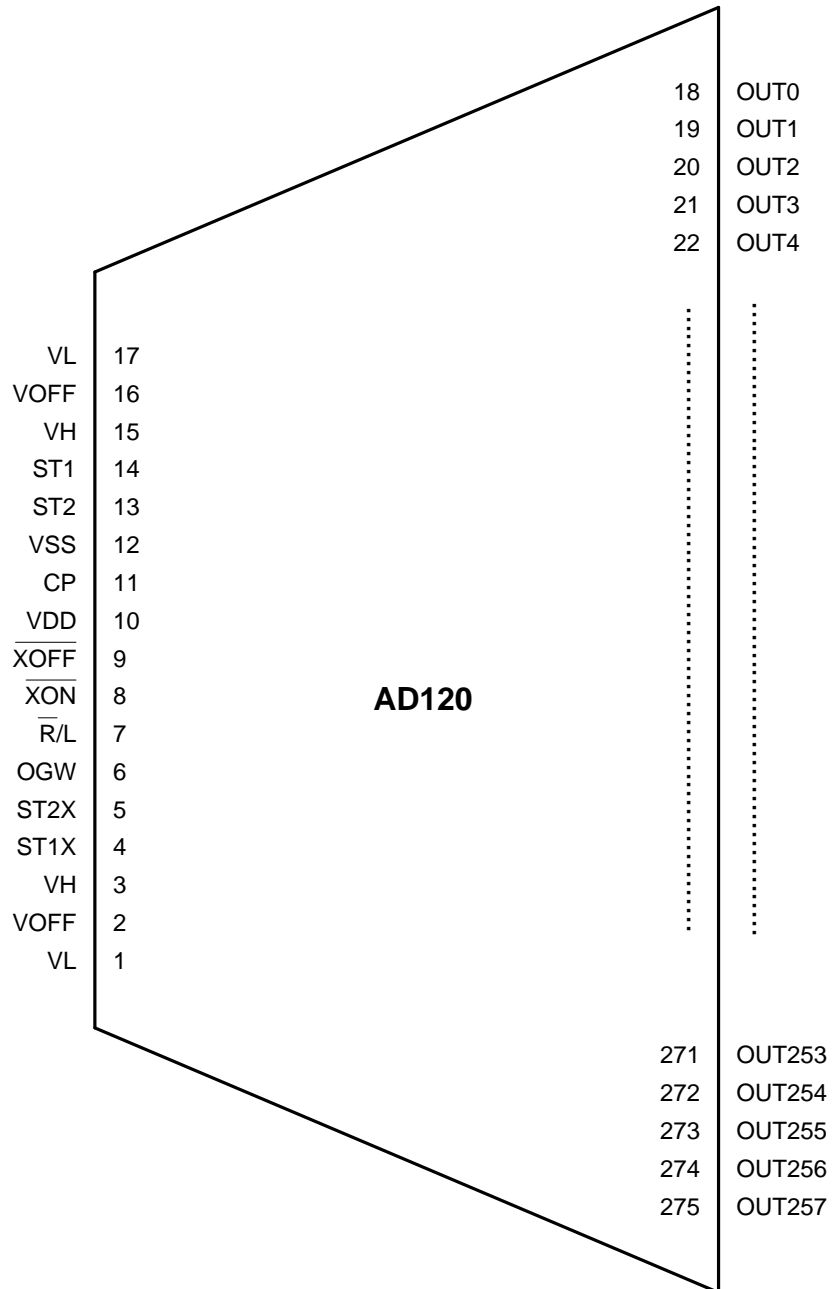
Features

- TFT LCD gate driver
- 3-level / 258 outputs
- 40V max. for each output
- -15V min. for each output
- 2.7V~3.6V logic input/output level
- Bi-directional data shift control
- Output waveform control
- TCP available

AD120 is a gate driver for TFT LCD panel. There are 258 outputs in the chip. Three-level output allows voltage correction for better switching noise rejection. It can be used for XGA / SXGA panels.

Block Diagram



**TCP Pinout**


**Input/Output Pin Function**

Pin No.	Symbol	I/O	Description
11	CP	I	Clock pulse
7	$\overline{R}/L$	I	Right / left direction control for shift register When $\overline{R}/L$ is LOW, data are shifted to the right, or ST1 / ST2 output0 output1 .... output257. When $\overline{R}/L$ is HIGH, data are shifted to the left, or ST1X / ST2X output257 output256 .... output0.
8	$\overline{XON}$	I	$\overline{XON}$ to force all the outputs to VH voltage. It is not synchronous to CP.
9	$\overline{XOFF}$	I	$\overline{XOFF}$ to force all the outputs to VOFF voltage. It is not synchronous to CP.
6	OGW	I	Output Gate pulse Width to select output_waveform format.
4,5, 13,14	ST1, ST2, ST1X, ST2X	I/O	When $\overline{R}/L$ is LOW, ST1 / ST2 are defined as inputs while ST1X / ST2X are defined as outputs . The synchronized ST1 / ST2 signals are placed at ST1X / ST2X after 256 CP pulses. When $\overline{R}/L$ is HIGH, ST1X / ST2X are defined as inputs, while ST1/ST2 are defined as outputs. The synchronized ST1X / ST2X signals are placed at ST1 / ST2 after 256 CP pulses.
18 - 275	OUT0~ OUT257	O	Output drivers These outputs are synchronized to CP pulses. The output format and voltage level are controlled by OGW, $\overline{XON}$ , $\overline{XOFF}$ , ST1 / ST2, ST1X / ST2X and $\overline{R}/L$ correspondingly as shown in the diagram.
12	VSS	PWR	Reference voltage
10	VDD	PWR	Supply voltage for logic operation VDD and VSS are voltage levels of input / output logic signals
3, 15	VH	PWR	High voltage for output drivers
1, 17	VL	PWR	Low voltage for output drivers
2, 16	VOFF	PWR	OFF voltage for output drivers

## Description

### Operation

Output signals OUT0~OUT257 are used for control of the TFT gates of the LCD panel. A bi-directional shift register is implemented to sequentially output signals OUT0~OUT257. A clock pulse CP is applied to the bi-directional shift register and the direction of the register is controlled by  $\bar{R}/L$  signal.

When  $\bar{R}/L$  is LOW and either starting signal ST1 or ST2 goes to HIGH, the shift register starts shifting from OUT0 to OUT257. The voltages of the corresponding outputs switch to V<sub>H</sub>, V<sub>L</sub> or V<sub>OFF</sub> depending on the starting signals as shown in the diagram. The outputs of the starting signals ST1X / ST2X switch accordingly after 256 CP pulses following start of the shift register which allows expansion of the outputs by cascading more devices.

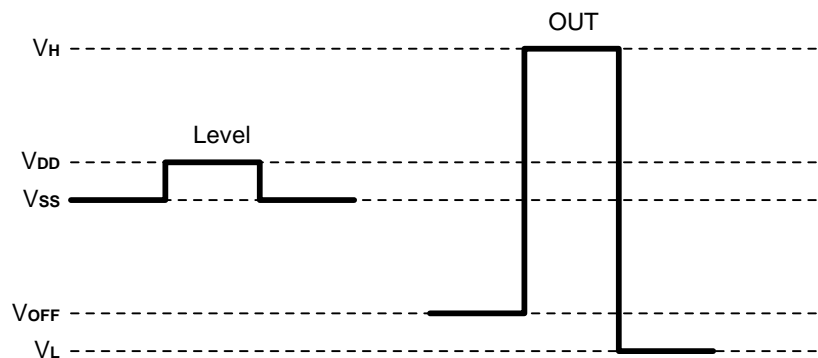
When  $\bar{R}/L$  is HIGH and either starting signal ST1X or ST2X goes to HIGH, the shift register starts shifting from OUT257 to OUT0. The voltages of the corresponding outputs switch to V<sub>H</sub>, V<sub>L</sub> or V<sub>OFF</sub> depending on the starting signals as shown in the diagram. The outputs of the starting signals ST1/ST2 switch accordingly after 256 CP pulses following start of the shift register which allows expansion of the outputs by cascading more devices.

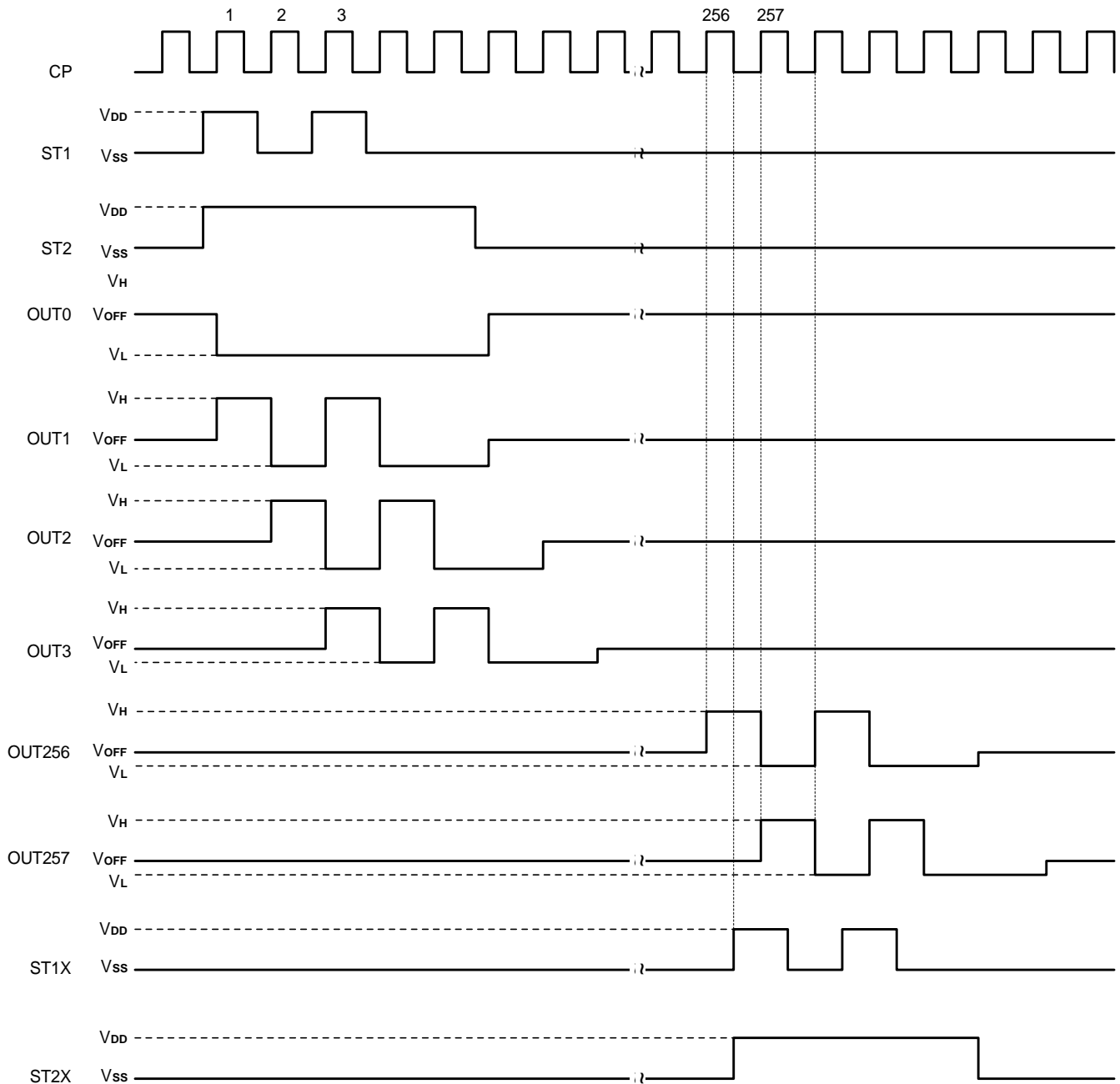
### 3-Level Output

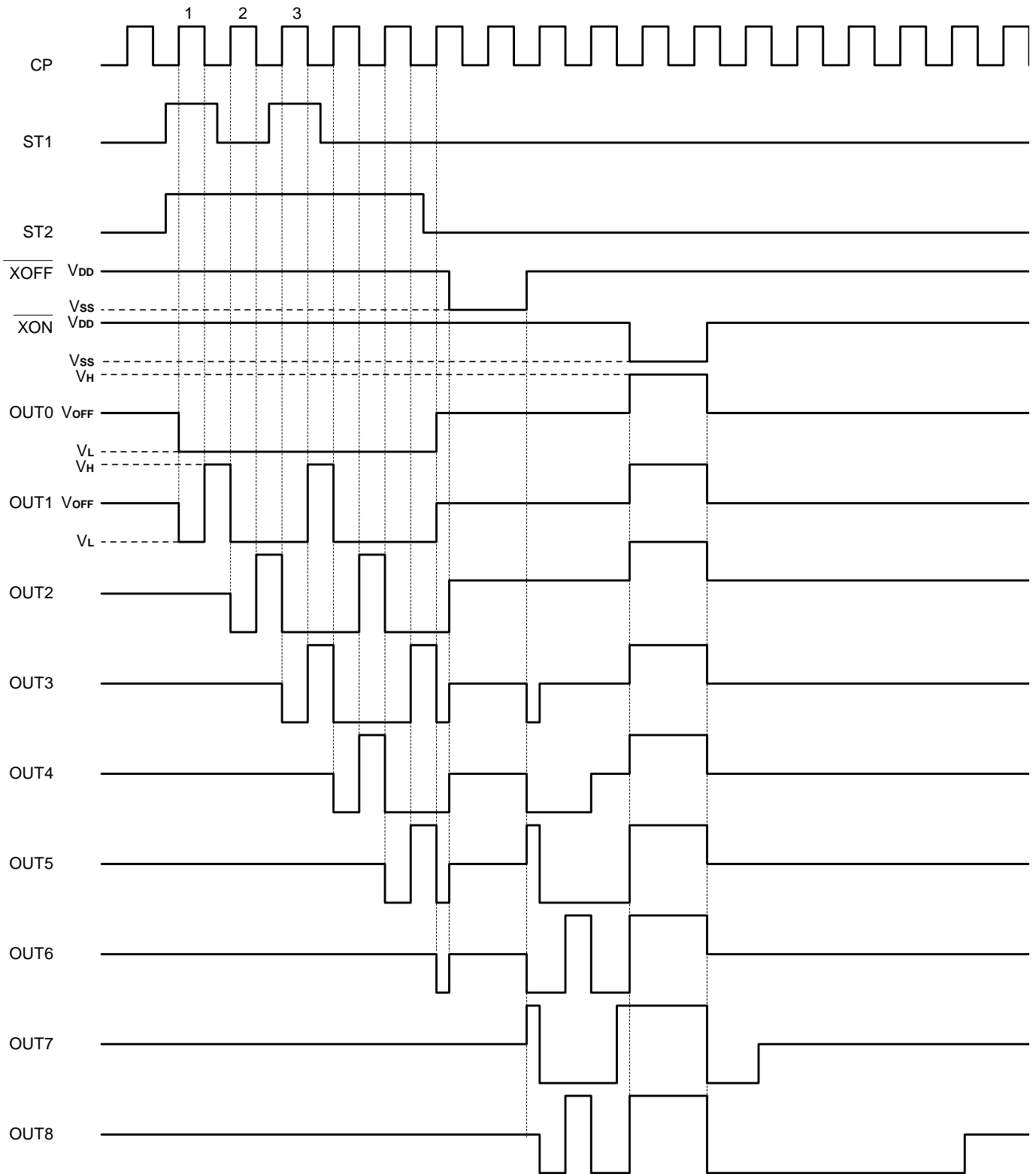
$$V_H - V_L = 40V(\text{max.})$$

$$V_{OFF} - V_L = 0\sim 10V$$

$$V_H - V_{SS} = 17\sim 28V$$



**Operation Diagram 1 ( $\overline{R}/L = L$ ,  $OGW = L$ )**


**Operation Diagram 2 ( $\overline{R}/L = L$ ,  $OGW = H$ )**


**Table 1. Function of  $\overline{XON}$  and  $\overline{XOFF}$** 

$\overline{XON}$	$\overline{XOFF}$	OUT0~OUT257
L	X	VH
H	L	VOFF
H	H	Table2

\* The outputs are asynchronous to CP.

**Table 2. Control of OUT1~OUT256**

( $\overline{XON} = H, \overline{XOFF} = H$ )

$(\overline{R}/L = L)$ ST1	ST2	OGW	OUT1~OUT256
$(\overline{R}/L = H)$ ST1X	ST2X		
L	L	X	VOFF
L	H	X	VL
H	L	X	VL
H	H	L	VH
		H	VH (CP = "L") VL (CP = "H")

\* The outputs are synchronous to CP.

**Table 3. Control of OUT0 and OUT257**

( $\overline{XON} = H, \overline{XOFF} = H$ )

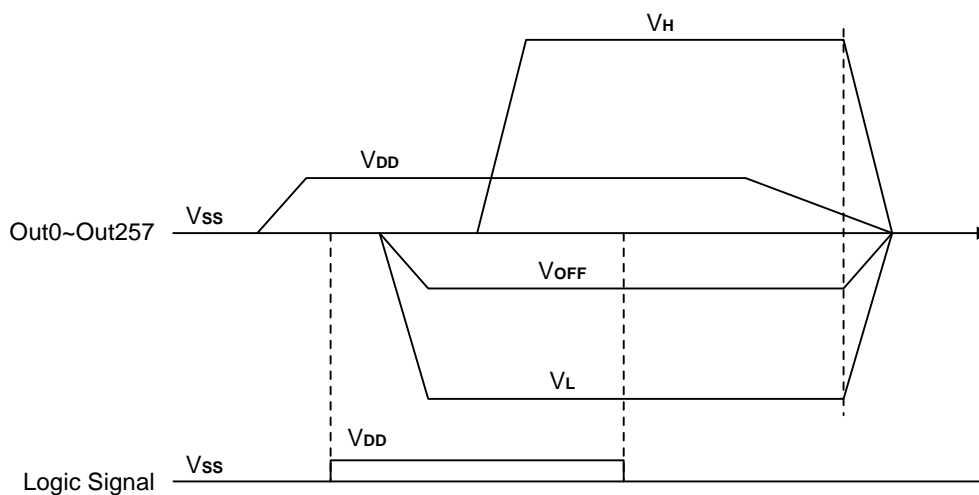
$(\overline{R}/L = L)$ ST1	ST2	OUT0
$(\overline{R}/L = H)$ ST1X	ST2X	OUT257
L	L	VOFF
L	H	VL
H	L	VL
H	H	VL

\* The outputs are synchronous to CP.



**Absolute Maximum Ratings Over Operating Free-air Temperature Range**

Parameter	Symbol	Ratings	Unit
Supply Voltage	VDD	-0.3 ~ +7.0	V
Supply Voltage	VH	-0.3 ~ 42.0	V
Supply Voltage	VL	-20.0 ~ +0.3	V
Supply Voltage	VOFF	VL-0.3 ~ VL+11.0	V
Supply Voltage	VH - VL	-0.3 ~ 42.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Storage Temperature	Tstg	-55 ~ 125	°C

**Power\_on Sequence and Voltage Levels**

**Operating Voltage Range**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	2.7	3.3	3.6	V
Supply Voltage	VH	17	-	28	V
Supply Voltage	VL	-15	-	-5	V
Supply Voltage	VOFF - VL	0	-	10.0	V
Supply Voltage	VH - VL	22	-	40	V
Clock Frequency	f <sub>CP</sub>	-	-	100	KHz
Operating Free-air Temperature	T <sub>a</sub>	-20	-	+75	°C

**DC Characteristics**

(VDD = 2.7~3.6V, Ta = -20~75°C)

Parameter	Symbol	Condition	Min.	Max.	Unit	Applicable Pin	Note
Low Level Input Voltage	V <sub>IL</sub>		VSS	0.2 X VDD	V	All input pins	
High Level Input Voltage	V <sub>IH</sub>		0.8 X VDD	VDD	V	All input pins	
Low Level Output Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 40μA	VSS	VSS + 0.4	V	ST1, ST2, ST1X, ST2X	
High Level Output Voltage	V <sub>OH</sub>	I <sub>OH</sub> = 40μA	VDD - 0.4	VDD	V		
Output Resistance (1)	R <sub>L</sub>	V <sub>OUT</sub> = V <sub>L</sub> + 0.5		1000	Ω	OUT0~OUT257	1
Output Resistance (2)	R <sub>OFF</sub>	V <sub>OUT</sub> = V <sub>OFF</sub> + 0.5		1000	Ω	OUT0~OUT257	1
Output Resistance (3)	R <sub>H</sub>	V <sub>OUT</sub> = V <sub>H</sub> - 0.5		1000	Ω	OUT0~OUT257	1
Input Current	I <sub>I</sub>	V <sub>I</sub> = VDD / VSS	-5.0	+5.0	μA	All input pins	
Operating Current (1)	I <sub>DD</sub>			1500	μA	VDD	1, 2
Operating Current (2)	I <sub>H</sub>			100	μA	VH	1, 2

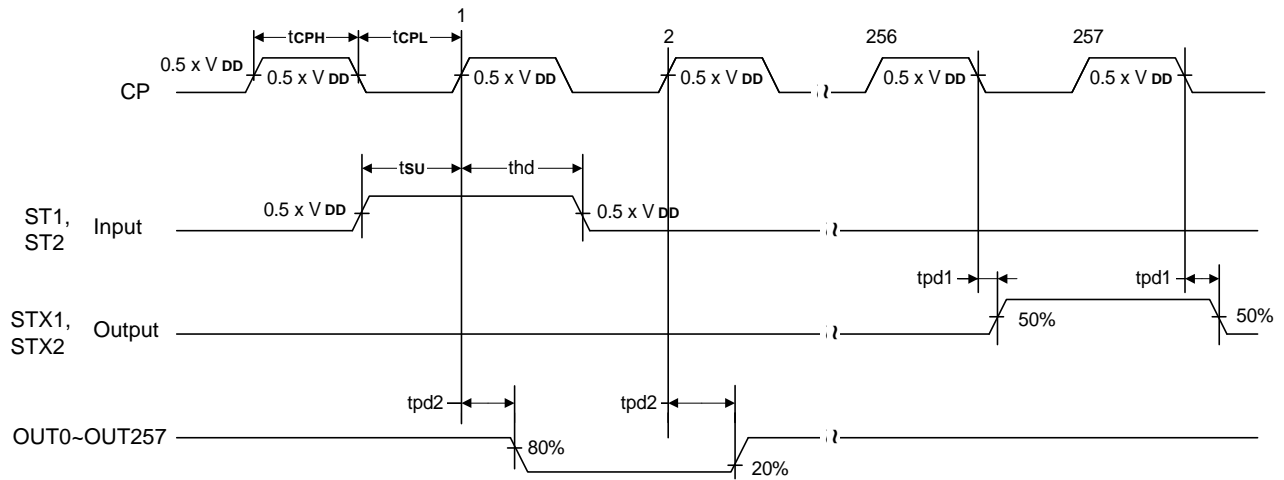
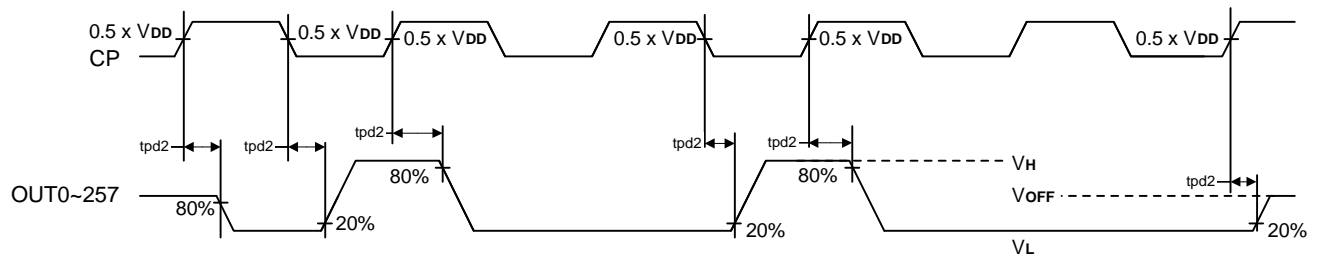
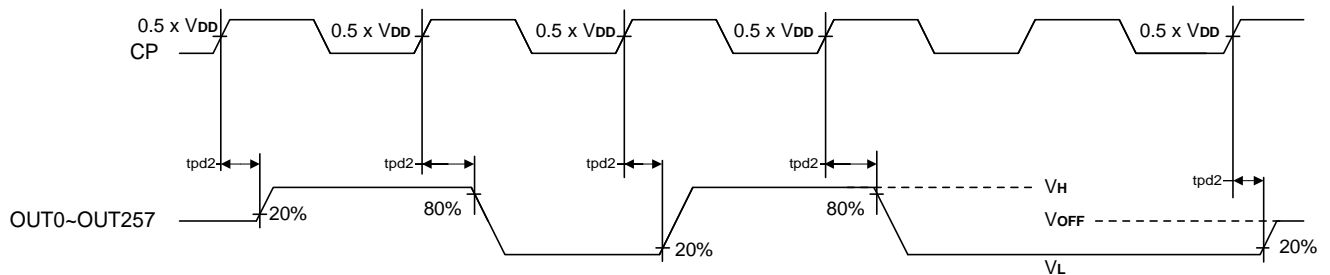
**Notes:**

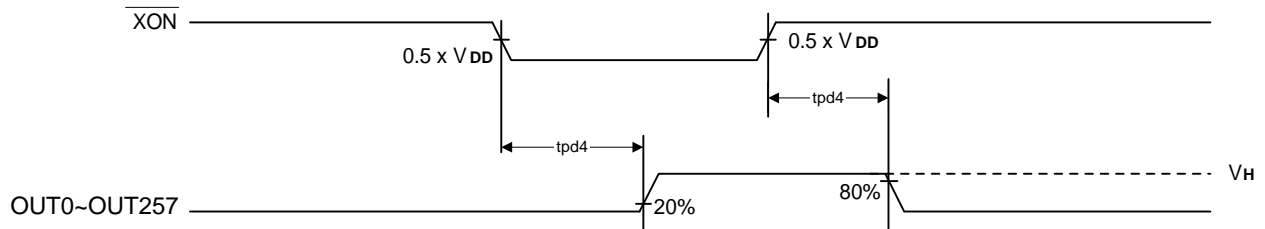
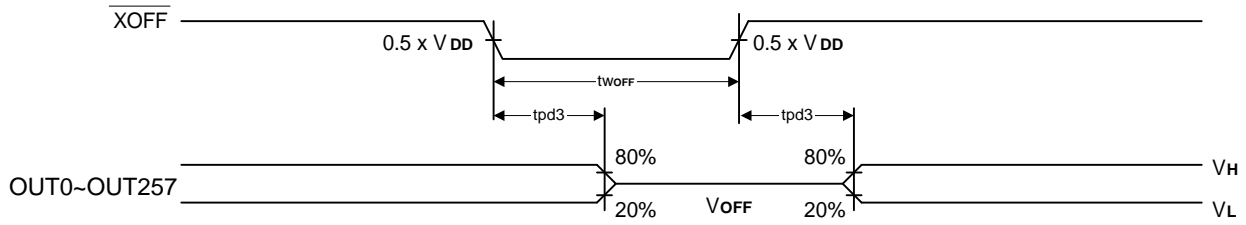
1. V<sub>H</sub> = 25V, V<sub>OFF</sub> = 0V, V<sub>L</sub> = -10V
2. CP = 50KHz

**AC Characteristics**

(VDD = 2.7~3.6V, Ta = -20~75°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Frequency	f <sub>CP</sub>			100	KHz
CP High Pulse Width	t <sub>CPH</sub>		1		μs
CP Low Pulse Width	t <sub>CPL</sub>		4		μs
Input Rise Time	t <sub>r</sub>	10% ~ 90%		50	ns
Input Fall Time	t <sub>f</sub>	90% ~ 10%		50	ns
Gate Off Time	t <sub>WOFF</sub>		1		μs
Data Setup Time	t <sub>SU</sub>		700		ns
Data Hold Time	t <sub>HD</sub>		700		ns
Delay Time 1	t <sub>PD1</sub>	CL = 20pF		800	ns
Delay Time 2	t <sub>PD2</sub>	CL = 300pF		1000	ns
Delay Time 3	t <sub>PD3</sub>	CL = 300pF		1000	ns
Delay Time 4	t <sub>PD4</sub>	CL = 300pF		1000	ns
Delay Time 5	t <sub>PD5</sub>	CL = 300pF		1000	ns

**Timing Waveform**

**(OGW = H)**

**(OGW = L)**


**Timing Waveform (continued)**




**Ordering Information**

Part No.	Package
AD120T	TCP