

ADG706/ADG707

FEATURES

- 1.8 V to 5.5 V Single Supply
- ± 3 V Dual Supply
- 2.5 Ω On Resistance
- 0.5 Ω On-Resistance Flatness
- 100 pA Leakage Currents
- 40 ns Switching Times
- Single 16-to-1 Multiplexer ADG706
- Differential 8-to-1 Multiplexer ADG707
- 28-Lead TSSOP Package
- Low-Power Consumption
- TTL/CMOS-Compatible Inputs

APPLICATIONS

- Data Acquisition Systems
- Communication Systems
- Relay Replacement
- Audio and Video Switching
- Battery-Powered Systems

GENERAL DESCRIPTION

The ADG706 and ADG707 are low-voltage, CMOS analog multiplexers comprising 16 single channels and eight differential channels respectively. The ADG706 switches one of 16 inputs (S1–S16) to a common output, D, as determined by the 4-bit binary address lines A0, A1, A2, and A3. The ADG707 switches one of eight differential inputs to a common differential output as determined by the 3-bit binary address lines A0, A1, and A2. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF.

Low-power consumption and operating supply range of 1.8 V to 5.5 V make the ADG706 and ADG707 ideal for battery-powered, portable instruments. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. These devices are also designed to operate from a dual supply of ± 3 V.

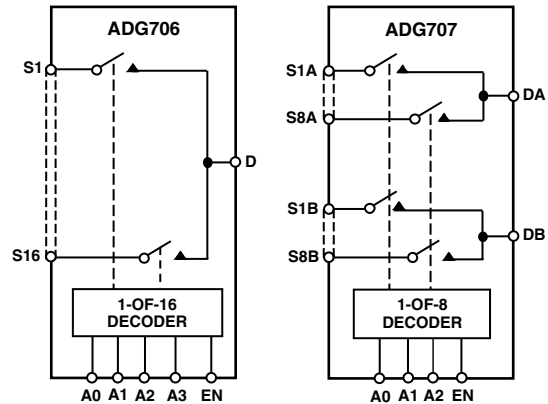
These multiplexers are designed on an enhanced submicron process that provides low-power dissipation yet gives high-switching speed, very low on resistance and leakage currents. On resistance is in the region of a few ohms and is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either multiplexers or demultiplexers and have an input signal range which extends to the supplies.

The ADG706 and ADG707 are available in small 28-lead TSSOP packages.

REV. 0

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FUNCTIONAL BLOCK DIAGRAMS



PRODUCT HIGHLIGHTS

1. Single/Dual Supply Operation. The ADG706 and ADG707 are fully specified and guaranteed with 3 V and 5 V single supply and ± 3 V dual supply rails.
2. Low On Resistance (2.5 Ω typical).
3. Low-Power Consumption ($<0.01 \mu\text{W}$).
4. Guaranteed Break-Before-Make Switching Action.
5. Small 28-Lead TSSOP Package.

ADG706/ADG707—SPECIFICATIONS¹ ($V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	25°C	-40°C to +85°C		
ANALOG SWITCH				
Analogue Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = 10\text{ mA}$; Test Circuit 1
	4.5	5	Ω max	
On Resistance Match Between Channels (ΔR_{ON})		0.3	Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5	0.8	Ω max	
		1.2	Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
			Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = 5.5\text{ V}$ $V_D = 4.5\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/4.5\text{ V}$; Test Circuit 2
	± 0.1	± 0.3	nA max	
Drain OFF Leakage I_D (OFF)	± 0.01		nA typ	$V_D = 4.5\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/4.5\text{ V}$; Test Circuit 3
ADG706	± 0.4	± 1.5	nA max	
ADG707	± 0.1	± 1	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.01		nA typ	$V_D = V_S = 1\text{ V}$, or 4.5 V ; Test Circuit 4
ADG706	± 0.4	± 1.5	nA max	
ADG707	± 0.1	± 1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
C_{IN} , Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS²				
$t_{TRANSITION}$	40		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 5; $V_{S1} = 3\text{ V}/0\text{ V}$, $V_{S16} = 0\text{ V}/3\text{ V}$
		60	ns max	
Break-Before-Make Time Delay, t_D	30		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 3\text{ V}$, Test Circuit 6
		1	ns min	
t_{ON} (EN)	32		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 3\text{ V}$, Test Circuit 7
		50	ns max	
t_{OFF} (EN)	10		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 3\text{ V}$, Test Circuit 7
		14	ns max	
Charge Injection	± 5		pC typ	$V_S = 1\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 8
Off Isolation	-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 9
	-80		dB typ	
Channel-to-Channel Crosstalk	-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 10
	-80		dB typ	
-3 dB Bandwidth				
ADG706	25		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
ADG707	36		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG706	180		pF typ	
ADG707	90		pF typ	
C_D , C_S (ON)				
ADG706	200		pF typ	
ADG707	100		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.001		μA typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
		1.0	μA max	

NOTES

¹Temperature range is as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS¹

($V_{DD} = 3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Version		Unit	Test Conditions/Comments
	25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	6		Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = 10\text{ mA}$;
	11	12	Ω max	Test Circuit 1
On-Resistance Match Between Channels (ΔR_{ON})		0.4	Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)		1.2	Ω max	
		3	Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = 3.3\text{ V}$
	± 0.1	± 0.3	nA max	$V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$;
Drain OFF Leakage I_D (OFF)	± 0.01		nA typ	Test Circuit 2
ADG706	± 0.4	± 1.5	nA max	$V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$;
ADG707	± 0.1	± 1	nA max	Test Circuit 3
Channel ON Leakage I_D , I_S (ON)	± 0.01		nA typ	$V_S = V_D = 1\text{ V}$ or 3 V ;
ADG706	± 0.4	± 1.5	nA max	Test Circuit 4
ADG707	± 0.1	± 1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
C_{IN} , Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS²				
$t_{TRANSITION}$	45		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 5
		75	ns max	$V_{S1} = 2\text{ V}/0\text{ V}$, $V_{S16} = 0\text{ V}/2\text{ V}$
Break-Before-Make Time Delay, t_D	30		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$;
		1	ns min	$V_S = 2\text{ V}$, Test Circuit 6
t_{ON} (EN)	40		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$;
		70	ns max	$V_S = 2\text{ V}$, Test Circuit 7
t_{OFF} (EN)	20		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$;
		28	ns max	$V_S = 2\text{ V}$, Test Circuit 7
Charge Injection	± 5		pC typ	$V_S = 1\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$;
				Test Circuit 8
Off Isolation	-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$;
	-80		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
				Test Circuit 9
Channel-to-Channel Crosstalk	-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$;
	-80		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
				Test Circuit 10
-3 dB Bandwidth				
ADG706	25		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
ADG707	36		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG706	180		pF typ	
ADG707	90		pF typ	
C_D , C_S (ON)				
ADG706	200		pF typ	
ADG707	100		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.001		μA typ	$V_{DD} = 3.3\text{ V}$
		1.0	μA max	Digital Inputs = 0 V or 3.3 V

NOTES

¹Temperature ranges are as follows: B Versions: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

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ADG706/ADG707

Dual Supply¹ ($V_{DD} = +3\text{ V} \pm 10\%$, $V_{SS} = -3\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.)

Parameter	B Version -40°C to +85°C		Unit	Test Conditions/Comments
	25°C			
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	2.5 4.5		Ω typ Ω max	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$; Test Circuit 1
On-Resistance Match Between Channels (ΔR_{ON})		0.3 0.8	Ω typ Ω max	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ Ω max	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01 ± 0.1	± 0.3	nA typ nA max	$V_{DD} = +3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$ $V_S = +2.25\text{ V}/-1.25\text{ V}$, $V_D = -1.25\text{ V}/+2.25\text{ V}$; Test Circuit 2
Drain OFF Leakage I_D (OFF)	± 0.01		nA typ	$V_S = +2.25\text{ V}/-1.25\text{ V}$, $V_D = -1.25\text{ V}/+2.25\text{ V}$; Test Circuit 3
ADG706	± 0.4	± 1.5	nA max	
ADG707	± 0.1	± 1	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.01		nA typ	$V_S = V_D = +2.25\text{ V}/-1.25\text{ V}$, Test Circuit 4
ADG706	± 0.4	± 1.5	nA max	
ADG707	± 0.1	± 1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	pF typ	
C_{IN} , Digital Input Capacitance	5			
DYNAMIC CHARACTERISTICS²				
$t_{TRANSITION}$	40		ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 5 $V_{S1} = 1.5\text{ V}/0\text{ V}$, $V_{S16} = 0\text{ V}/1.5\text{ V}$
Break-Before-Make Time Delay, t_D	15	60	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, Test Circuit 6
t_{ON} (EN)	32	1	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, Test Circuit 7
t_{OFF} (EN)	16	50	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, Test Circuit 7
Charge Injection	± 8	26	ns typ pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 8
Off Isolation	-60 -80		dB typ dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 9
Channel-to-Channel Crosstalk	-60 -80		dB typ dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 10
-3 dB Bandwidth				
ADG706	25		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
ADG707	36		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG706	180		pF typ	
ADG707	90		pF typ	
C_D , C_S (ON)				
ADG706	200		pF typ	
ADG707	100		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.001		μA typ μA max	$V_{DD} = +3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V
I_{SS}	0.001	1.0	μA typ μA max	$V_{SS} = -3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V

NOTES

¹Temperature range is as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C unless otherwise noted)

V _{DD} to V _{SS}	7 V
V _{DD} to GND	-0.3 V to +7 V
V _{SS} to GND	+0.3 V to -3.5 V or 30 mA, Whichever Occurs First
Analog Inputs ²	V _{SS} - 0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs ²	-0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C

Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ _{JA} Thermal Impedance	97.9°C/W
θ _{JC} Thermal Impedance	14°C/W
Lead Temperature, Soldering (10 seconds)	300°C
IR Reflow, Peak Temperature	220°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overtolerances at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG706/ADG707 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

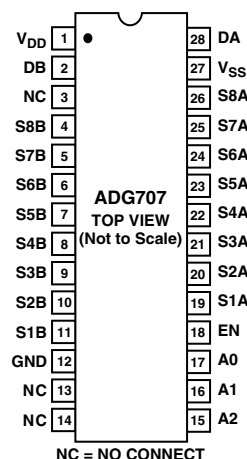
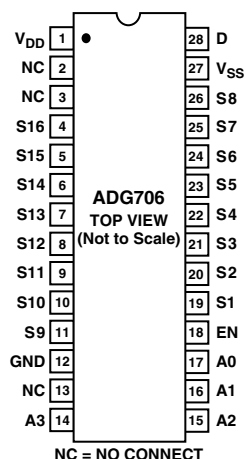


ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG706BRU	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-28
ADG707BRU	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-28

PIN CONFIGURATIONS

28-Lead TSSOP



ADG706/ADG707

Table I. ADG706 Truth Table

A3	A2	A1	A0	EN	ON Switch
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

X = Don't Care.

Table II. ADG707 Truth Table

A2	A1	A0	EN	ON Switch Pair
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care.

TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.	C_D (OFF)	“OFF” Switch Drain Capacitance. Measured with reference to ground.
V_{SS}	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground at the device.	C_D, C_S (ON)	“ON” Switch Capacitance. Measured with reference to ground.
I_{DD}	Positive Supply Current.	C_{IN}	Digital Input Capacitance.
I_{SS}	Negative Supply Current.	$t_{TRANSITION}$	Delay Time Measured Between the 50% and 90% Points of the Digital Inputs and the Switch “ON” Condition when Switching from One Address State to Another.
GND	Ground (0 V) Reference.	t_{ON} (EN)	Delay Time Between the 50% and 90% Points of the EN Digital Input and the Switch “ON” Condition.
S	Source Terminal. May be an input or output.	t_{OFF} (EN)	Delay Time Between the 50% and 90% Points of the EN Digital Input and the Switch “OFF” Condition.
D	Drain Terminal. May be an input or output.	t_{OPEN}	“OFF” Time Measured Between the 80% Points of Both Switches when Switching from One Address State to Another.
IN	Logic Control Input.	Charge Injection	A Measure of the Glitch Impulse Transferred from the Digital Input to the Analog Output During Switching.
$V_D (V_S)$	Analog Voltage on Terminals D, S.	Off Isolation	A Measure of Unwanted Signal Coupling through an “OFF” Switch.
R_{ON}	Ohmic Resistance Between D and S.	Crosstalk	A Measure of Unwanted Signal which is Coupled through from One Channel to Another as a Result of Parasitic Capacitance.
ΔR_{ON}	On Resistance Match Between any Two Channels, i.e., $R_{ONmax} - R_{ONmin}$.	Bandwidth	The Frequency at which the Output Is Attenuated by 3 dBs.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.	On Response	The Frequency Response of the “ON” Switch.
I_S (OFF)	Source Leakage Current with the Switch “OFF.”	Insertion Loss	The Loss Due to the ON Resistance of the Switch.
I_D (OFF)	Drain Leakage Current with the Switch “OFF.”		
I_D, I_S (ON)	Channel Leakage Current with the Switch “ON.”		
V_{INL}	Maximum Input Voltage for Logic “0.”		
V_{INH}	Minimum Input Voltage for Logic “1.”		
$I_{INL}(I_{INH})$	Input Current of the Digital Input.		
C_S (OFF)	“OFF” Switch Source Capacitance. Measured with reference to ground.		

Typical Performance Characteristics—ADG706/ADG707

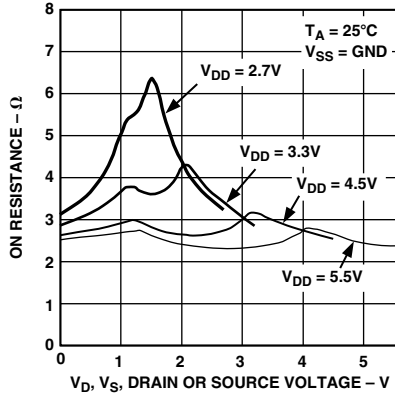


Figure 1. On Resistance as a Function of V_D (V_S) for Single Supply

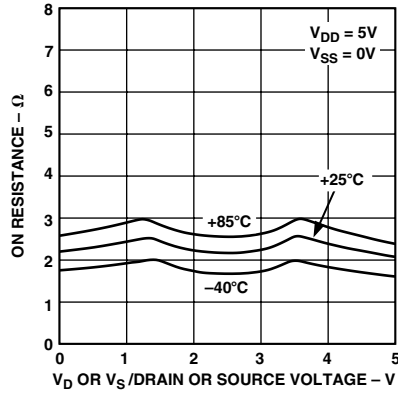


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

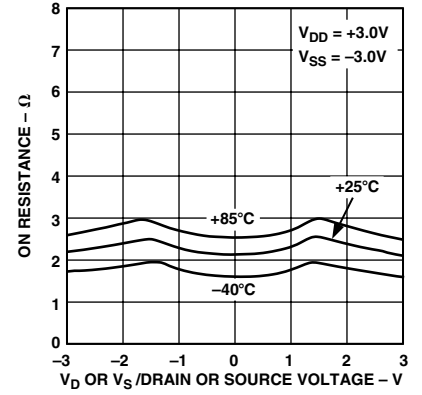


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

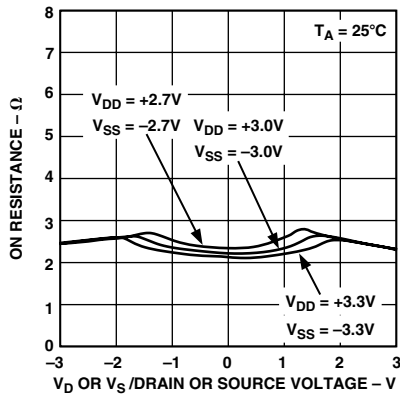


Figure 4. On Resistance as a Function of V_D (V_S) for Dual Supply

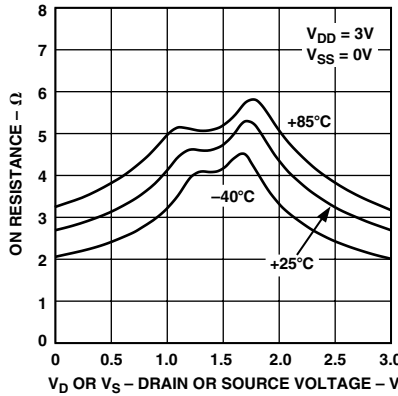


Figure 5. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

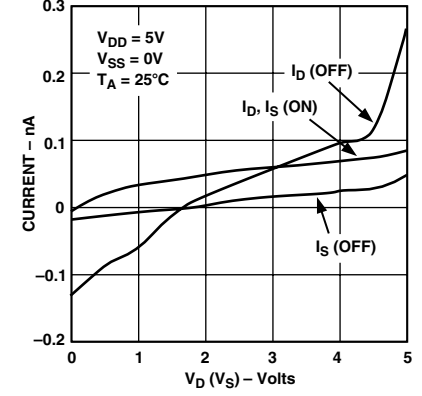


Figure 6. Leakage Currents as a Function of V_D (V_S)

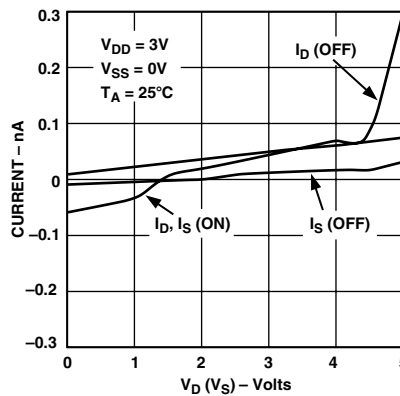


Figure 7. Leakage Currents as a Function of V_D (V_S)

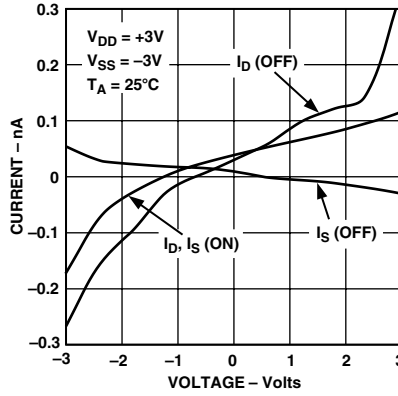


Figure 8. Leakage Currents as a Function of V_D (V_S)

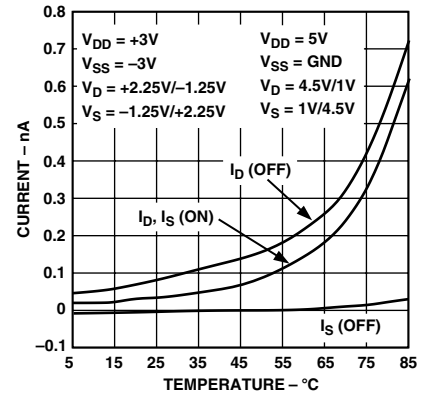


Figure 9. Leakage Currents as a Function of Temperature

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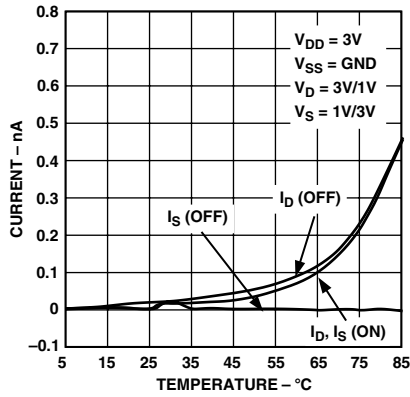


Figure 10. Leakage Currents as a Function of Temperature

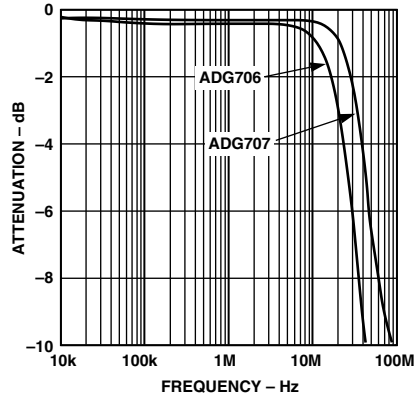


Figure 11. On Response vs. Frequency

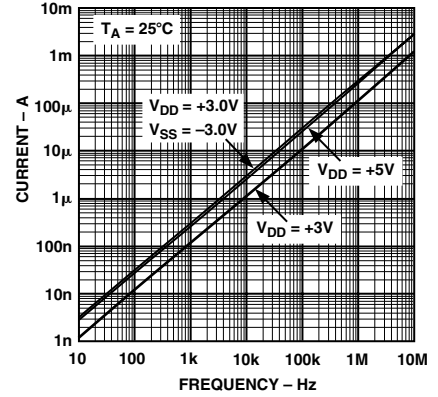


Figure 12. Supply Currents vs. Input Switching Frequency

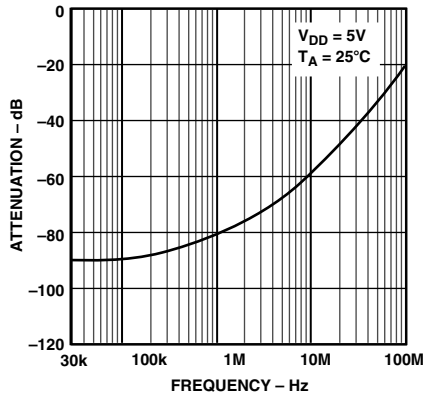


Figure 13. Off Isolation vs. Frequency

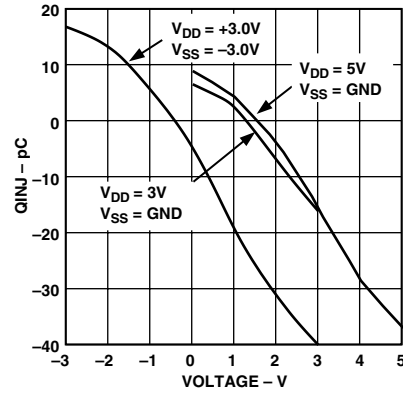


Figure 14. Charge Injection vs. Source Voltage

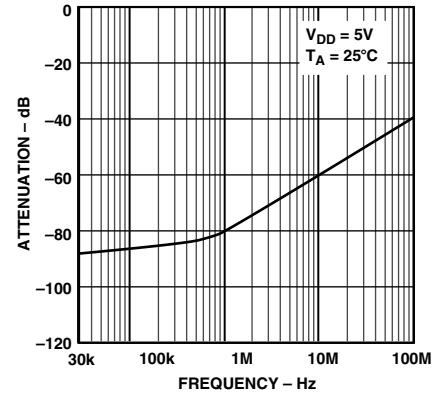
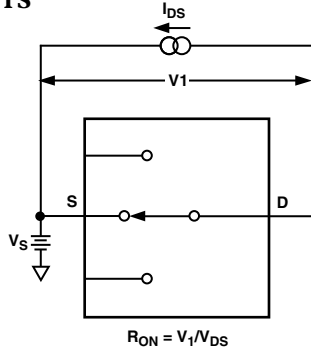
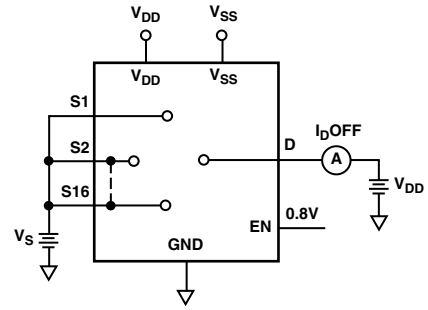


Figure 15. Crosstalk vs. Frequency

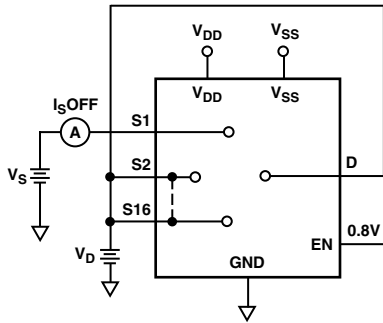
TEST CIRCUITS



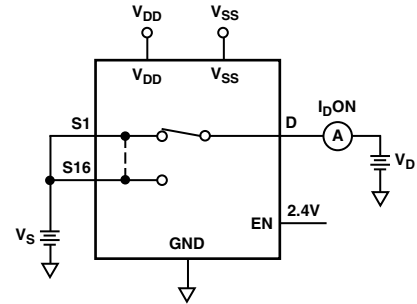
Test Circuit 1. On Resistance



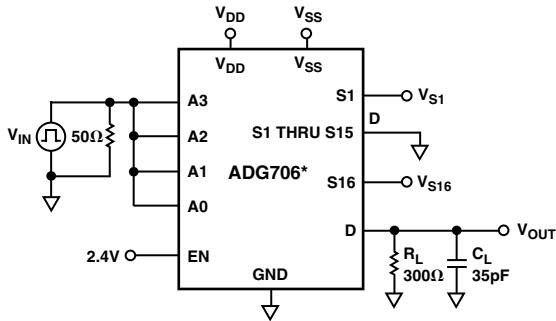
Test Circuit 3. I_D (OFF)



Test Circuit 2. I_S (OFF)

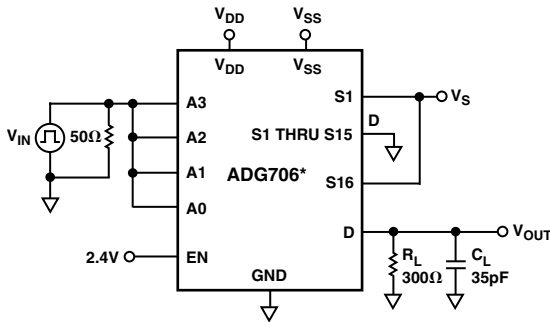
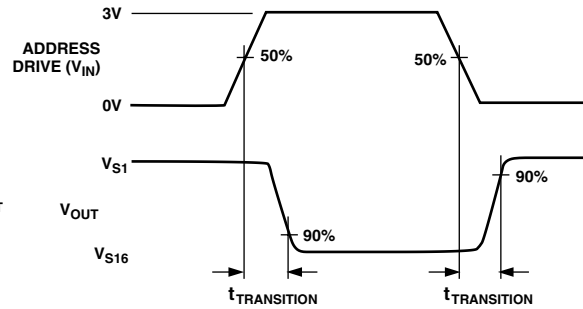


Test Circuit 4. I_D (ON)



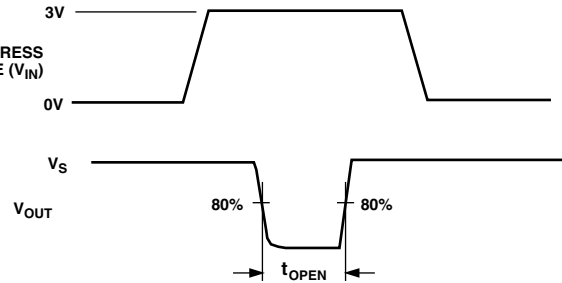
*SIMILAR CONNECTION FOR ADG707

Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$

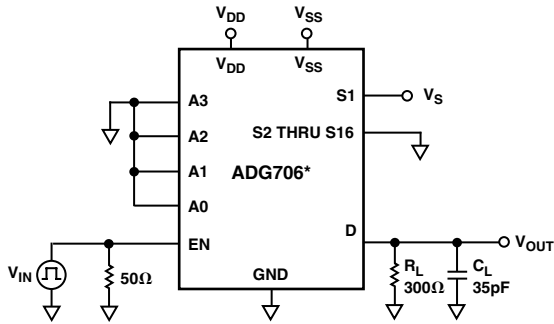


*SIMILAR CONNECTION FOR ADG707

Test Circuit 6. Break-Before-Make Delay, t_{OPEN}

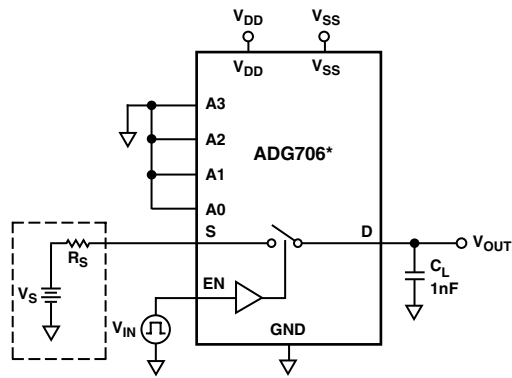
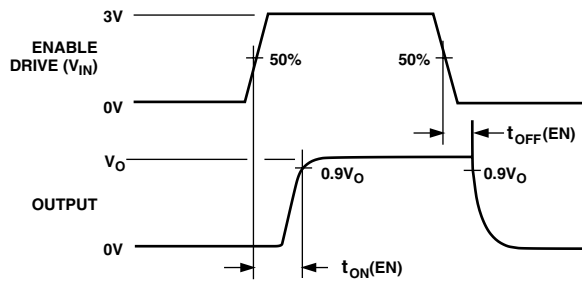


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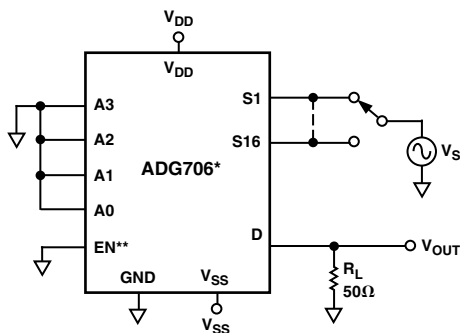
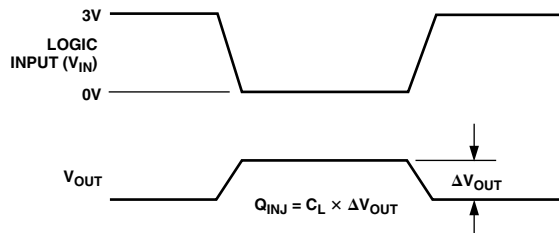
*SIMILAR CONNECTION FOR ADG707

Test Circuit 7. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$



*SIMILAR CONNECTION FOR ADG707

Test Circuit 8. Charge Injection



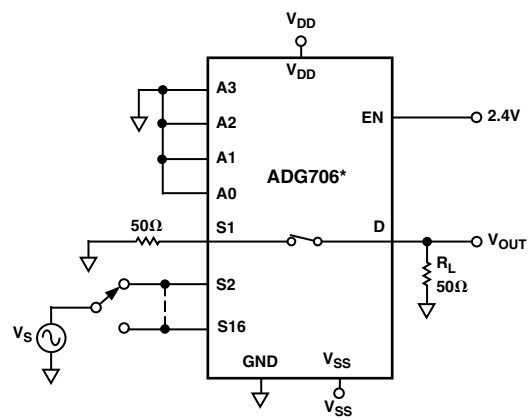
*SIMILAR CONNECTION FOR ADG707

**CONNECT TO 2.4V FOR BANDWIDTH MEASUREMENTS

OFF ISOLATION = $20\text{LOG}_{10}(V_{OUT}/V_S)$

OFF ISOLATION = $20\text{LOG}_{10}\left(\frac{V_{OUT} \text{ WITH SWITCH}}{V_{OUT} \text{ WITHOUT SWITCH}}\right)$

Test Circuit 9. Off Isolation and Bandwidth



*SIMILAR CONNECTION FOR ADG707
CHANNEL-TO-CHANNEL CROSSTALK = $20\text{LOG}_{10}(V_{OUT}/V_S)$

Test Circuit 10. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead TSSOP
(RU-28)

