SONY

CXD2931R

1 chip GPS LSI

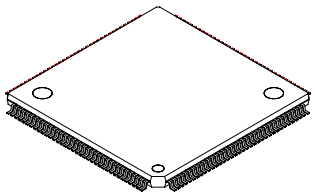
Description

The CXD2931R is a dedicated LSI for the GPS (Global Positioning System) satellite-based position measurement system.

This LSI contains a 32-bit RISC CPU, 2M-bit MASK ROM, RAM, UART, timer, and others.

This LSI, used together with the RF LSI (CXA1951AQ), enables the configuration of a 2-chip system capable of measuring its position anywhere on the globe.

144 pin LQFP (Plastic)



Features

- 16-channel GPS receiver capable of simultaneously receiving 16 satellites
- Supports differential GPS
  — Comforms to RTCM SC-104 Ver. 2.1
  — Supports DARC
- All-in-view measurement
- 2-satellite measurement
- Timer supporting GPS time
- High performance 32-bit RISC CPU
- 256K-byte program ROM
- 36K-byte RAM
- 3-channel UART
  — Baud rate generator
  — Supports 1.2K, 2.4K, 4.8K, 9.6K, 19.2K and 38.4K baud
  — Supports 1/2/4-byte buffer mode
- 23-bit general-purpose I/O port capable of defining input/output independently for each bit

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to 4.6	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–40 to +85	°C
• Storage temperature	Tstg	–50 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 3.6	V
• Operating temperature	Topr	–40 to +85	°C

Input/Output Pin Capacitance

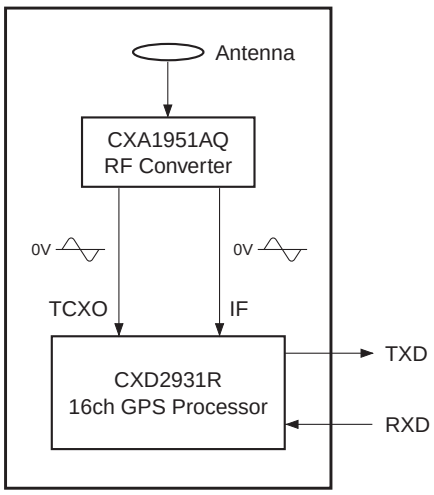
• Input capacitance	C_{IN}	9 (Max.)	pF
• Output capacitance	C_{OUT}	11 (Max.)	pF
• I/O capacitance	$C_{I/O}$	11 (Max.)	pF

E99702-PS

Performance

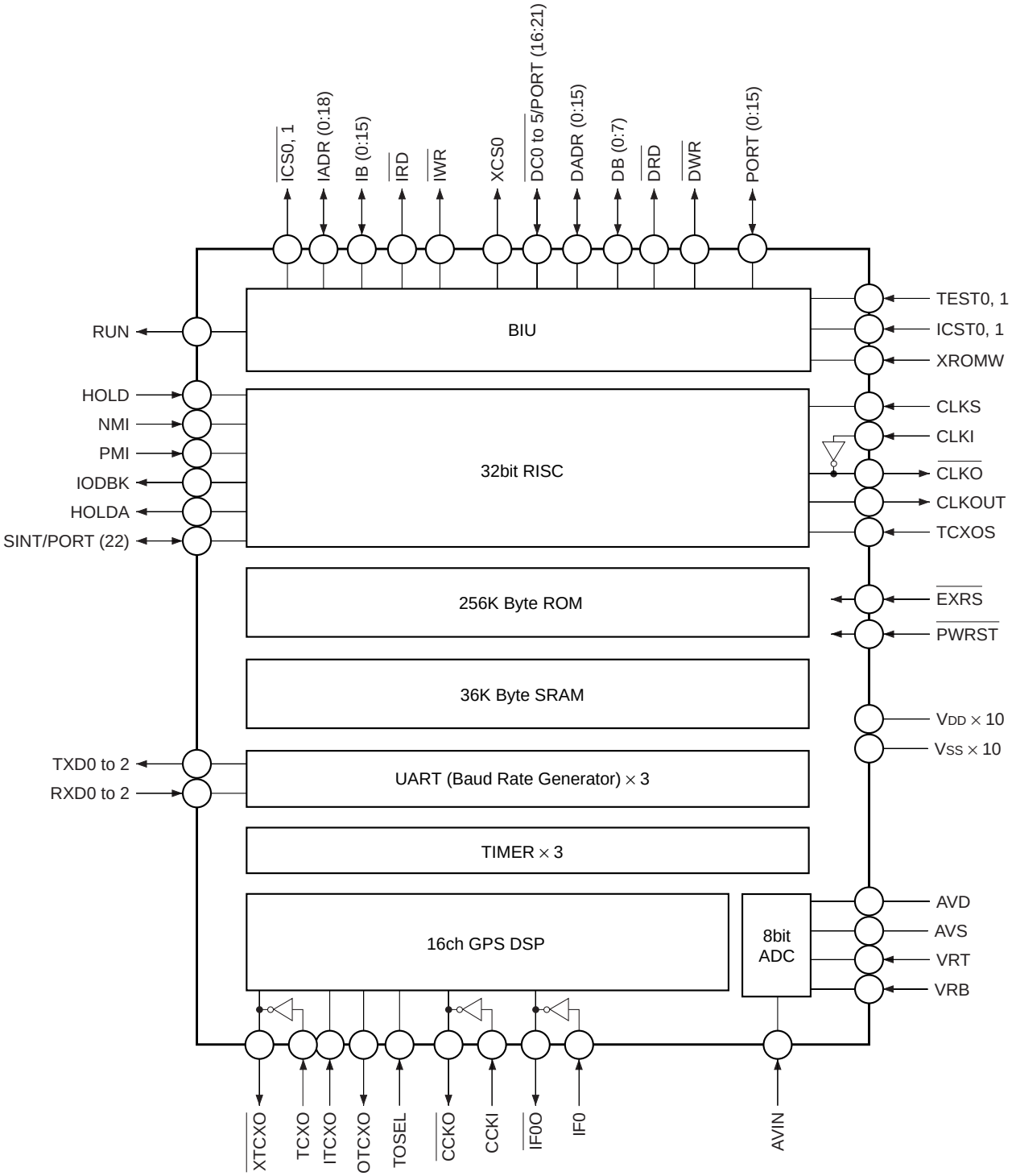
- 16-channel GPS receiver
- High performance 32-bit RISC CPU
- Reception frequency 1575.42MHz (L1 band, CA code)
- Reception sensitivity (using the CXA1951AQ in the RF block)
  –130dBm or less
- Time to first fix* (time until initial measurement after power-on)
  - Cold Start (without ephemeris and almanac) 35 to 60s
  - Warm Start (without ephemeris with almanac) 33 to 50s
  - Hot Start (with ephemeris and almanac) 6 to 20s
  - Reacquisition Time (interrupt recovery time) Less than 5 minutes: < 3 to 6s
    5 minutes or more: < 6 to 10s
- Positioning accuracy
  - Stand alone (GPS unit only) 1σ: < 30m
    3σ: < 90m
  - D-GPS (differential GPS) 1σ: < 6m
    3σ: < 18m
- Measurement data update time Every 1s
- Communication method Sony standard serial communication
  Supports NMEA-0183
- All-in-view measurement
- 2-satellite measurement
- High performance 32-bit RISC CPU

* The noted values may be exceeded depending on the operating environment and other conditions.

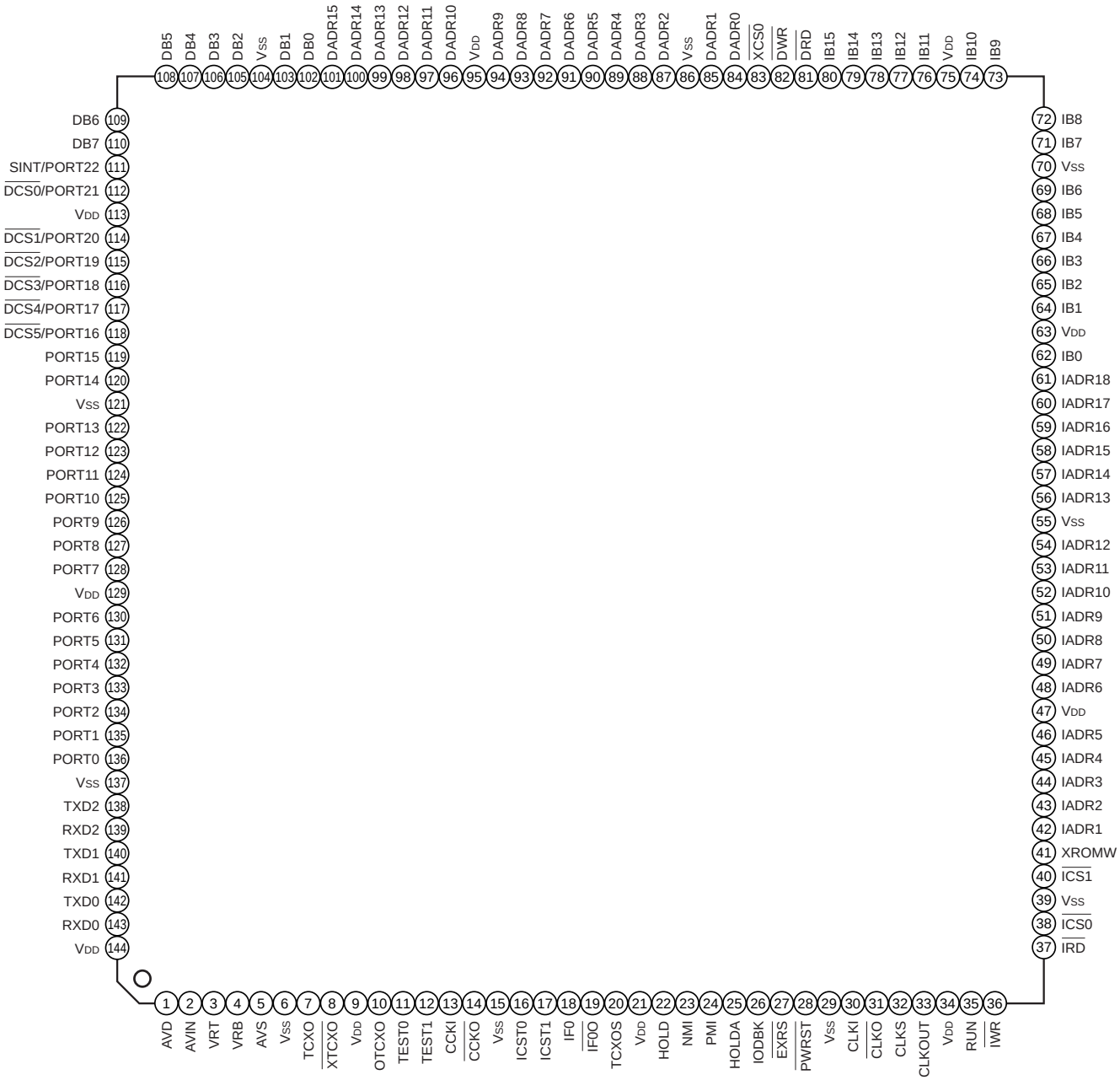


GPS receiver system diagram using the CXD2931R

Block Diagram



Pin Configuration



Pin Configuration

Pin No.	Symbol	I/O	Description
1	AVD	—	A/D converter power supply.
2	AVIN	I	Analog input.
3	VRT	I	Reference input.
4	VRB	I	
5	AVS	—	A/D converter GND.
6	V_{SS}	—	GND
7	TCXO	I	TCXO binary conversion circuit/crystal oscillator.
8	$\overline{XTCXO}$	O	
9	V_{DD}	—	Power supply.
10	OTCXO	O	TCXO clock output.
11	TEST0	I	Test. (Low level fixed)
12	TEST1	I	
13	CCKI	I	Timer oscillation. (32.768kHz ± 100ppm)
14	$\overline{CCKO}$	O	
15	V_{SS}	—	GND
16	ICST0	I	Test. (Low level fixed)
17	ICST1	I	
18	IF0	I	IF signal binary conversion circuit.
19	IF0O	O	
20	TCXOS	I	TCXO select. (Low: TCXO/2, High: TCXO through)
21	V_{DD}	—	Power supply.
22	HOLD	I	Hold input signal. (High: Hold)
23	NMI	I	Non maskable interrupt.
24	PMI	I	Program maskable interrupt.
25	HOLDA	O	Hold acknowledge signal.
26	IODBK	O	Break signal for debugging.
27	EXRS	I	Reset input signal.
28	PWRST	I	Connect to main power supply. Leave open during backup.
29	V_{SS}	—	GND
30	CLKI	I	CPU clock oscillation circuit.
31	$\overline{CLKO}$	O	
32	CLKS	I	CPU clock select signal. (Low: TCXO, High: CLKI)
33	CLKOUT	O	CPU clock output.
34	V_{DD}	—	Power supply.
35	RUN	O	Signal indicating CPU operating status.

Pin No.	Symbol	I/O	Description
36	IWR	O	Write signal for external expansion memory.
37	IRD	O	Read signal for external expansion memory.
38	ICS0	O	Chip select 0 for external expansion memory.
39	V_{SS}	—	GND
40	ICS1	O	Chip select 1 for external expansion memory.
41	XROMW	I	Wait signal for external expansion memory. (High: Wait)
42	IADR1	I/O	(LSB)
43	IADR2	I/O	
44	IADR3	I/O	Address signal for external expansion memory.
45	IADR4	I/O	
46	IADR5	I/O	
47	V_{DD}	—	Power supply.
48	IADR6	I/O	
49	IADR7	I/O	
50	IADR8	I/O	
51	IADR9	I/O	Address signal for external expansion memory.
52	IADR10	I/O	
53	IADR11	I/O	
54	IADR12	I/O	
55	V_{SS}	—	GND
56	IADR13	I/O	
57	IADR14	I/O	
58	IADR15	I/O	Address signal for external expansion memory.
59	IADR16	I/O	
60	IADR17	I/O	
61	IADR18	I/O	(MSB)
62	IB0	I/O	(LSB) Data bus I/O for external expansion memory.
63	V_{DD}	—	Power supply.
64	IB1	I/O	
65	IB2	I/O	
66	IB3	I/O	Data bus I/O for external expansion memory.
67	IB4	I/O	
68	IB5	I/O	
69	IB6	I/O	
70	V_{SS}	—	GND

Pin No.	Symbol	I/O	Description
71	IB7	I/O	Data bus I/O for external expansion memory.
72	IB8	I/O	
73	IB9	I/O	
74	IB10	I/O	
75	V_{DD}	—	Power supply.
76	IB11	I/O	Data bus I/O for external expansion memory.
77	IB12	I/O	
78	IB13	I/O	
79	IB14	I/O	
80	IB15	I/O	(MSB)
81	DRD	O	Read signal for external expansion data memory.
82	DWR	O	Write signal for external expansion data memory.
83	XCS0	O	Chip select signal for external expansion data memory.
84	DADR0	I/O	(LSB)
85	DADR1	I/O	Address signal for external expansion data memory.
86	V_{SS}	—	GND
87	DADR2	I/O	Address signal for external expansion data memory.
88	DADR3	I/O	
89	DADR4	I/O	
90	DADR5	I/O	
91	DADR6	I/O	
92	DADR7	I/O	
93	DADR8	I/O	
94	DADR9	I/O	
95	V_{DD}	—	Power supply.
96	DADR10	I/O	Address signal for external expansion data memory.
97	DADR11	I/O	
98	DADR12	I/O	
99	DADR13	I/O	
100	DADR14	I/O	
101	DADR15	I/O	(MSB)
102	DB0	I/O	(LSB)
103	DB1	I/O	Data bus I/O for external expansion data memory.
104	V_{SS}	—	GND

Pin No.	Symbol	I/O	Description
105	DB2	I/O	Data bus I/O for external expansion data memory.
106	DB3	I/O	
107	DB4	I/O	
108	DB5	I/O	
109	DB6	I/O	
110	DB7	I/O	(MSB)
111	SINT/PORT22	I/O	External interrupt input signal/general-purpose I/O port. This pin can be used as a general-purpose I/O port according to the internal registers.
112	$\overline{\text{DCS0}}$/PORT21	I/O	Chip select for external expansion data memory/general-purpose I/O port. This pin can be used as a general-purpose I/O port according to the internal registers.
113	V_{DD}	—	Power supply.
114	$\overline{\text{DCS1}}$/PORT20	I/O	Chip select for external expansion data memory/general-purpose I/O port. These pins can be used as a general-purpose I/O port according to the internal registers.
115	$\overline{\text{DCS2}}$/PORT19	I/O	
116	$\overline{\text{DCS3}}$/PORT18	I/O	
117	$\overline{\text{DCS4}}$/PORT17	I/O	
118	$\overline{\text{DCS5}}$/PORT16	I/O	
119	PORT15	I/O	General-purpose I/O port.
120	PORT14	I/O	
121	V_{SS}	—	GND
122	PORT13	I/O	General-purpose I/O port.
123	PORT12	I/O	
124	PORT11	I/O	
125	PORT10	I/O	
126	PORT9	I/O	
127	PORT8	I/O	
128	PORT7	I/O	
129	V_{DD}	—	Power supply.
130	PORT6	I/O	General-purpose I/O port.
131	PORT5	I/O	
132	PORT4	I/O	
133	PORT3	I/O	
134	PORT2	I/O	
135	PORT1	I/O	
136	PORT0	I/O	
137	V_{SS}	—	GND
138	TXD2	O	UART transmission data output (channel 2)

Pin No.	Symbol	I/O	Description
139	RXD2	I	UART reception data input (channel 2)
140	TXD1	O	UART transmission data output (channel 1)
141	RXD1	I	UART reception data input (channel 1)
142	TXD0	O	UART transmission data output (channel 0)
143	RXD0	I	UART reception data input (channel 0)
144	V_{DD}	—	Power supply.

Electrical Characteristics

DC Characteristics

(V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1) (CMOS level)	High level	V_{IH} (1)		0.7 × V_{DD}		V_{DD}	V	*1
	Low level	V_{IL} (1)				0.2 × V_{DD}	V	
Input voltage (2) (5V interface)	High level	V_{IH} (2)		0.7 × V_{DD}		5.5	V	*2
	Low level	V_{IL} (2)				0.2 × V_{DD}	V	
Output voltage (1)	High level	V_{OH} (1)	I_{OH} = –4.0mA	V_{DD} – 0.4			V	*3
	Low level	V_{OL} (1)	I_{OL} = 4.0mA			0.4	V	
Output voltage (2)	High level	V_{OH} (2)	I_{OH} = –8.0mA	V_{DD} – 0.4			V	*4
	Low level	V_{OL} (2)	I_{OL} = 8.0mA			0.4	V	
Output voltage (3)	High level	V_{OH} (3)	I_{OH} = –12.0mA	V_{DD} – 0.4			V	*5
	Low level	V_{OL} (3)	I_{OL} = 12.0mA			0.4	V	
Current consumption in standby mode		ISTB	V_{DD} = 3.0V		20	70	µA	—
			V_{DD} = 1.8V		4	50		
Supply current		I_{DD}	f = 18.414MHz		55		mA	—

Applicable pins

*1 Pins 11, 12, 16, 17, 20, 22 to 24, 32, 41

*2 Pins 62, 64 to 69, 72 to 74, 76 to 80, 84, 85, 87 to 94, 96 to 103, 105 to 112, 114 to 120, 122, 128, 130 to 136, 139, 141, 143

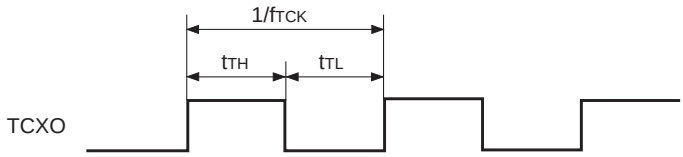
*3 Pins 10, 25, 26, 33, 35, 42 to 46, 48 to 54, 56 to 61, 81 to 83, 138, 140, 142

*4 Pins 38, 40, 62, 64 to 69, 71 to 74, 76 to 80, 84, 85, 87 to 94, 96 to 103, 105 to 112, 114 to 120, 122 to 128, 130 to 136

*5 Pins 36, 37

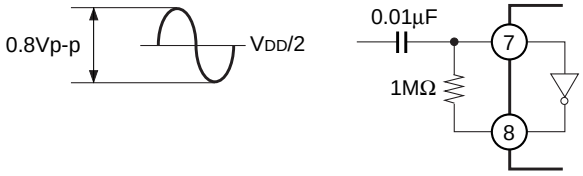
AC Characteristics

(1) When inputting a pulse to the TCXO pin (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)



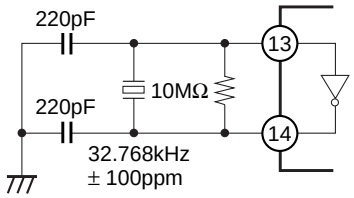
When inputting a binary-converted signal

Item	Symbol	Min.	Typ.	Max.	Unit
TCXO clock frequency	f_{TCK}	Typ. – 3ppm	18.414	Typ. + 3ppm	MHz
TCXO clock pulse width	t_{TH}, t_{TL}	10			ns



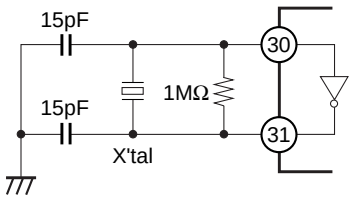
When performing binary conversion with the TCXO and $\overline{\text{XTCXO}}$ pins (Pins 7 and 8)

(2) When performing self-oscillation with the CCKI and $\overline{\text{CCKO}}$ pins (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)



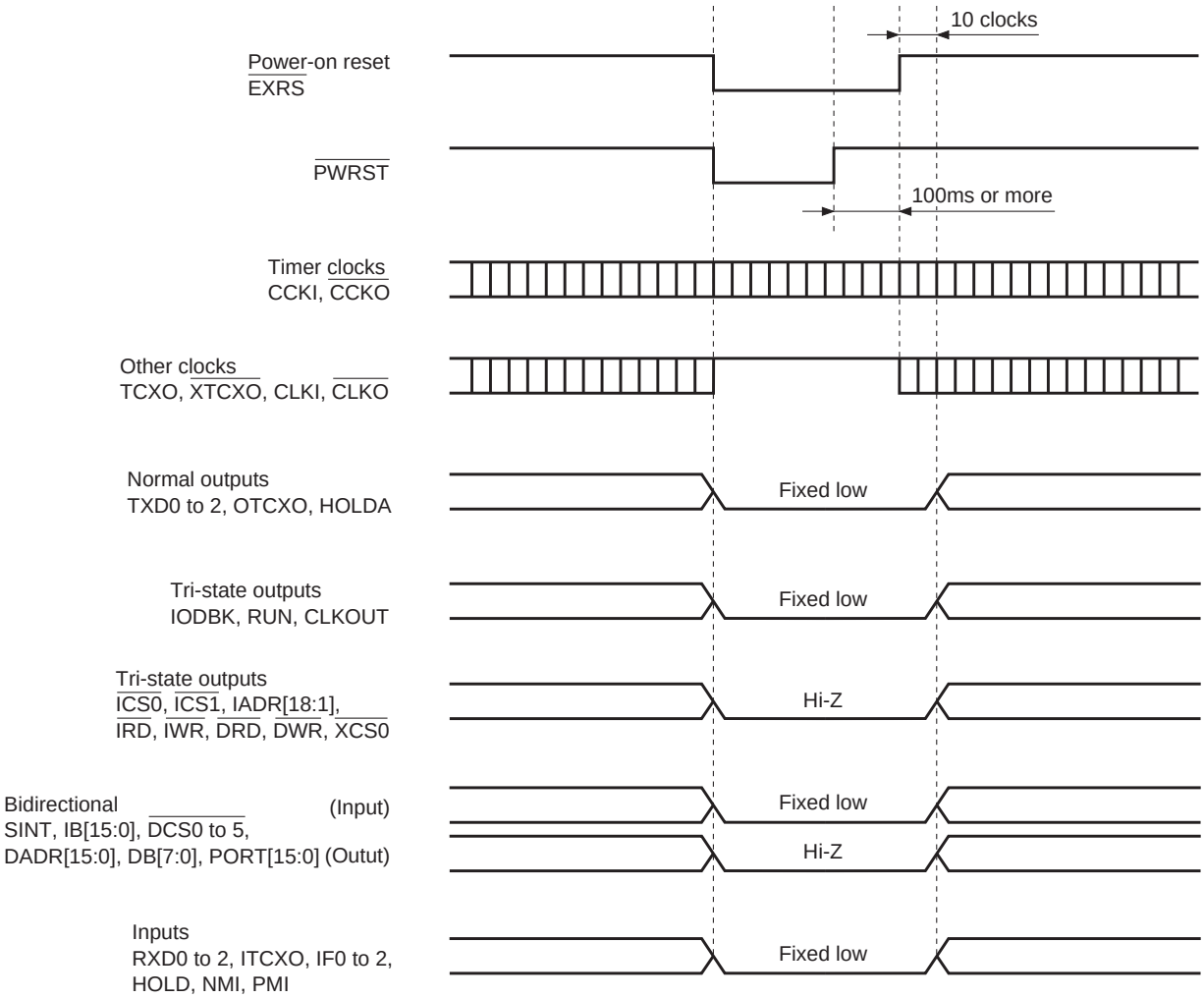
(3) IF signal input (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)

(4) When performing self-oscillation with the MCKI, $\overline{\text{MCKO}}$ pins (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)



Battery Backup Mode

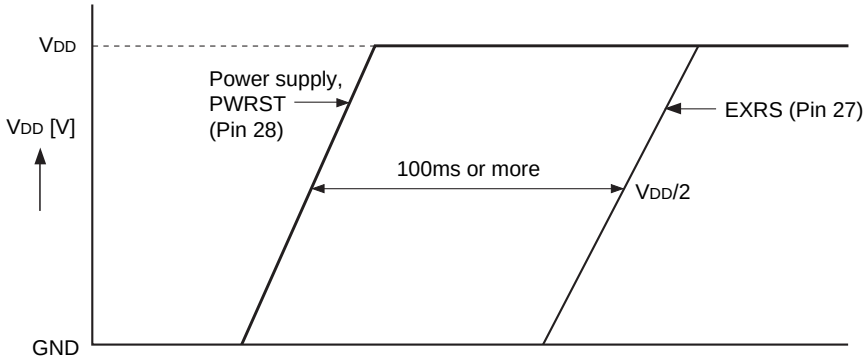
The battery backup mode is activated when the power for the GPS receiver is turned off and power-on reset goes to low level. The timer clock continues to operate even when power-on reset goes low, but all other clock are fixed high and the LSI is set to the low power consumption mode. At this time, the RAM data is held and the registers are initialized.
Battery backup mode is canceled by setting power-on reset to high.



CXD2931R Initialization

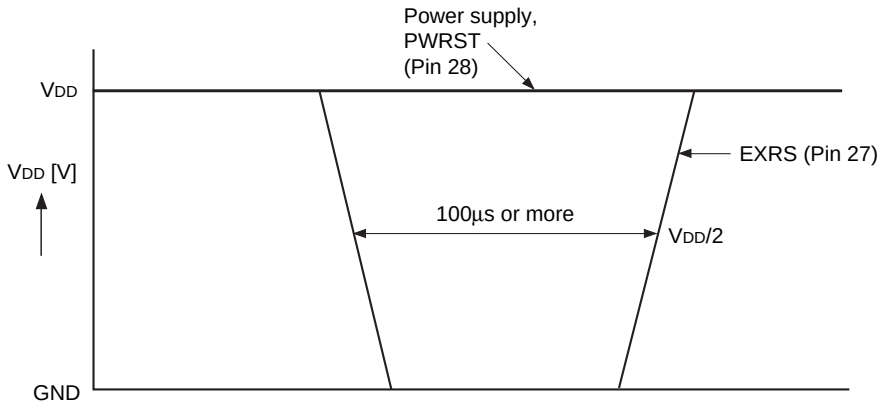
CXD2931R initialization is started by setting the reset input signal EXRS (Pin 27) to low level. The timing should satisfy the conditions noted below.

1. During power-on (power-on reset) (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)



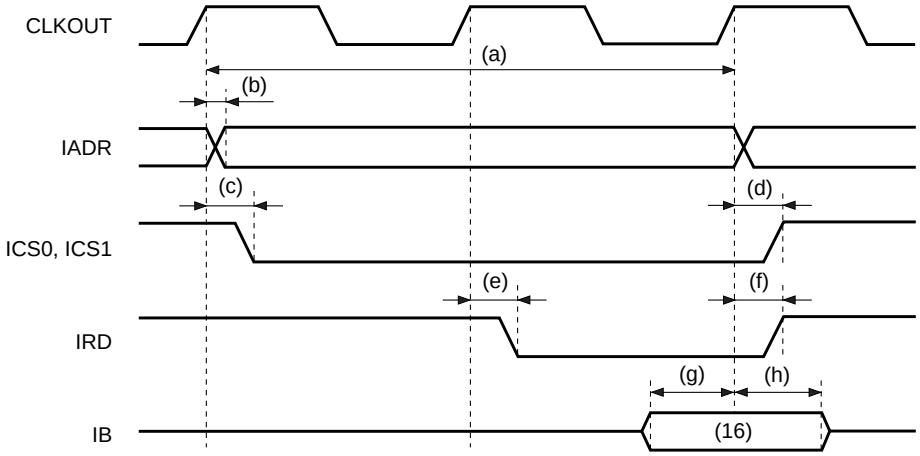
The PWRST (Pin 28) signal should rise simultaneously with the power supply. The EXRS (Pin 27) signal should rise 100ms or more after the power supply and the PWRST signal have risen. Note that the PWRST signal should be left open during battery backup.

2. Initialization during operation (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)



The internal registers can be initialized during operation by setting the EXRS (Pin 27) signal to low level for 100µs or more.
Keep the PWRST (Pin 28) signal at high level at this time.

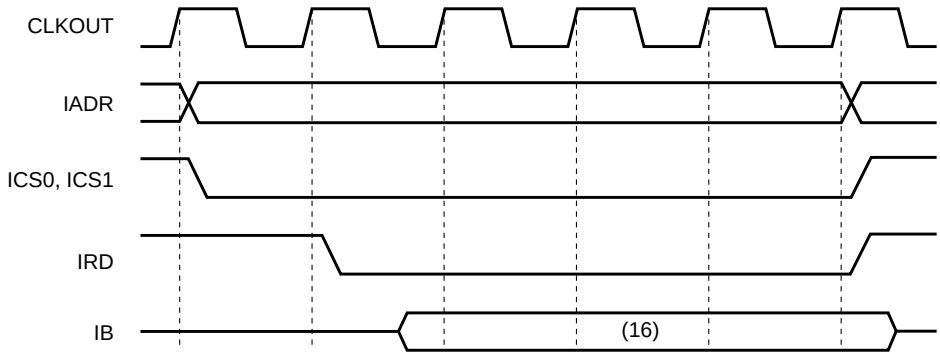
• External Command Fetch Timing (XROMW = 0)



No.	Item	Min.	Typ.	Max.	Unit
(a)	Read cycle time (Fex: @20MHz)	—	100	—	ns
(b)	Address delay time	—	—	5	ns
(c)	Chip select fall delay time	2	—	10	ns
(d)	Chip select rise delay time	2	—	9	ns
(e)	Read signal fall delay time	1	—	3	ns
(f)	Read signal rise delay time	1	—	5	ns
(g)	Read data setup time	23	—	—	ns
(h)	Read data hold time	0	—	—	ns

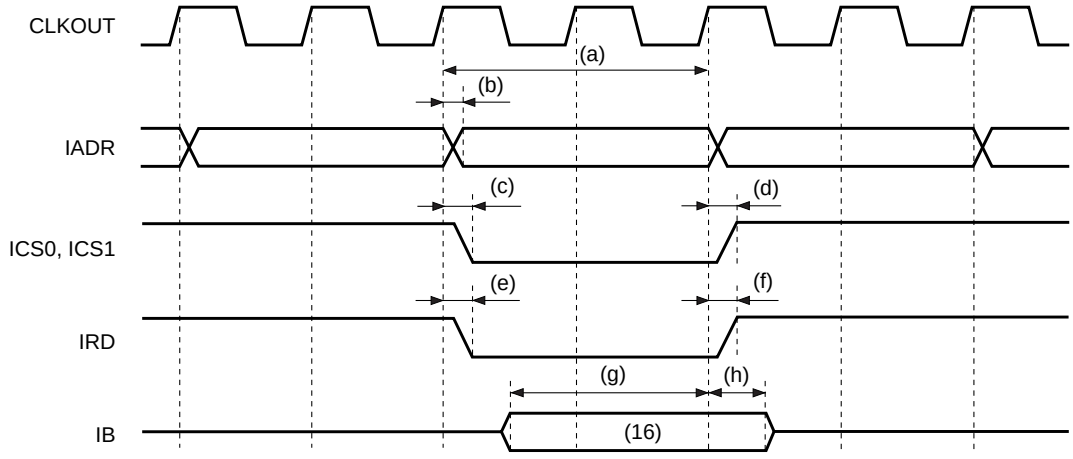
* The load capacitance = 30pF.

• External Command Fetch Timing (XROMW = 1)

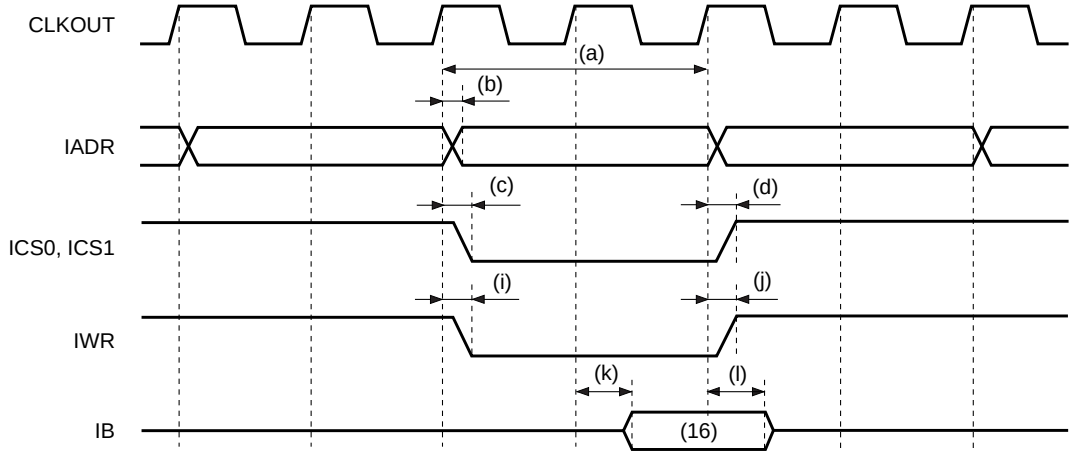


• External Data Access Timing (ICS0, ICS1/XROMW = 0)

(1) Read (half-word access/XROMW = 0)



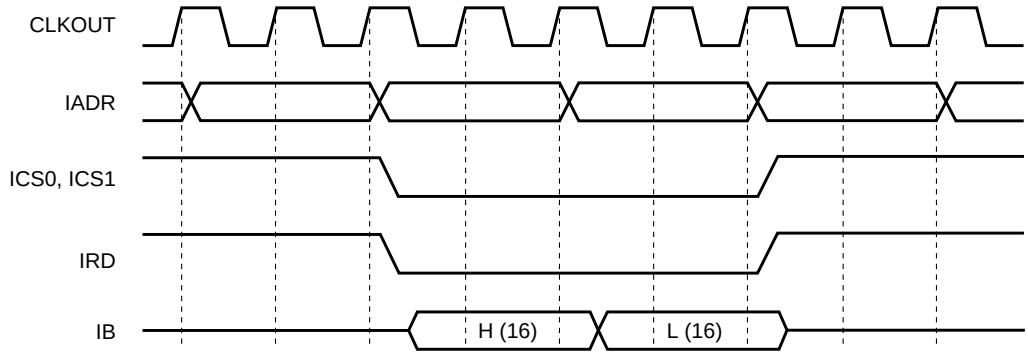
(2) Write (half-word access/XROMW = 0)



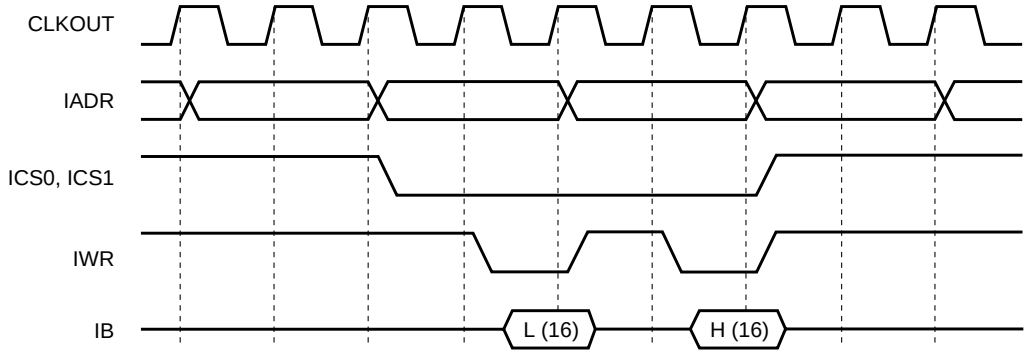
No.	Item	Min.	Typ.	Max.	Unit
(a)	Read/write cycle time (Fex: @20MHz)	—	100	—	ns
(b)	Address delay time	—	—	5	ns
(c)	Chip select fall delay time	2	—	10	ns
(d)	Chip select rise delay time	2	—	9	ns
(e)	Read signal fall delay time	1	—	3	ns
(f)	Read signal rise delay time	1	—	5	ns
(g)	Read data setup time	23	—	—	ns
(h)	Read data hold time	0	—	—	ns
(i)	Write signal fall delay time	0	—	1	ns
(j)	Write signal rise delay time	0	—	2	ns
(k)	Write data established time	—	—	5	ns
(l)	Write data hold time	5	—	—	ns

* The load capacitance = 30pF.

(3) Read (word access/XROMW = 0)

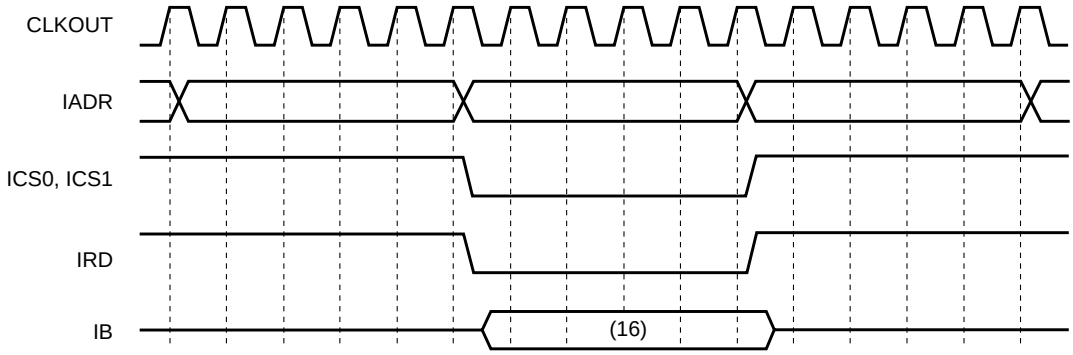


(4) Write (word access/XROMW = 0)

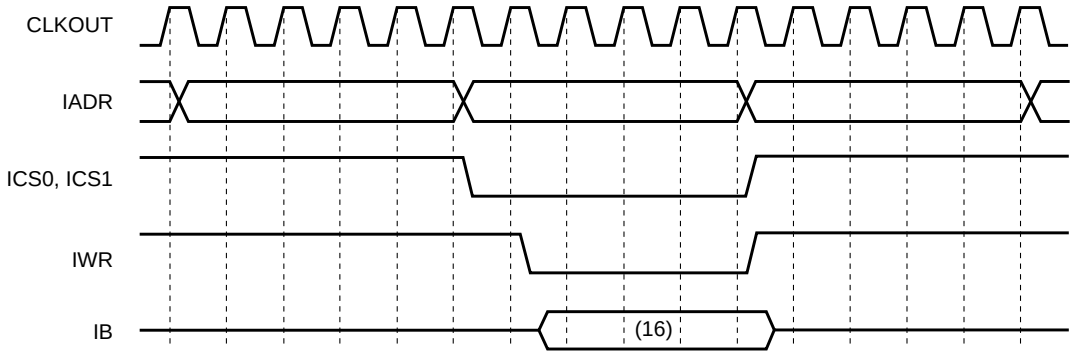


• External Data Access Timing (ICS0, ICS1/XROMW = 1)

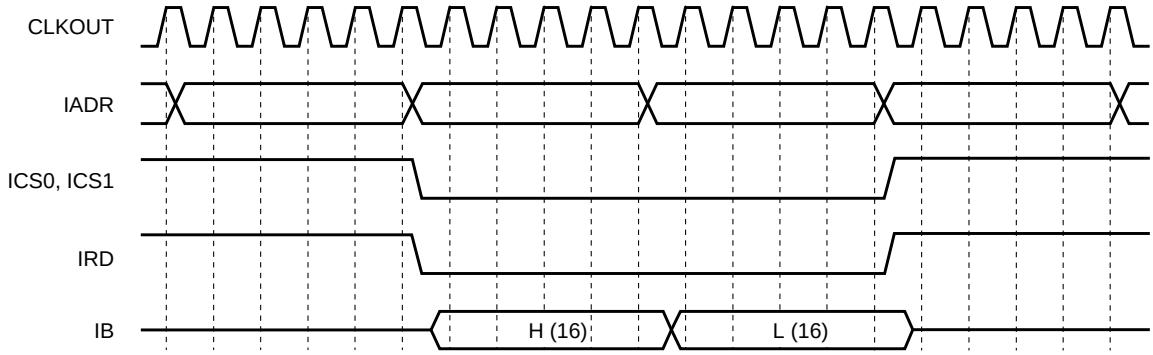
(1) Read (half-word access/XROMW = 1)



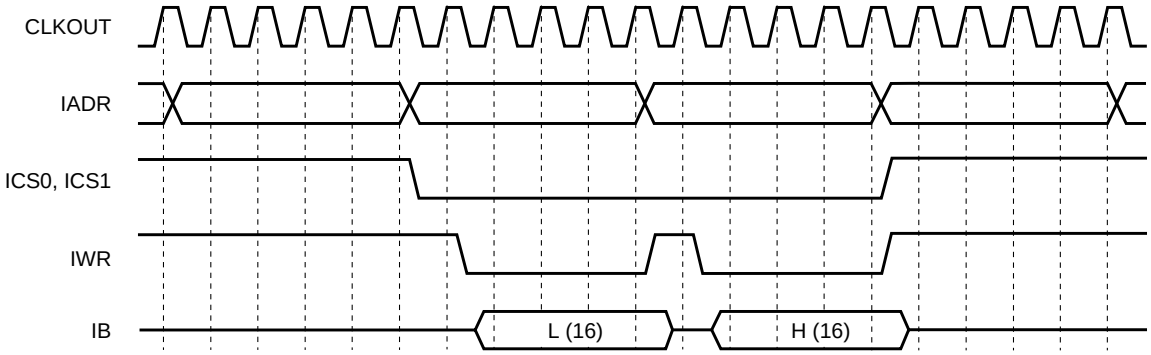
(2) Write (half-word access/XROMW = 1)



(3) Read (word access/XROMW = 1)

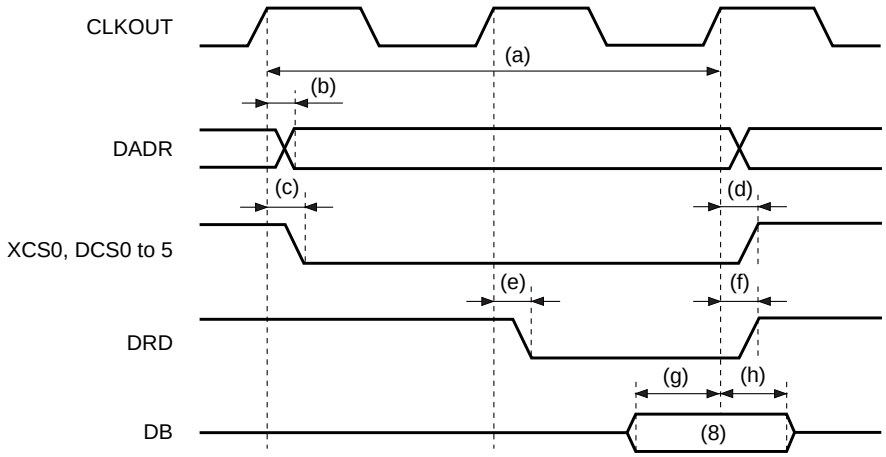


(4) Write (word access/XROMW = 1)

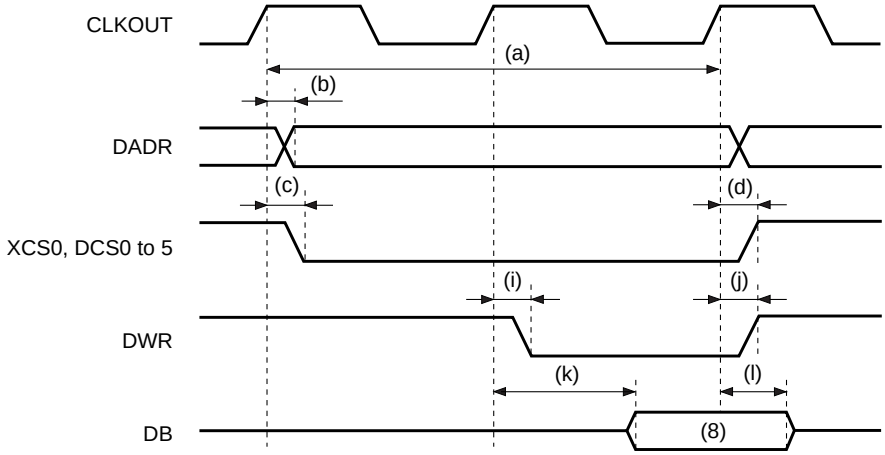


• External Data Access Timing (XCS0, DCS0 to 5/no data wait)

(1) Read (byte access/no data wait)



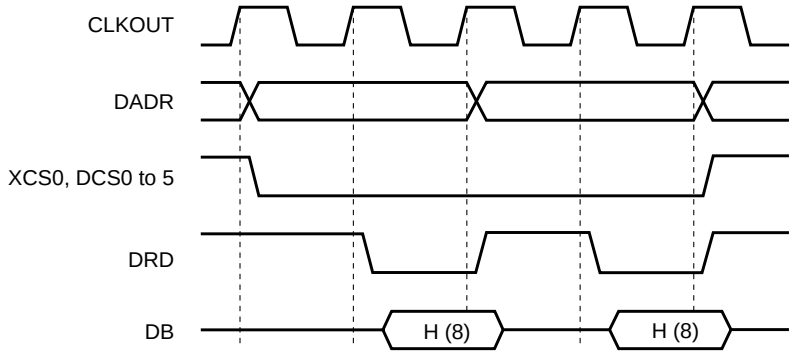
(2) Write (byte access/no data wait)



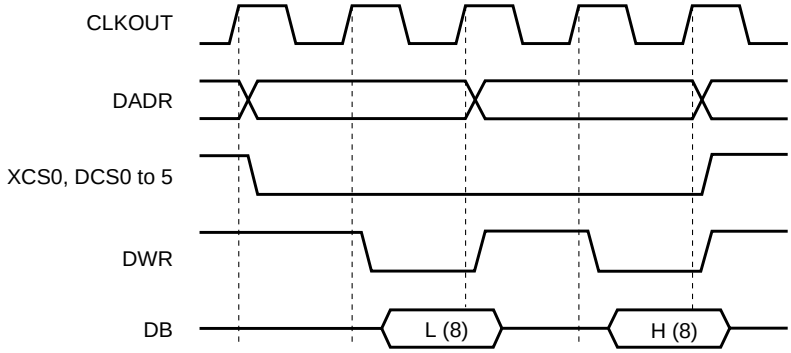
No.	Item	Min.	Typ.	Max.	Unit
(a)	Read/write cycle time (Fex: @20MHz)	—	100	—	ns
(b)	Address delay time	—	—	9	ns
(c)	Chip select fall delay time	4	—	13	ns
(d)	Chip select rise delay time	4	—	13	ns
(e)	Read signal fall delay time	2	—	8	ns
(f)	Read signal rise delay time	3	—	10	ns
(g)	Read data setup time	16	—	—	ns
(h)	Read data hold time	0	—	—	ns
(i)	Write signal fall delay time	0	—	1	ns
(j)	Write signal rise delay time	0	—	2	ns
(k)	Write data established time	—	—	7	ns
(l)	Write data hold time	5	—	—	ns

* The load capacitance = 30pF.

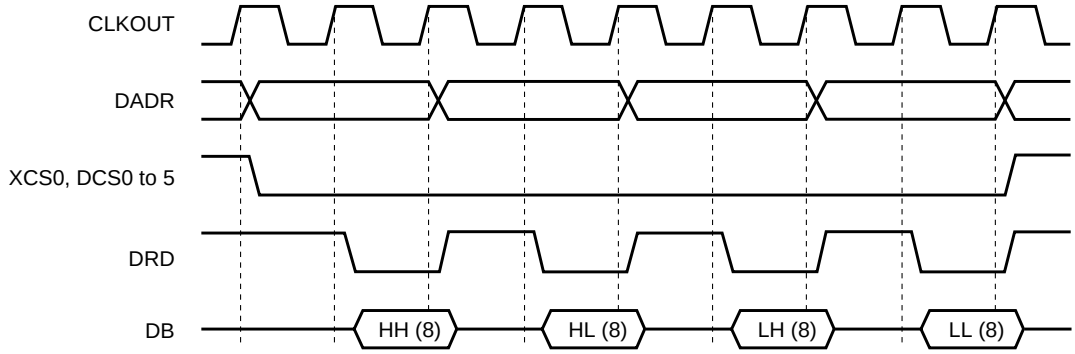
(3) Read (half-word access/no data wait)



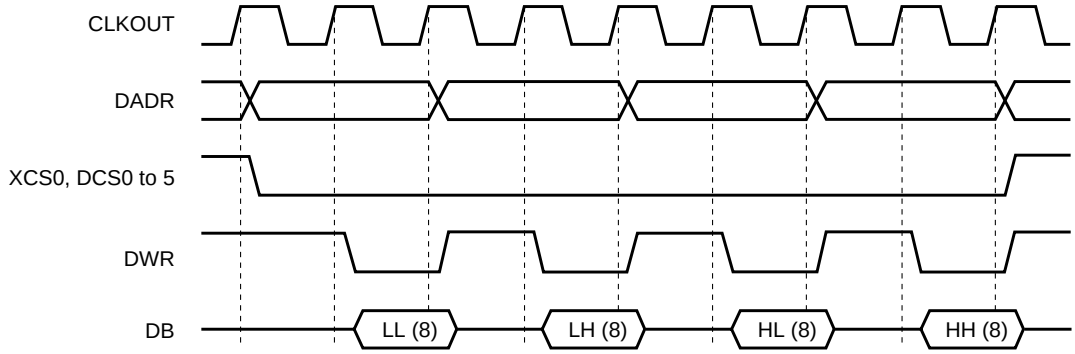
(4) Write (half-word access/no data wait)



(5) Read (word access/no data wait)

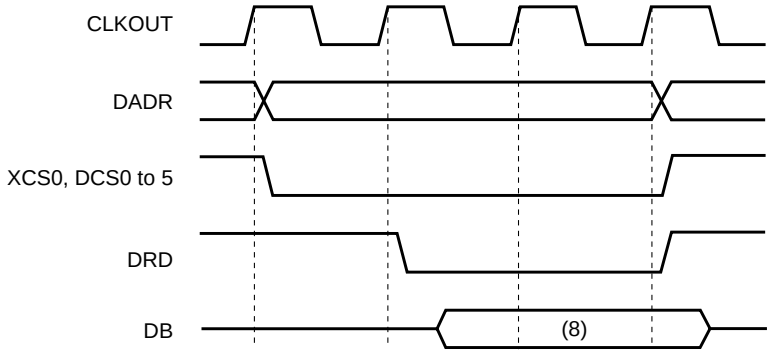


(6) Write (word access/no data wait)

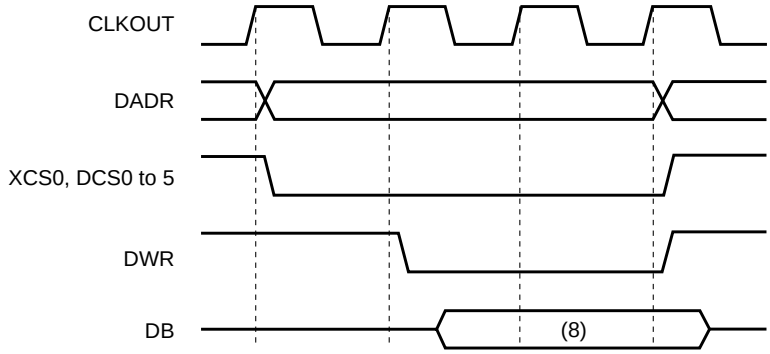


• External Data Access Timing (XCS0, DCS0 to 5/data wait = 1)

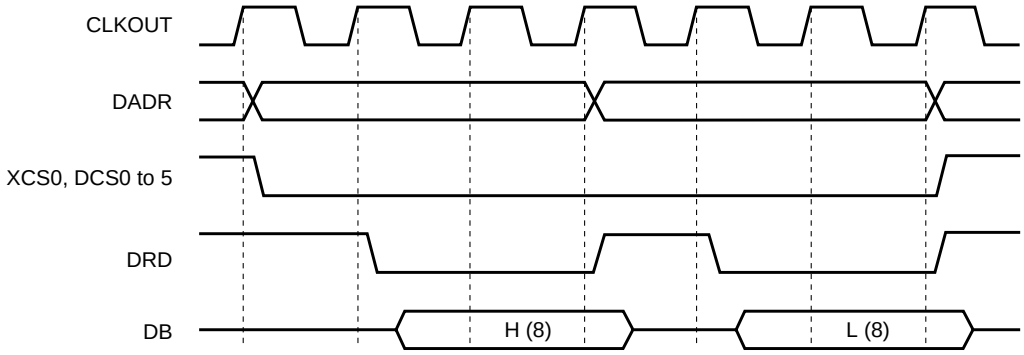
(1) Read (byte access/data wait = 1)



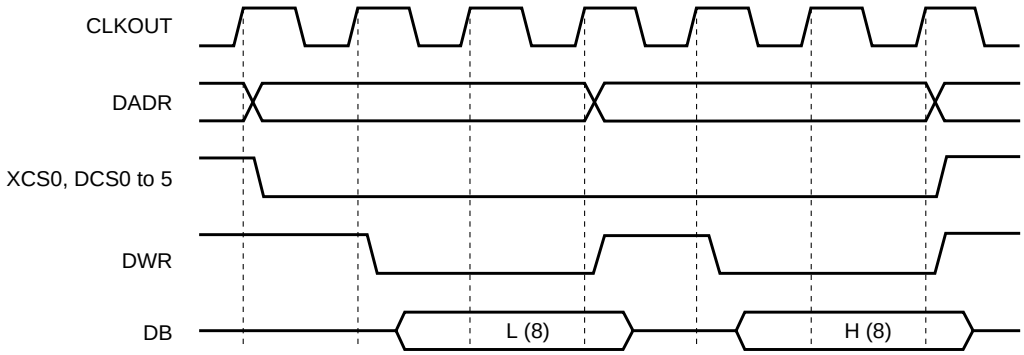
(2) Write (byte access/data wait = 1)



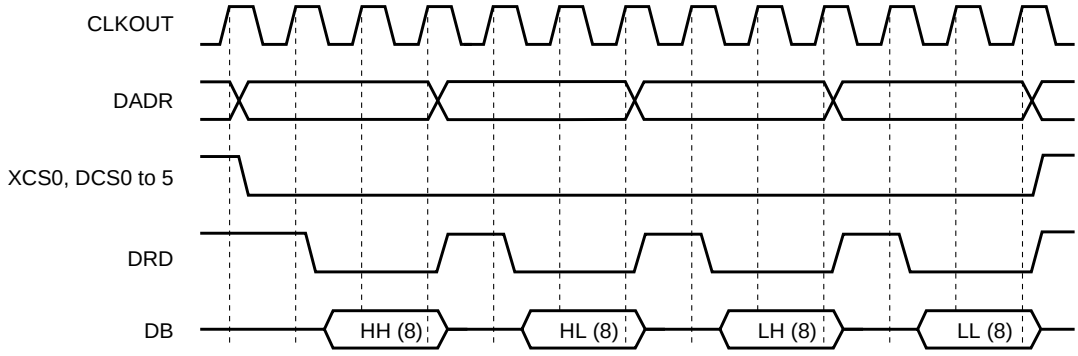
(3) Read (half-word access/data wait = 1)



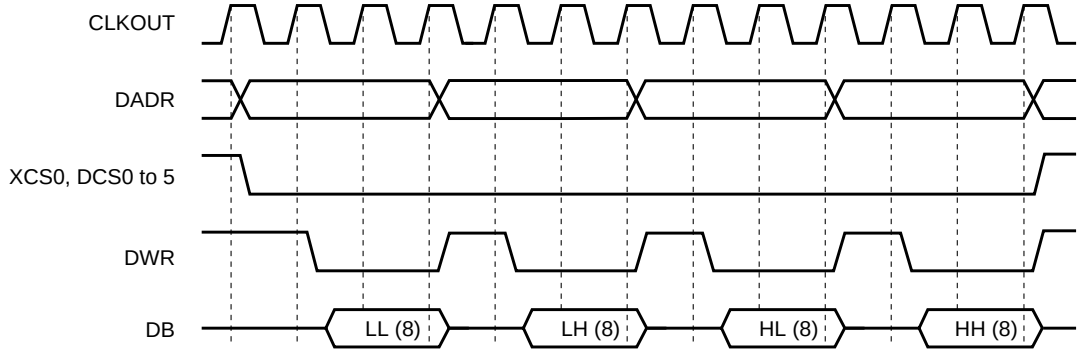
(4) Write (half-word access/data wait = 1)



(5) Read (word access/data wait = 1)

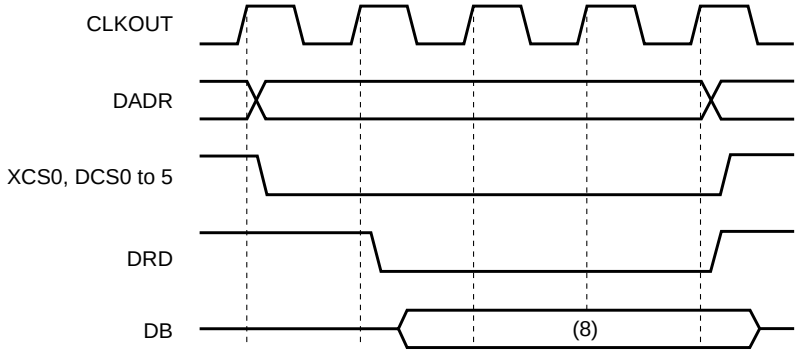


(6) Write (word access/data wait = 1)

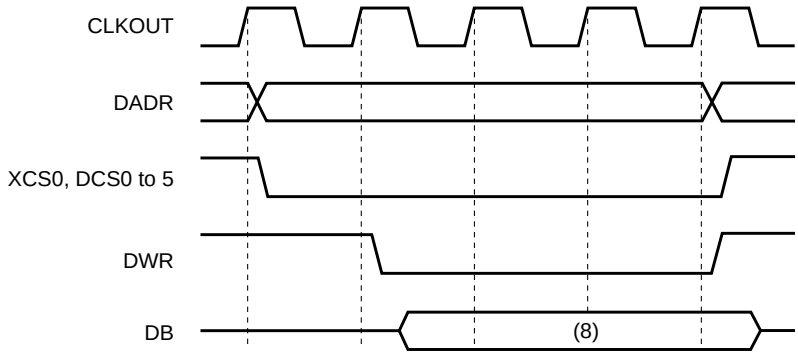


• External Data Access Timing (XCS0, DCS0 to 5/data wait = 2)

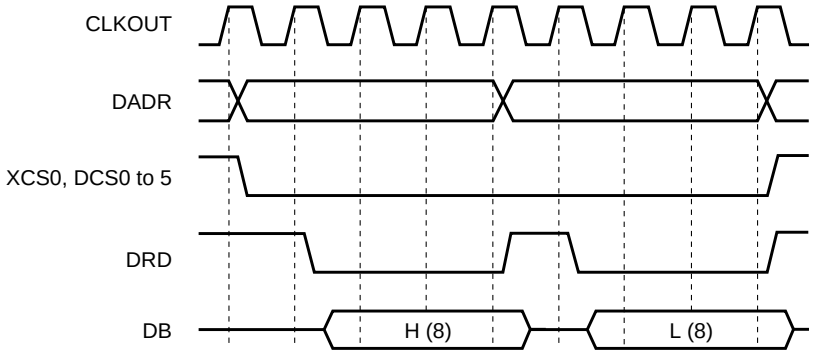
(1) Read (byte access/data wait = 2)



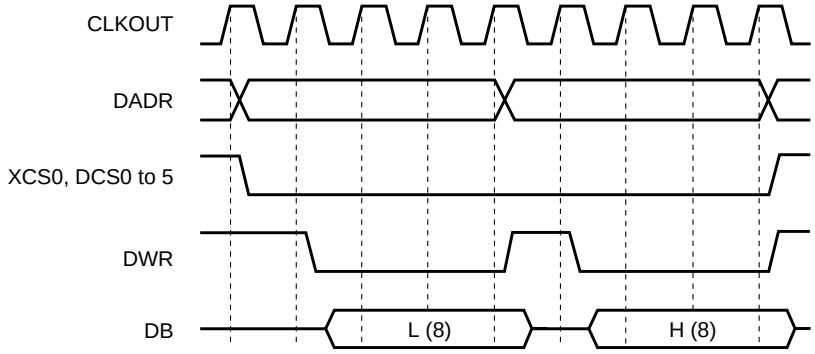
(2) Write (byte access/data wait = 2)



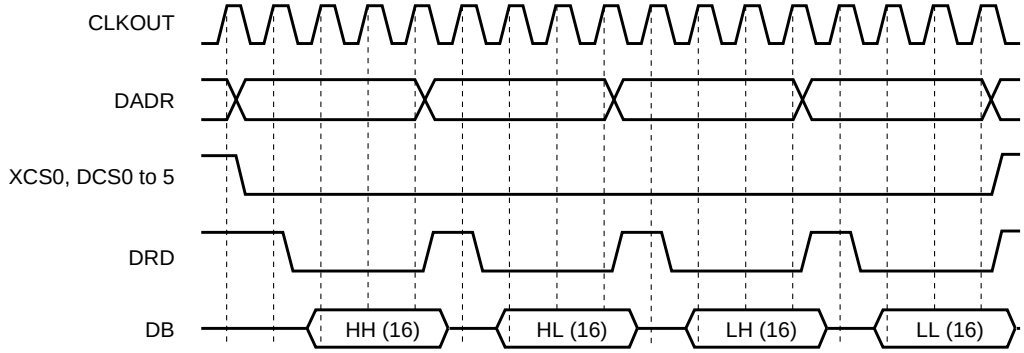
(3) Read (half-word access/data wait = 2)



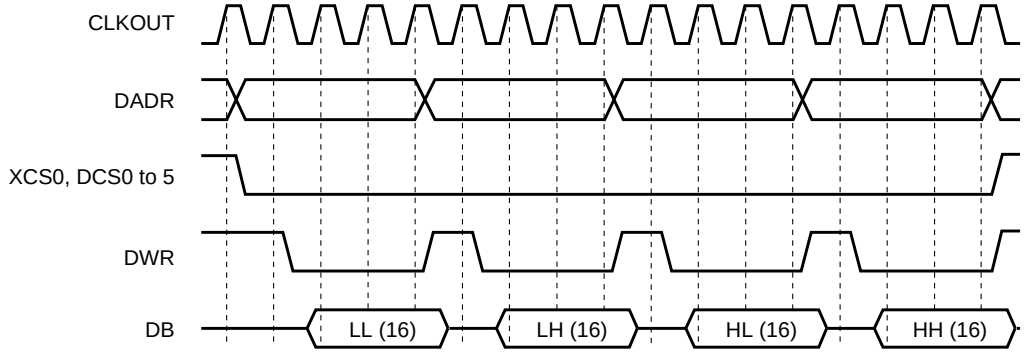
(4) Write (half-word access/data wait = 2)



(5) Read (word access/data wait = 2)

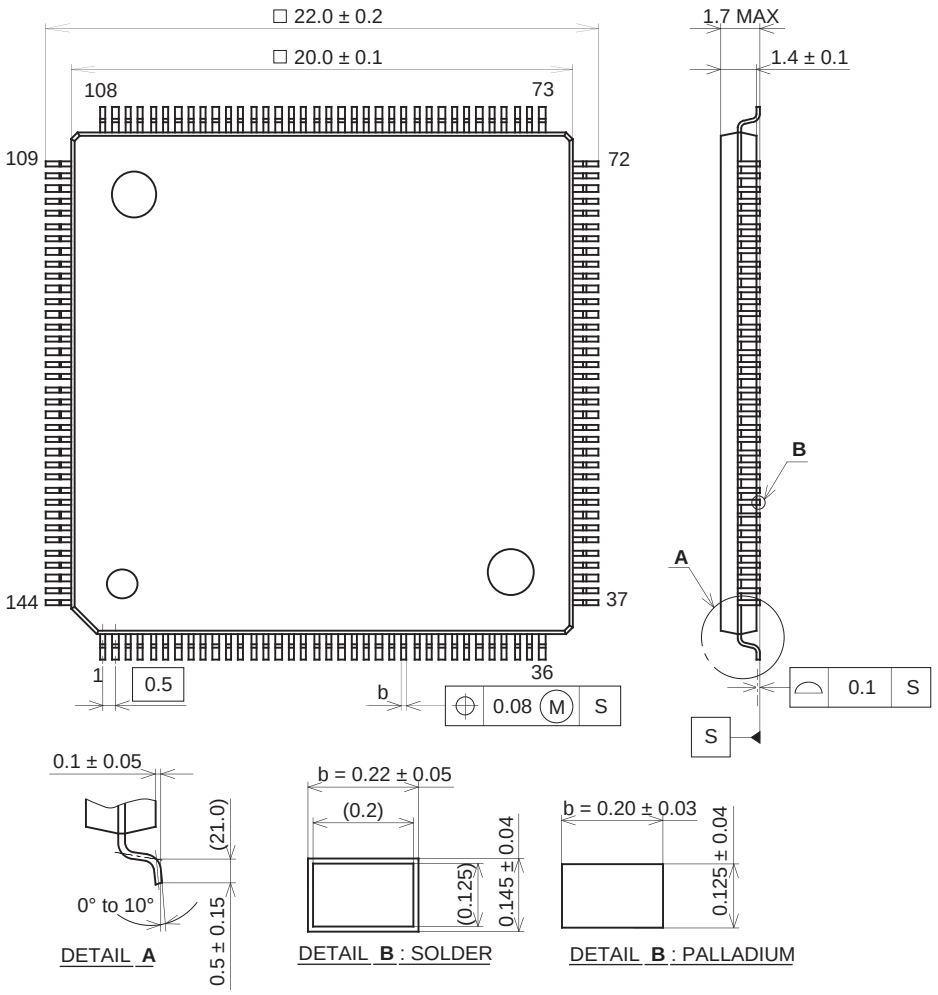


(6) Write (word access/data wait = 2)



Package Outline Unit: mm

144PIN LQFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	LQFP-144P-L01
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.3 g