SONY

CXP844P16

## CMOS 8-bit Single Chip Microcomputer

Description

The CXP844P16 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, 32kHz timer/counter, remote control reception circuit and other servo systems besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

The CXP844P16 also provides and a sleep/stop function that enables lower power consumption.

This IC is the PROM-incorporated version of the CXP84416 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.
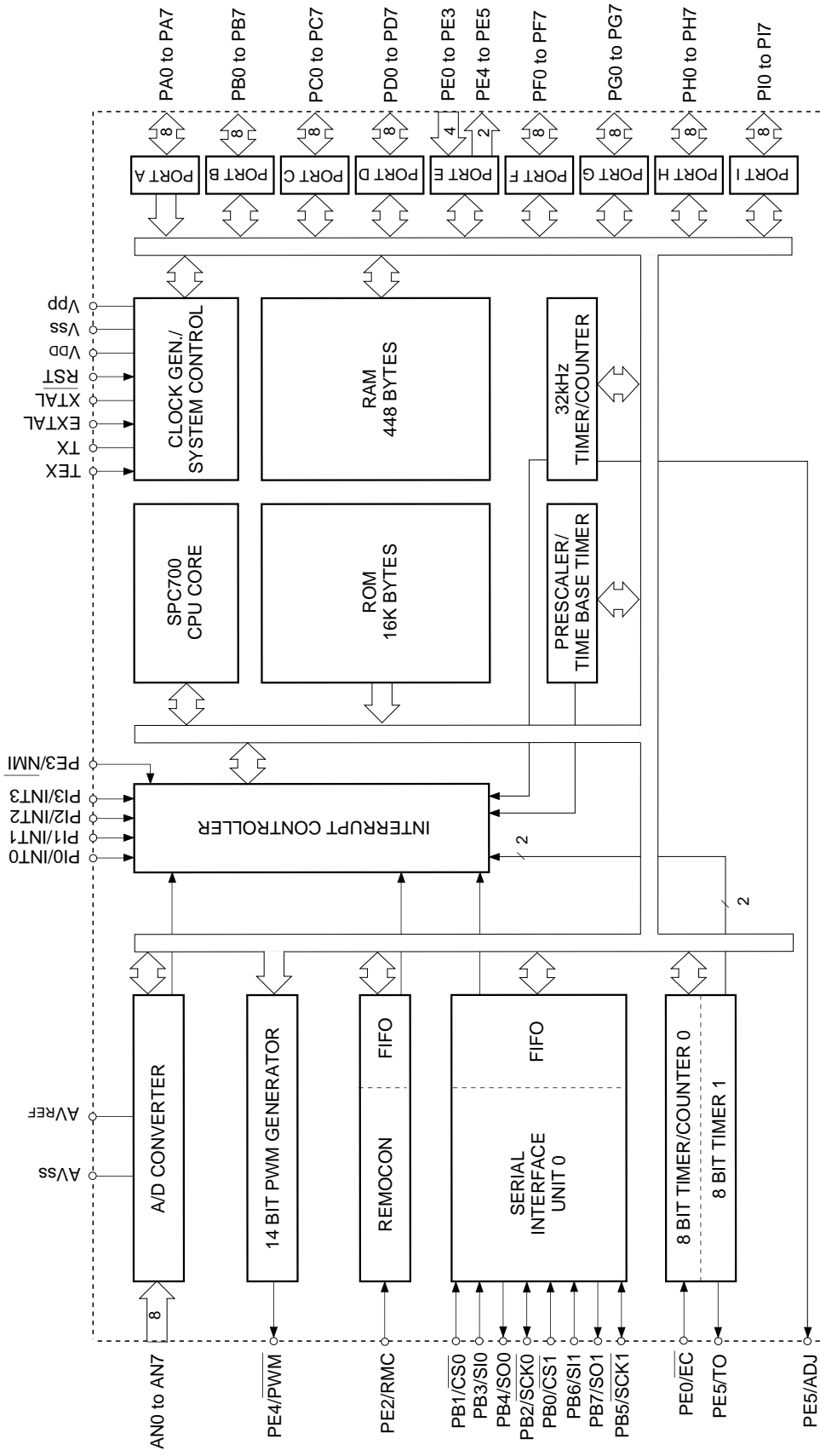
80 pin QFP (Plastic)
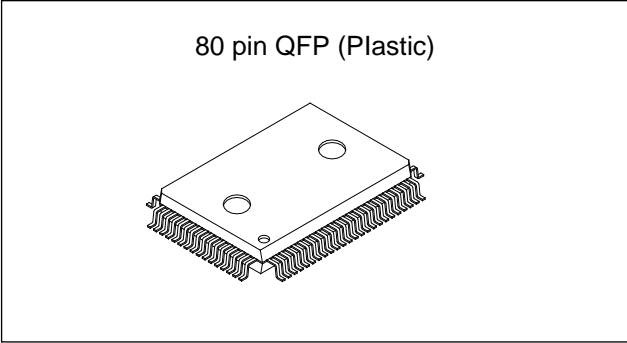
Features

- Wide-range instruction system (213 instructions) to cover various types of data.
  — 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle   400ns at 10MHz operation
                                    122µs at 32kHz operation
- Incorporated PROM capacity   16Kbytes
- Incorporated RAM capacity   448bytes
- Peripheral functions
  — A/D converter   8-bit, 8-channel, successive approximation method
                                    (Conversion time of 32µs/10MHz)
  — Serial interface   Incorporated 8-bit, 8-stage FIFO
                                    (Auto transfer for 1 to 8 bytes), 2 channel
  — Timer   8-bit timer, 8-bit timer/counter, 19-bit time base timer,
                                    32kHz timer/counter
  — Remote control reception circuit Incorporated 6-stage FIFO 8-bit measurement counter
  — PWM output for tuner   14 bits, 1 channel
- Interruption   12 factors, 12 vectors, multi-interruption possible
- Standby mode   SLEEP/STOP
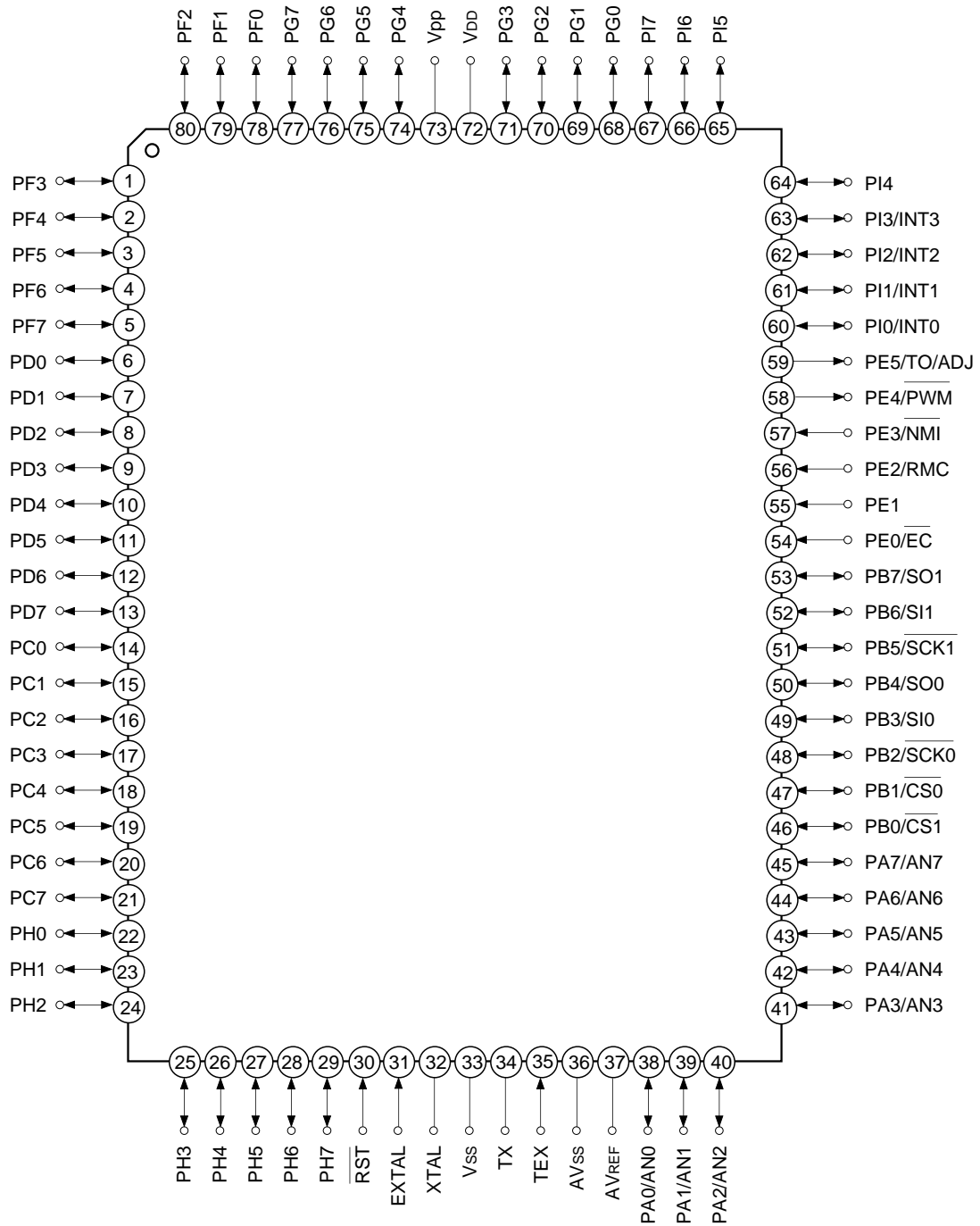- Package   80-pin plastic QFP

Structure

Silicon gate CMOS IC

E93908-ST

Block Diagram

PA0 to PA7
PB0 to PB7
PC0 to PC7
PD0 to PD7
PE0 to PE3
PE4 to PE5
PF0 to PF7
PG0 to PG7
PH0 to PH7
PI0 to PI7

PORT A
PORT B
PORT C
PORT D
PORT E
PORT F
PORT G
PORT H
PORT I

CLOCK GEN./ SYSTEM CONTROL

VPP
VSS
VDD
RST
XTAL
EXTAL
TX
TEX

SPC700 CPU CORE

ROM 16K BYTES

RAM 448 BYTES

32kHz TIMER/COUNTER

PRESCALER/ TIME BASE TIMER

PE3/NMI
PI3/INT3
PI2/INT2
PI1/INT1
PI0/INT0

INTERRUPT CONTROLLER

A/D CONVERTER

14 BIT PWM GENERATOR

REMOCON

FIFO

SERIAL INTERFACE UNIT 0

FIFO

8 BIT TIMER/COUNTER 0

8 BIT TIMER 1

AVREF
AVSS

AN0 to AN7

PE4/PWM

PE2/RMC

PB1/CS0
PB3/SI0
PB4/SO0
PB2/SCK0
PB0/CS1
PB6/SI1
PB7/SO1
PB5/SCK1

PE0/EC
PE5/TO

PE5/ADJ

Pin Assignment (Top View)

Note) NC (Pin 73) must be connected to V$_{DD}$.
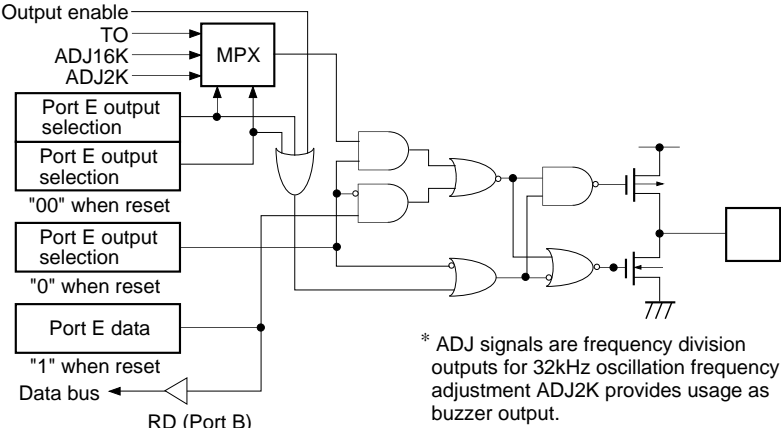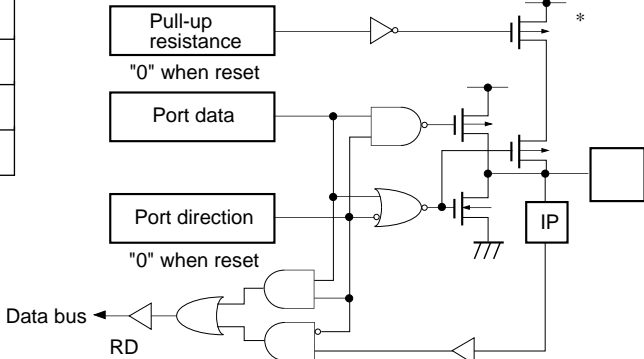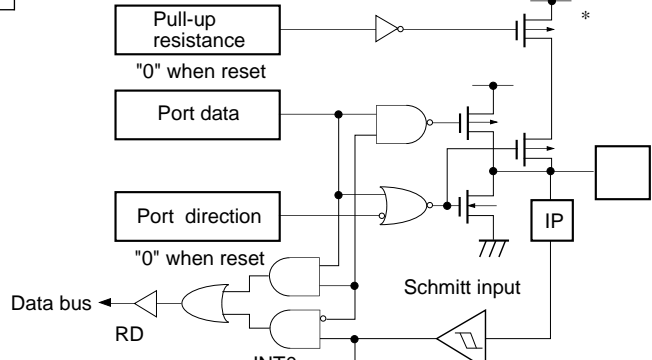
Pin Description

Pin code	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/analog input	(Port A) 8-bit I/O port. I/O can be set in single bit units. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/$\overline{CS1}$	I/O/input	(Port B) 8-bit I/O port. I/O can be set in single bit units. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Chip select input for serial interface (CH1).
PB1/$\overline{CS0}$	I/O/input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/input		Serial data input (CH0).
PB4/SO0	I/O/output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/input/output		Serial clock I/O (CH1).
PB6/SI1	I/O/input		Serial data input (CH1).
PB7/SO1	I/O/output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/$\overline{EC}$	Input/input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. Incorporation of pull-up resistor can be set through the software. (8 pins)	External event inputs for timer/counter.
PE1	Input		
PE2/RMC	Input/input		Remote control reception circuit input.
PE3/$\overline{NMI}$	Input/input		Non-maskable interruption request input.
PE4/$\overline{PWM}$	Output/output		14-bit PWM output.
PE5/TO/ADJ	Output/output/ output		Rectangular wave output for 16-bit timer/ counter (duty output 50%). Output for 32kHz oscillation frequency demultiplication.
PF0 to PF7	I/O	(Port F) 8-bit output port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

Pin code	I/O	Functions	
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PI0/INT0 to PI3/INT3	I/O/input	(Port I) 8-bit output ports. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs.
PI4 to PI7	I/O		
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock generation circuit. Connect a 32.768kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and open TX.	
TX	Output		
$\overline{RST}$	Input	Low-level active, system reset.	
Vpp		Vcc supply for writing of built-in PROM. Under normal operating conditions, connect to VDD.	
AVREF	Input	Reference voltage input for A/D converter.	
AVss		A/D converter GND.	
VDD		Vcc supply.	
Vss		GND	
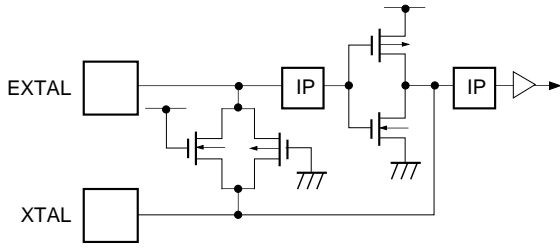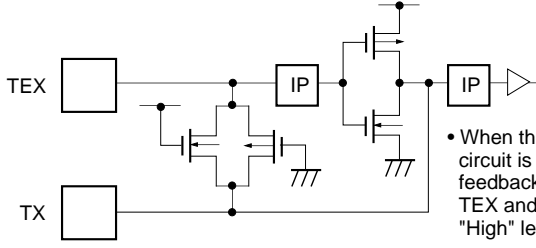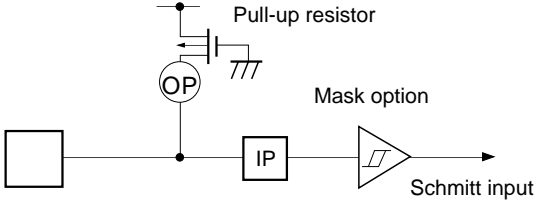
I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	**Port A** Pull-up resistance "0" when reset Port A data Port A direction "0" when reset Data bus ◄ RD (Port A) Port A input selection "0" when reset Input multiplexer A/D converter ◄ IP — Input protection circuit * Pull-up transistors approx. 100kΩ	Hi-Z
PB0/CS1 PB1/CS0 PB3/SI0 PB6/SI1 4 pins	**Port B** Pull-up resistance "0" when reset Port B data Port B direction "0" when reset Data bus ◄ RD (Port B) CS1 CS0 SI0 SI1 Schmitt input IP * Pull-up transistors approx. 100kΩ	Hi-Z
PB2/SCK0 PB5/SCK1 2 pins	**Port B** Pull-up resistance "0" when reset SCK OUT Output enable Port B output selection "0" when reset Port B data Port B direction "0" when reset Data bus ◄ RD (Port B) SCK0, SCK1 in ◄ Schmitt input IP * Pull-up transistors approx. 100kΩ	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1 2 pins	**Port B** Pull-up resistance SO Output enable Port B output selection "0" at reset Port B data Port B direction "0" when reset Data bus RD (Port B) IP * Pull-up transistors approx. 100kΩ	Hi-Z
PC0 to PC7 8 pins	**Port C** Pull-up resistance "0" when reset Port C data Port C direction "0" when reset Data bus RD (Port C) IP *1 High current drive of 12mA possible *2 Pull-up transistors approx. 100kΩ	Hi-Z
PE0/$\overline{EC}$ PE1 PE2/RMC PE3/$\overline{NMI}$ 4 pins	**Port E** Schmitt input IP $\overline{EC}$ RMC/$\overline{NMI}$ Data bus RD (Port E) Note : PE1 No schmitt input.	Hi-Z
PE4/$\overline{PWM}$ 1 pin	**Port E** $\overline{PWM}$ Port E output selection "0" when reset Port E data "1" when reset Data bus RD (Port E)	H level

Pin	Circuit format	When reset
PE5/TO/ADJ 1 pin	**Port E** Output enable TO ADJ16K → MPX ADJ2K Port E output selection Port E output selection "00" when reset Port E output selection "0" when reset Port E data "1" when reset Data bus RD (Port B) * ADJ signals are frequency division outputs for 32kHz oscillation frequency adjustment ADJ2K provides usage as buzzer output.	H level When reset. "H level" with about 150kΩ resistor.
PD0 to PD7 PF0 to PF7 PG0 to PG7 PH0 to PH7 PI4 to PI7 36 pins	**Port D** **Port F** **Port G** **Port H** **Port I** Pull-up resistance "0" when reset Port data Port direction "0" when reset Data bus RD IP * Pull-up transistors approx. 100kΩ	Hi-Z
PI0 to PI3 4 pins	**Port I** Pull-up resistance "0" when reset Port data Port direction "0" when reset Data bus RD INT0 INT1 INT2 INT3 Schmitt input IP * Pull-up transistors approx. 100kΩ	Hi-Z

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop and XTAL becomes "High" level.	Oscillation
TEX TX 2 pins	 • Digram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become "Low" level and "High" level respectively.	Oscillation
$\overline{\text{RST}}$ 1 pin	 Pull-up resistor Mask option Schmitt input	L level

Absolute Maximum Ratings   (Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	−0.3 to +7.0	V	
	V_{PP}	−0.3 to +13.0	V	Incorporated PROM
	AV_{SS}	−0.3 to +0.3	V	
Input voltage	V_{IN}	−0.3 to +7.0[*1]	V	
Output voltage	V_{OUT}	−0.3 to +7.0[*1]	V	
High level output current	I_{OH}	−5	mA	Output per pin
High level total output current	ΣI_{OH}	−50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	Value per pin, excluding high current outputs
	I_{OLC}	20	mA	Value per pin[*2] for high current outputs
Low level total output current	ΣI_{OL}	100	mA	Total for all output pins
Operating temperature	Topr	−10 to +75	°C	
Storage temperature	Tstg	−55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

[*1] V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

[*2] The high current drive transistor is the N-ch transistor of Port C (PC)

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should
    be conducted under the recommended operating conditions. Exceeding these conditions may adversely
    affect the reliability of the LSI.

Recommended Operating Conditions   (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	High speed mode guaranteed operation range[1]
		3.5	5.5		Low speed mode guaranteed operation range[1]
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
	Vpp	$Vpp = V_{DD}$		V	[5]
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	[2]
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	Hysteresis input[3]
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL[4]
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	[2]
	V_{ILS}	0	$0.2V_{DD}$	V	Hysteresis input[3]
	V_{ILEX}	-0.3	0.4	V	EXTAL[4]
Operating temperature	Topr	-10	$+75$	°C	

[1] High speed mode is 1/2 frequency demultiplication clock selection; low-speed mode is 1/16 frequency demultiplication clock selection.

[2] Value for each pin of normal input ports (PA, PB4, PB7, PC, PD, PE1, PF to PH, PI4 to PI7).

[3] Value of the following pins: $\overline{RST}$, $\overline{CS0}$, $\overline{CS1}$, $\overline{SCK0}$, $\overline{SCK1}$, SI0, SI1, $\overline{EC}$, RMC, $\overline{NMI}$, INT0, INT1, INT2, INT3.

[4] Specifies only during external clock input.

[5] Vpp and V_{DD} should be set to same voltage.

Electrical Characteristics

DC Characteristics

(Ta = −10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	V_{OH}	PA to PD, PE4, PE5, PF to PI	V_{DD} = 4.5V, I_{OH} = −0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = −1.2mA	3.5			V
Low level output current	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	μA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.5		−40	μA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IL} = 5.5V	0.1		10	μA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.1		−10	μA
	I_{ILR}	$\overline{RST}$[*1]		−1.5		−400	μA
	I_{IL}	PA to PD[*2], PF to PI[*2]				−50	μA
			V_{DD} = 4.5V, V_{IL} = 4.0V	−3.3			μA
I/O leakage current	I_{IZ}	PE0 to PE3 $\overline{RST}$[*1] PA to PD[*2], PF to PI[*2]	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	μA
Power supply current[*3]	I_{DD1}	V_{DD}	High-speed mode operation (1/2 frequency demultiplier clock) V_{DD} = 5.5V, 10MHz crystal oscillation ($C_1 = C_2$ = 15pF)		18	40	mA
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation ($C_1 = C_2$ = 47pF)		400	1000	μA
	I_{DDS1}		SLEEP mode V_{DD} = 5.5V, 10MHz crystal oscillation ($C_1 = C_2$ = 15pF)		1.1	8	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation ($C_1 = C_2$ = 47pF)		9	30	μA
	I_{DDS3}		STOP mode V_{DD} = 5.5V, 10MHz crystal oscillation; and termination of 32kHz oscillation			30	μA
Input capacity	C_{IN}	Pins other than PE4, PE5, XTAL, TX, AV_{REF}, AV_{SS}, V_{DD}, V_{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

[*1] $\overline{RST}$ pin specifies the input current when the product with pull-up resistance has been selected, and specifies the leakage current when the product with no resistance has been selected. (Refer to the products list.)

[*2] Pins PA to PD, and PF to PI specifies the input current when pull-up resistance has been selected, and specifies the leakage current when no resistance has been selected.

[*3] When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = −10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	$t_{sys} + 50$*			ns
Event count input clock rise time, fall time	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_c	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock application condition)		32.768		kHz
Event count input clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			μs
Event count input clock rise time, fall time	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

* t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: 00FE$_H$).

t_{sys} (ns) = 2000/f_c (upper two bits = "00"), 4000/f_c (upper two bits = "01"), 16000/f_c (upper two bits = "11")
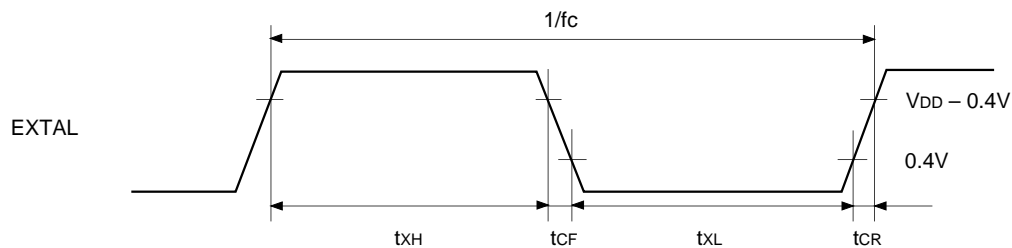
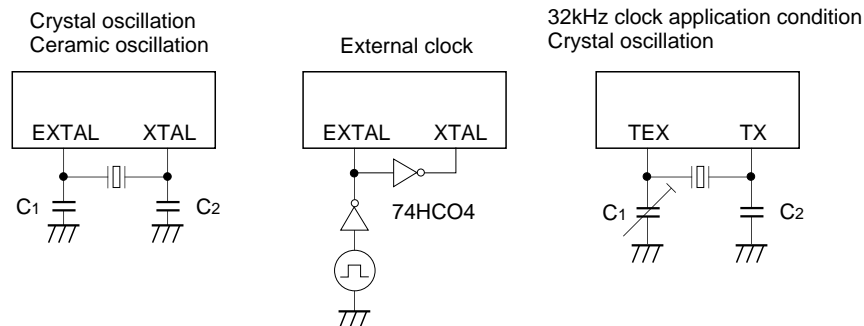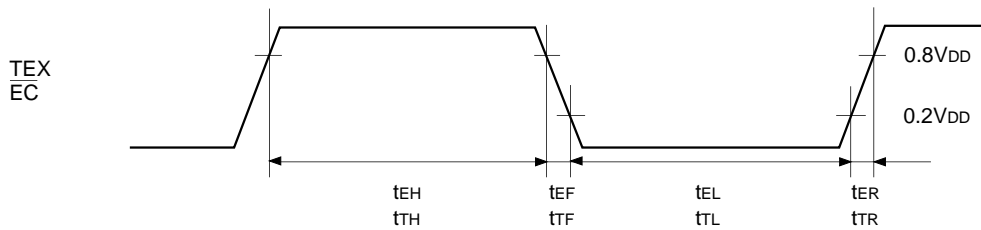### Fig. 1. Clock timing

Fig. 2. Clock application conditions

Fig. 3. Event count clock timing

(2) Serial transfer   (Ta = −10 to +75°C, VDD = 4.5 to 5.5V, Vss reference)
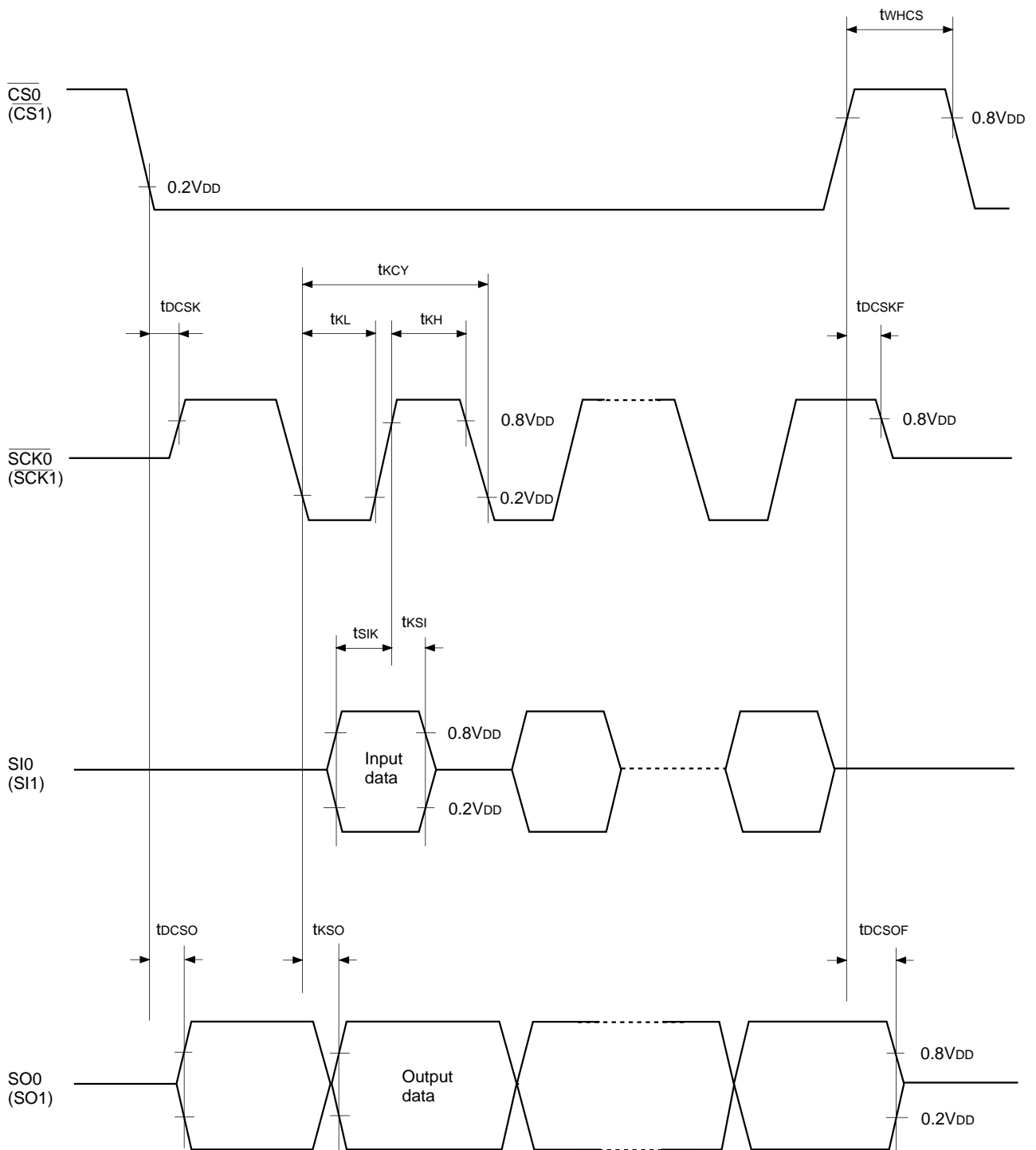
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ ($\overline{CS1} \downarrow \rightarrow \overline{SCK1}$) delay time	t_{DCSK}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		1.5t_{SYS} + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ ($\overline{CS1} \uparrow \rightarrow \overline{SCK1}$) float delay time	t_{DCSKF}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		1.5t_{SYS} + 200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ ($\overline{CS1} \downarrow \rightarrow SO1$) delay time	t_{DCSO}	SO0 (SO1)	Chip select transfer mode		1.5t_{SYS} + 200	ns
$\overline{CS0} \uparrow \rightarrow SO0$ ($\overline{CS1} \uparrow \rightarrow SO1$) float delay time	t_{DCSOF}	SO0 (SO1)	Chip select transfer mode		1.5t_{SYS} + 200	ns
$\overline{CS0}$ ($\overline{CS1}$) High level width	t_{WHCS}	$\overline{CS0}$ ($\overline{CS1}$)	Chip select transfer mode	t_{SYS} + 200		ns
$\overline{SCK0}$ ($\overline{SCK1}$) cycle time	t_{KCY}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	2t_{SYS} + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ ($\overline{SCK1}$) High, Low level width	t_{KH} t_{KL}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	t_{SYS} + 100		ns
			Output mode	8000/fc − 50		ns
SI0 (SI1) input set-up time (for $\overline{SCK0}$ $\uparrow$)	t_{SIK}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	100		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	200		ns
SI0 (SI1) input hold time (for $\overline{SCK0}$ $\uparrow$ ($\overline{SCK1}$ $\uparrow$))	t_{KSI}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	t_{SYS} + 200		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ ($\overline{SCK1} \downarrow \rightarrow SO1$) delay time	t_{KSO}	SO0 (SO1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode		t_{SYS} + 200	ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode		100	ns

Note 1) t_{SYS} indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: 00FEH).

t_{SYS} (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ ($\overline{SCK1}$) output mode, SO0 (SO1) output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing

(3) A/D converter characteristics (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						±3	LSB
Zero transition voltage	V_{ZT}*1		Ta = 25°C V_{DD} = 5.0V Vss = AV_{SS} = 0V	–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4930	4990	5050	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}		V_{DD} – 0.5		V_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV$_{REF}$ current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	µA

Fig. 5. Definition of A/D converter terms
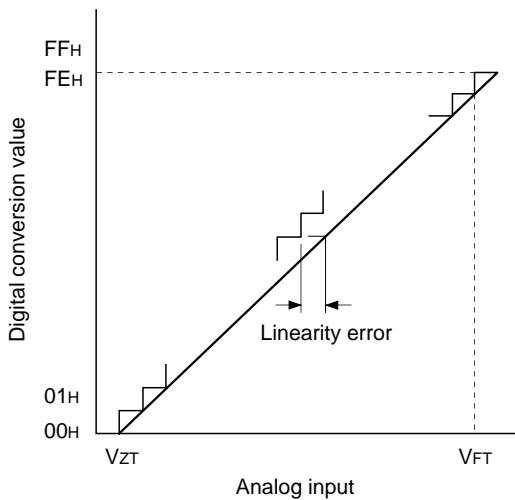
*1 V_{ZT} : Value at which the digital transfer value changes from 00H to 01H and vice versa.

*2 V_{FT} : Value at which the digital transfer value changes from FEH to FFH and vice versa.

*3 f_{ADC} indicates the below values due to the bit 6 (CKS) of A/D control resistor (address : 00F9H) and the Bit 7 (PCK1) and Bit 6 (PCK0) of clock control resistor (address : 00FFH).

CKS PCK1, 0	0 (φ/2 selection)	1 (φ/2 selection)
00 (φ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (φ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (φ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input   (Ta = −10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 $\overline{NMI}$		1		μs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		μs

Fig 6. Interruption input timing

INT0
INT1
INT2
INT3
$\overline{NMI}$
($\overline{NMI}$ specifies only for the falling edge)
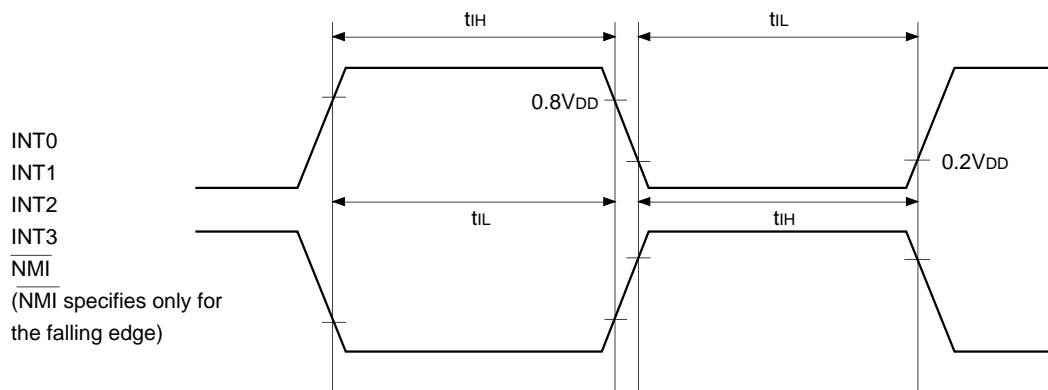
Fig. 7. $\overline{RST}$ input timing

$\overline{RST}$
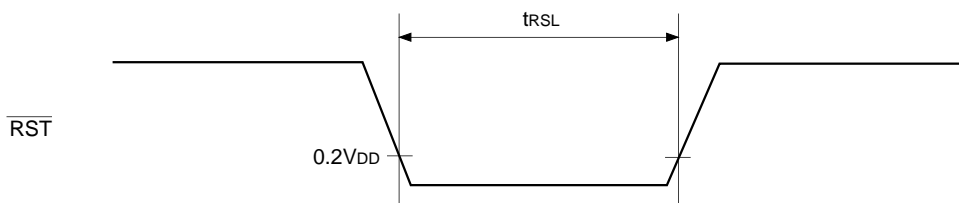
Appendix

Fig. 8. Recommended oscillation circuit

(i) Main clock

(ii) Main clock

(iii) Sub clock
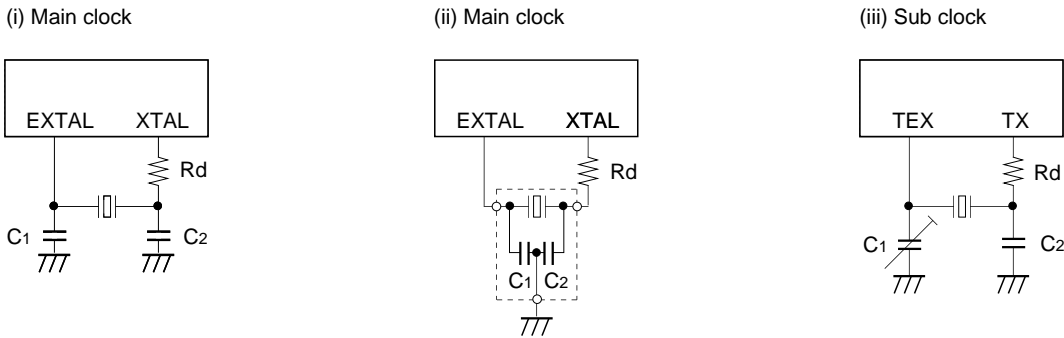
Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.00MTW*	10.00				
RIVER ELETEC CO., LTD.	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		
	P3	32.768kHz	50	22	1M	(iii)

Those marked with an asterisk (*) signify types with built-in ground capacitance (C_1, C_2).

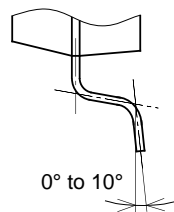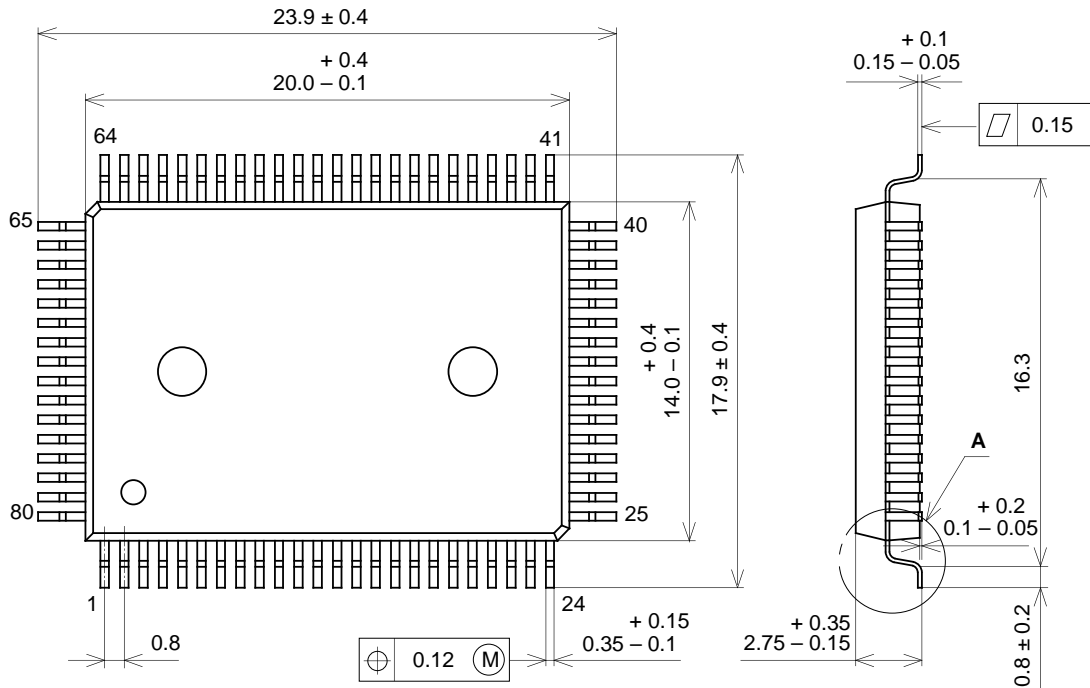**Selection Guide**

Item	Mask product	CXP844P16Q-1-□□□
Package	80-pin plastic QFP	80-pin plastic QFP
ROM capacitance	12K bytes/16K bytes	PROM 16K bytes
Reset pin pull-up resistor	Existent/Non-existent	Existent

Characteristics curves

I_{DD} vs. V_{DD}
(fc = 10MHz, Ta = 25°C, Typical)

I_{DD} – Supply current [mA]

20.0
10.0
5.0

1.0
0.5

0.1
(100µA)
0.05
(50µA)

0.01
(10µA)

1/2 dividing mode
1/4 dividing mode
1/16 dividing mode
SLEEP mode
32kHz mode
(instruction)

32kHz
SLEEP mode

2 3 4 5 6 7

V_{DD} – Supply voltage [V]

I_{DD} vs. fc
(V_{DD} = 5V, Ta = 25°C, Typical)

I_{DD} – Supply current [mA]

20

15

10

5

1/2 dividing mode
1/4 dividing mode
1/16 dividing mode
SLEEP mode

0 5 10 15

fc – System clock [MHz]

Package Outline   Unit: mm

80PIN QFP (PLASTIC)

23.9 ± 0.4

20.0 $^{+0.4}_{-0.1}$

64   41

65   40

14.0 $^{+0.4}_{-0.1}$ 17.9 ± 0.4

80   25

1   24

0.8   0.35 $^{+0.15}_{-0.1}$

⊕ 0.12 Ⓜ

0.15 $^{+0.1}_{-0.05}$ ▱ 0.15

16.3

A

0.1 $^{+0.2}_{-0.05}$

2.75 $^{+0.35}_{-0.15}$ 0.8 ± 0.2

0° to 10°

DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	∗QFP080-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g