

CMOS Analog Switch

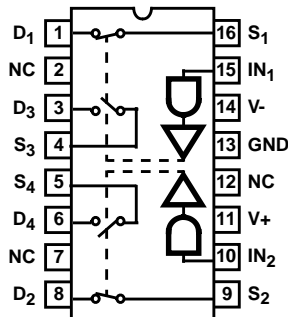
The HI-390 switch is a monolithic device fabricated using CMOS technology and the Intersil dielectric isolation process. This device is TTL compatible and features low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0390-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-0390-5	0 to 75	16 Ld PDIP	E16.3

Pinout Switch States shown for a Logic "1" Input

**DUAL SPDT HI-390 (CERDIP, PDIP)
TOP VIEW**



LOGIC	SW1, SW2	SW3, SW4
0	OFF	ON
1	ON	OFF

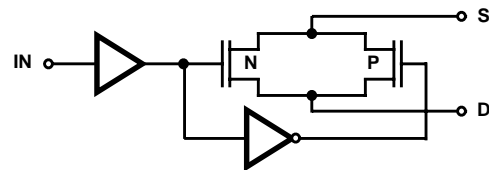
Features

- Analog Signal Range ($\pm 15V$ Supplies) $\pm 15V$
- Low Leakage 40pA
- Low On Resistance 35 Ω
- Break-Before-Make Delay 60ns
- Charge Injection 30pC
- TTL Compatible
- Symmetrical Switch Elements
- Low Operating Power 1.0mW

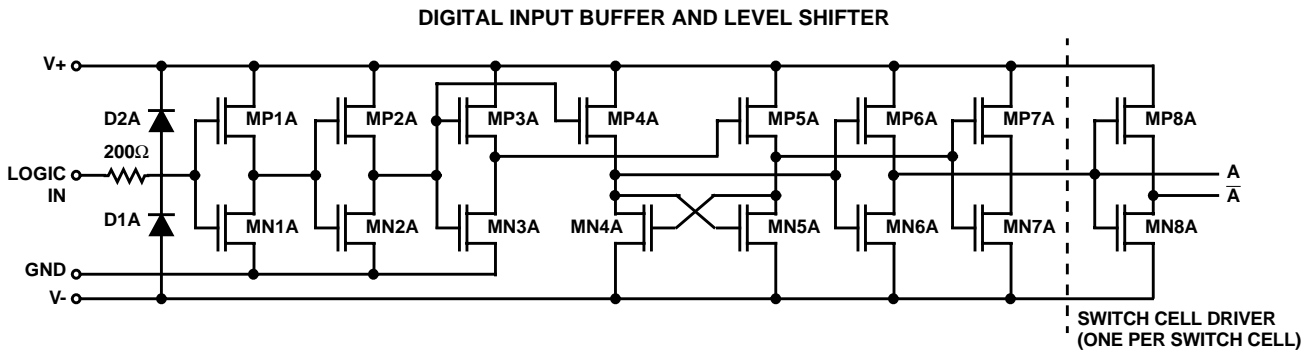
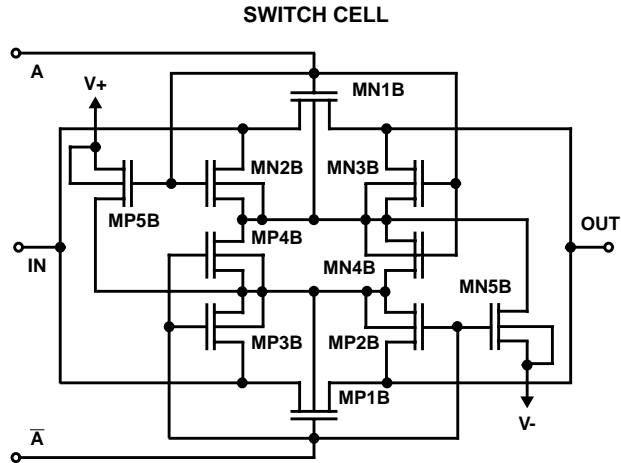
Applications

- Sample and Hold (i.e., Low Leakage Switching)
- Op Amp Gain Switching (i.e., Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Functional Diagram



Schematic Diagrams



Electrical Specifications Supplies = +15V, -15V; V_{IN} = Logic Input. V_{IN} for Logic "1" = 4V, for Logic "0" = 0.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	-2			-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS									
Current, I+	(Note 8)	25	-	0.09	0.5	-	0.09	0.5	mA
		Full	-	-	1	-	-	1	mA
Current, I-	(Note 8)	25	-	0.01	10	-	0.01	100	μA
		Full	-	-	100	-	-	-	μA
Current, I+	(Note 9)	25	-	0.01	10	-	0.01	100	μA
		Full	-	-	100	-	-	-	μA
Current, I-	(Note 9)	25	-	0.01	10	-	0.01	100	μA
		Full	-	-	100	-	-	-	μA

NOTES:

- $V_S = \pm 10V$, $I_{OUT} = \mp 10mA$. On resistance derived from the voltage measured across the switch under these conditions.
- $V_S = \pm 14V$, $V_D = \mp 14V$.
- $V_S = V_D = \pm 14V$.
- The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
- $V_S = 1V_{RMS}$, $f = 500kHz$, $C_L = 15pF$, $R_L = 1K$, $C_L = C_{FIXTURE} + C_{PROBE}$, OFF Isolation = 20 Log V_S/V_D .
- $V_S = 0V$, $C_L = 10nF$, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged. Charge Injection = $Q = C_L \times \Delta V$.
- $V_{IN} = 4V$ (one input, all other inputs = 0V).
- $V_{IN} = 0.8V$ (all inputs).

Test Circuits and Waveforms

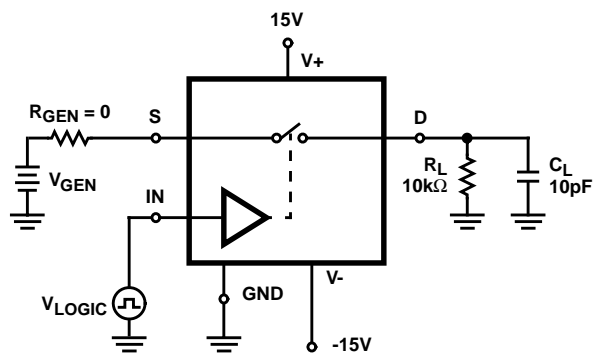


FIGURE 1A. TEST CIRCUIT

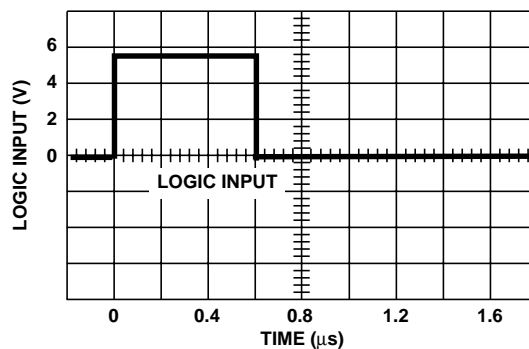


FIGURE 1B. LOGIC INPUT

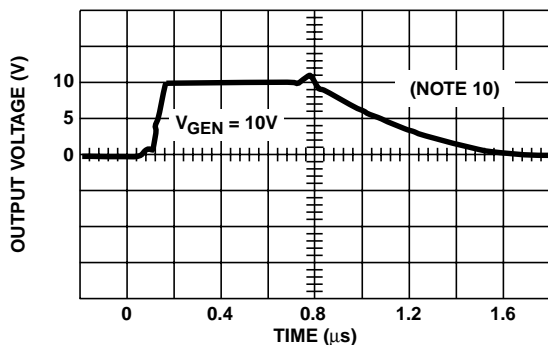


FIGURE 1C. $V_{ANALOG} = 10V$

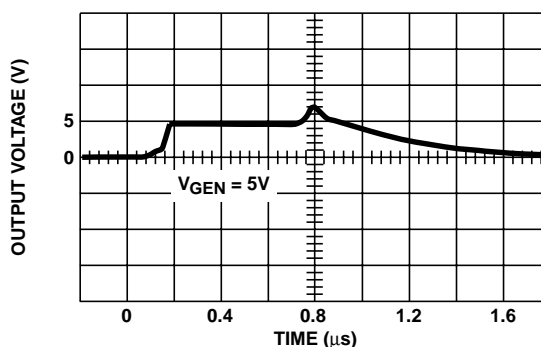


FIGURE 1D. $V_{ANALOG} = 5V$

Test Circuits and Waveforms (Continued)

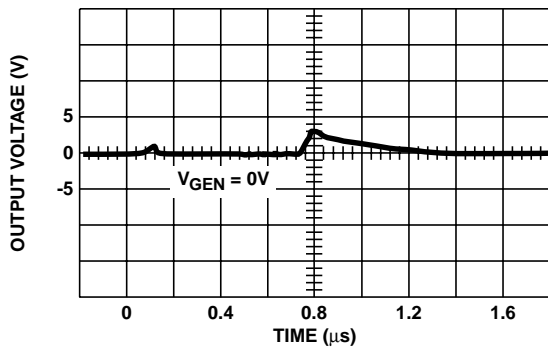


FIGURE 1E. $V_{ANALOG} = 0V$

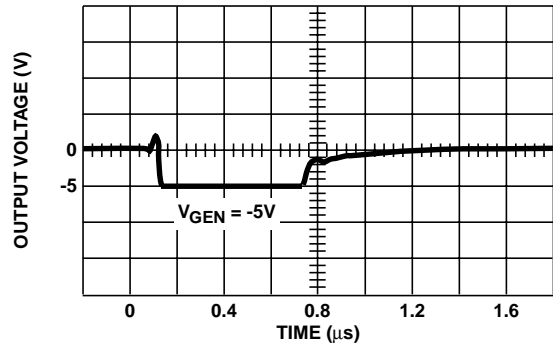


FIGURE 1F. $V_{ANALOG} = -5V$

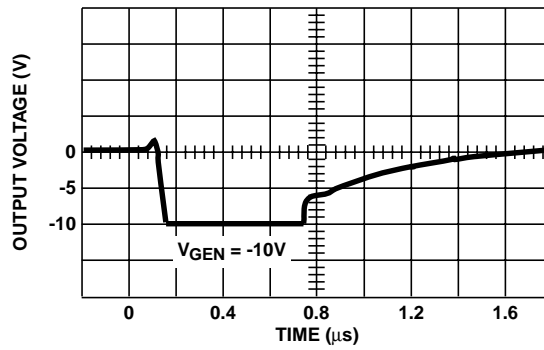


FIGURE 1G. $V_{ANALOG} = -10V$

NOTE:

10. If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 1. SWITCHING WAVEFORMS FOR VARIOUS ANALOG INPUT VOLTAGES

Typical Performance Curves

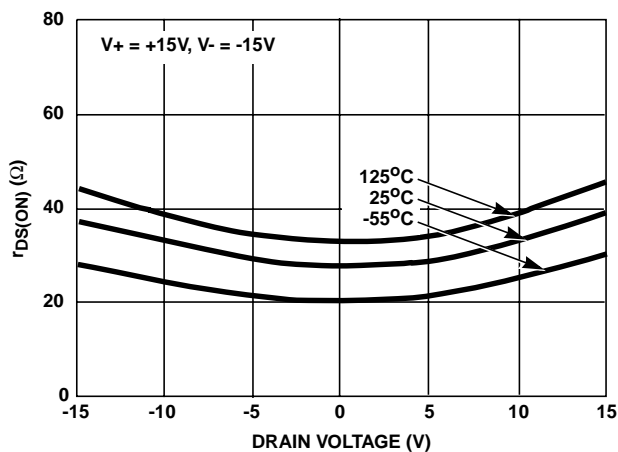


FIGURE 2. $r_{DS(ON)}$ vs V_D

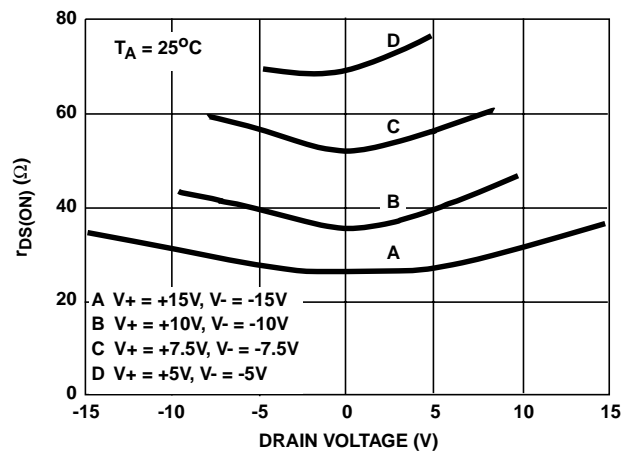


FIGURE 3. $r_{DS(ON)}$ vs V_D

Typical Performance Curves (Continued)

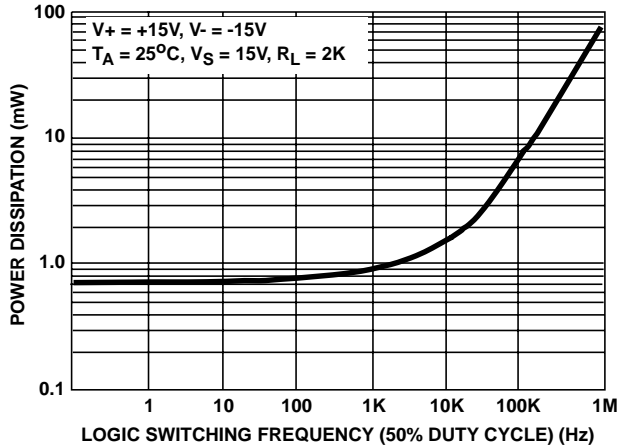


FIGURE 4. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY (SINGLE LOGIC INPUT)

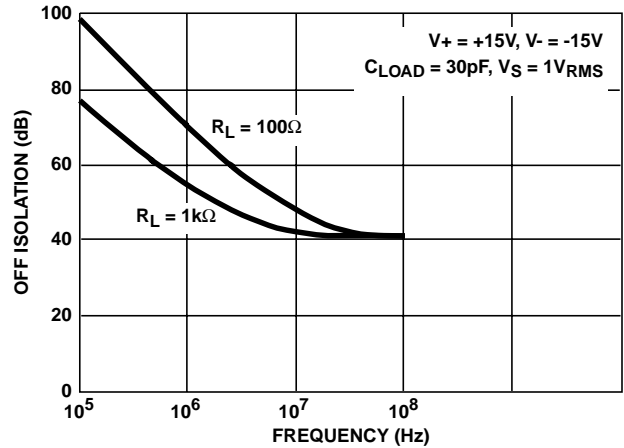


FIGURE 5. OFF ISOLATION vs FREQUENCY

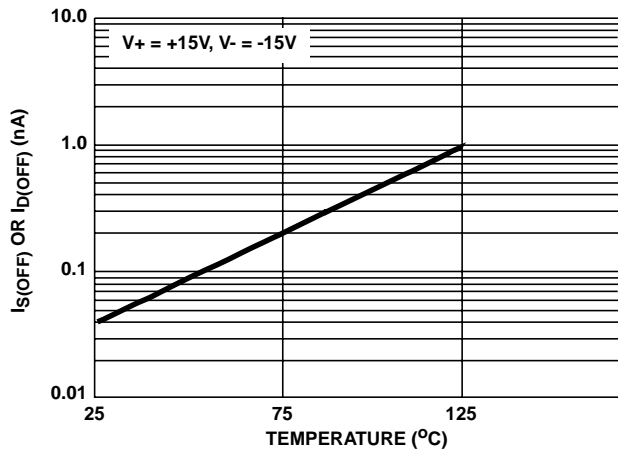


FIGURE 6. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE (NOTE 11)

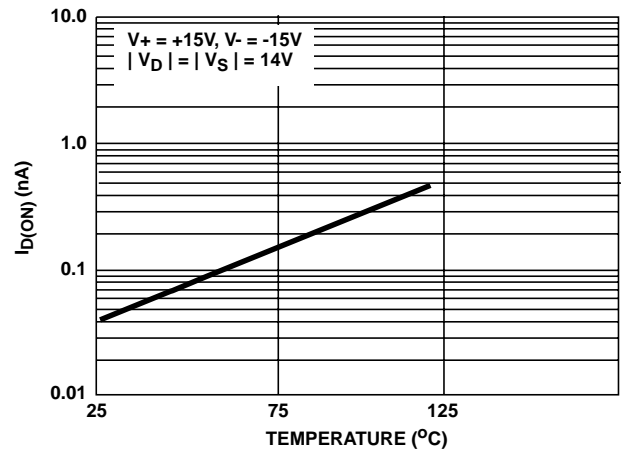


FIGURE 7. $I_{D(ON)}$ vs TEMPERATURE (NOTE 11)

NOTE:

11. The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

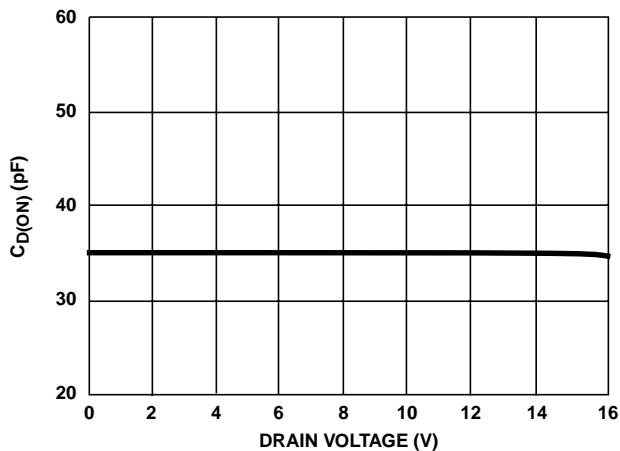


FIGURE 8. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

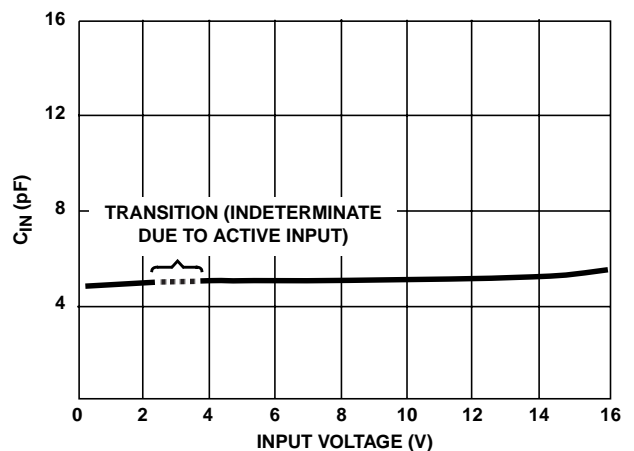


FIGURE 9. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

Typical Performance Curves (Continued)

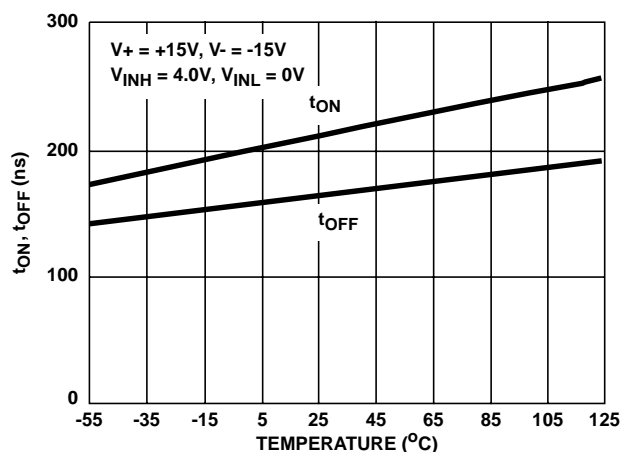


FIGURE 10. SWITCHING TIME vs TEMPERATURE

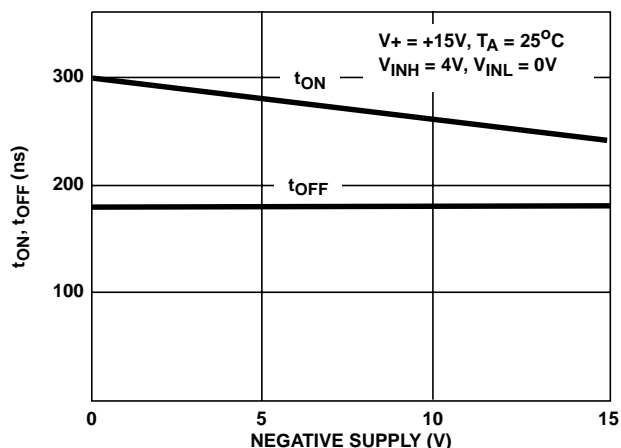


FIGURE 11. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

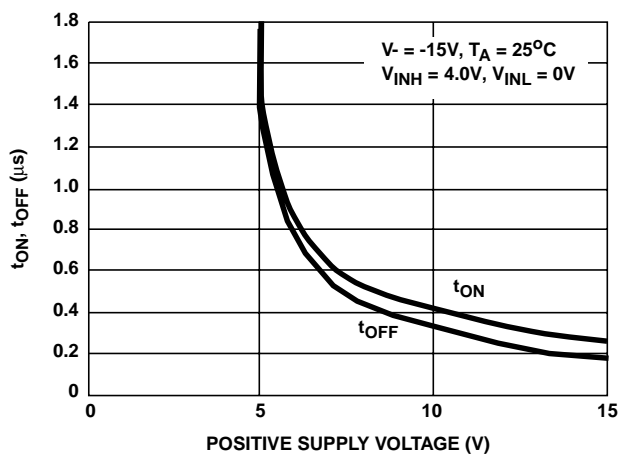


FIGURE 12. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE

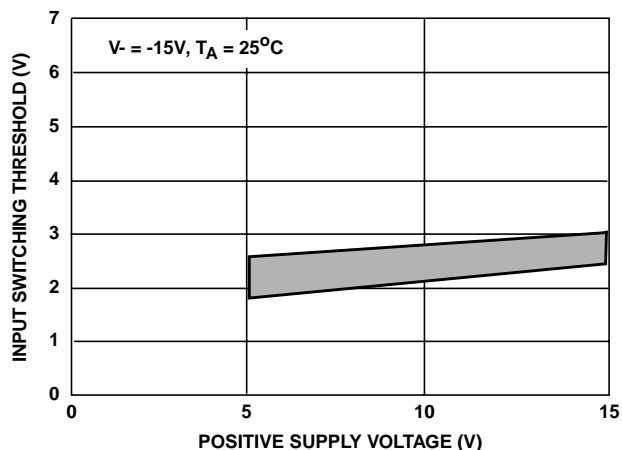


FIGURE 13. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE

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