
HN62V454 Series

524288-word × 8-bit/ 262144-word × 16-bit CMOS
Mask Programmable ROM

HITACHI

ADE-203-615A (Z)
Rev. 1.0
Jul. 4, 1996

Description

The HN62V454 is a 4-Mbit CMOS mask-Programmable ROM organized either as 262144 words by 16 bits or 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 200 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

- Low voltage operation
 - Operating supply voltage: 2.7 to 3.6 V
- High speed
 - Access time: 200 ns (max)
- Low power
 - Active: 72 mW (max)
 - Standby: 72 μ W (max)
- Byte-wide or word-wide data organization (Switched by BHE terminal)
- Three-state data output for or-tying
- Directly LVTTTL compatible
 - All inputs and outputs

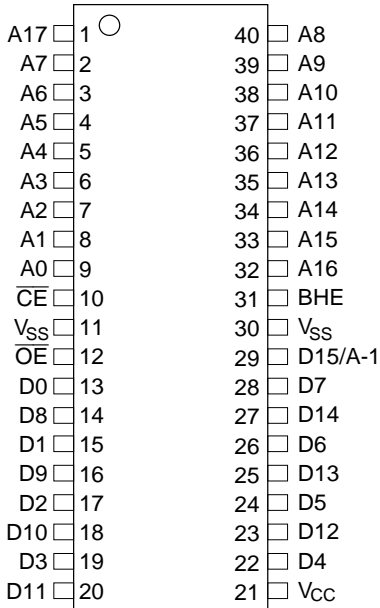
Ordering Information

Type No.	Access time	Package
HN62V454P-20	200 ns	600 mil 40-pin plastic DIP (DP-40)
HN62V454FA-20	200 ns	525 mil 40-pin plastic SOP (FP-40D)
HN62V454TT-20	200 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

HN62V454 Series

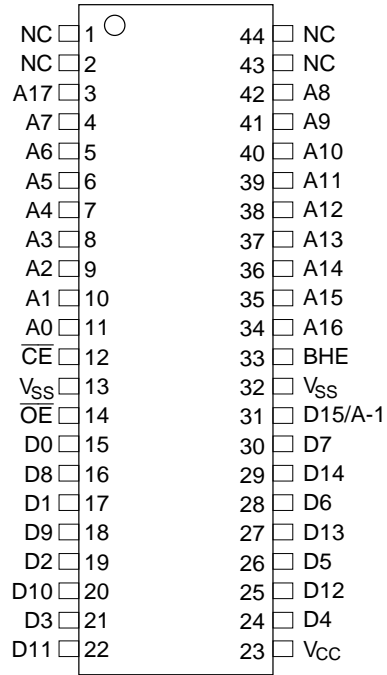
Pin Arrangement

HN62V454P Series



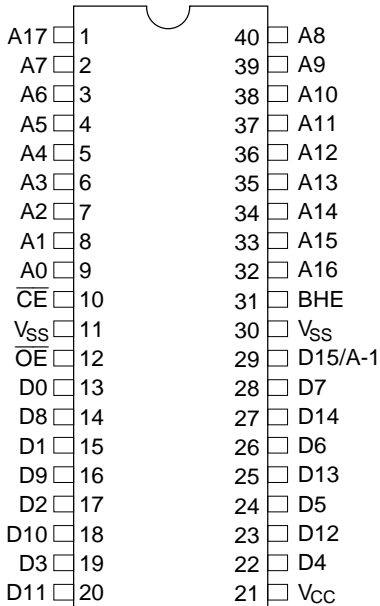
(Top view)

HN62V454TT Series



(Top view)

HN62V454FA Series

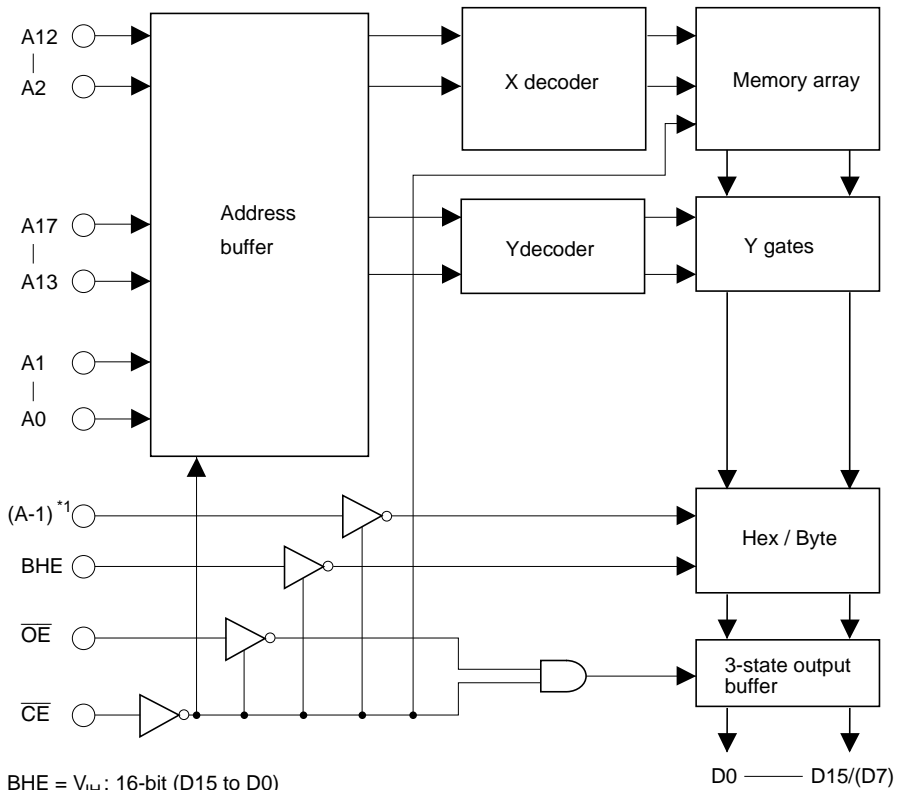


(Top view)

Pin Description

Pin name	Function
A-1, A0 to A17	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
\overline{CE}	Chip enable
\overline{OE}	Output enable
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

Mode	Pin				Data output		Address input	
	$\overline{\text{CE}}$	$\overline{\text{OE}}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
	Standby	H	\times^{*1}	\times	\times	High-Z ^{*2}	High-Z	—
Output disable	L	H	\times	\times	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A17
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A17
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A17

Notes: 1. \times : Don't care.

2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ^{*1}	V_{DD}	-0.3 to + 5.5	V
All input and output voltage ^{*1}	$V_{\text{in}}, V_{\text{out}}$	-0.3 to $V_{\text{DD}} + 0.3$	V
Operating temperature range	T_{opr}	0 to + 70	°C
Storage temperature range	T_{stg}	-55 to + 125	°C
Temperature under bias	T_{bias}	-20 to + 85	°C

Note: 1. With respect to V_{SS} .

Recommended DC Operating Conditions ($T_{\text{a}} = 0$ to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.7	3.3	3.6	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	$V_{\text{DD}} + 0.3$	V
	V_{IL}	-0.3	—	0.8	V

DC Characteristics ($V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_a = 0$ to $+70^\circ\text{C}$)

Parameter		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{DD}	—	20	mA	$V_{DD} = 3.6$ V, $I_{DOUT} = 0$ mA, $t_{RC} = 200$ ns
	Standby	I_{SB1}	—	20	μA	$V_{DD} = 3.6$ V, $\overline{CE} \geq V_{DD} - 0.2$ V
	Standby	I_{SB2}	—	3	mA	$V_{DD} = 3.6$ V, $\overline{CE} \geq 2.2$ V
Input leakage current		$ I_{IL} $	—	2	μA	$V_{in} = 0$ to V_{DD}
Output leakage current		$ I_{OL} $	—	2	μA	$\overline{CE} = 2.2$ V, $V_{out} = 0$ to V_{DD}
Output voltage		V_{OH}	$V_{DD} - 0.2$	—	V	$I_{OH} = -100$ μA
		V_{OL}	—	0.2	V	$I_{OL} = 100$ μA

Capacitance ($V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_a = 25^\circ\text{C}$, $V_{in} = 0$ V, $f = 1$ MHz)

Parameter		Symbol	Min	Max	Unit
Input capacitance*1		C_{in}	—	10	pF
Output capacitance*1		C_{out}	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

HN62V454 Series

AC Characteristics ($V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_a = 0$ to $+70^\circ\text{C}$)

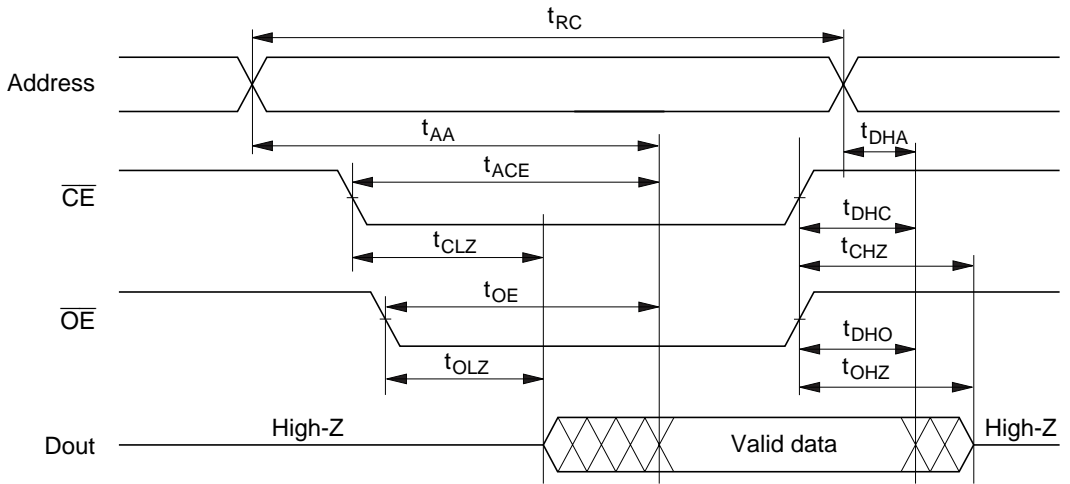
- Output load: $C_L = 50$ pF (including jig)
- Input pulse level: 0.4 to 2.4 V
- Input and output timing reference levels: 1.4 V
- Input rise and fall time: 5 ns

Parameter	Symbol	HN62V454-20		Unit	Note
		Min	Max		
Read cycle time	t_{RC}	200	—	ns	
Address access	t_{AA}	—	200	ns	
\overline{CE} access time	t_{ACE}	—	200	ns	
\overline{OE} access time	t_{OE}	—	70	ns	
BHE access time	t_{BHE}	—	200	ns	
Output hold time from address change	t_{DHA}	0	—	ns	
Output hold time from \overline{CE}	t_{DHC}	0	—	ns	
Output hold time from \overline{OE}	t_{DHO}	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	ns	
\overline{CE} to output in high-Z	t_{CHZ}	—	70	ns	1
\overline{OE} to output in high-Z	t_{OHZ}	—	70	ns	1
BHE to output in high-Z	t_{BHZ}	—	70	ns	1
\overline{CE} to output in low-Z	t_{CHZ}	5	—	ns	
\overline{OE} to output in low-Z	t_{OLZ}	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	ns	

Note: 1. t_{CHZ} , t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

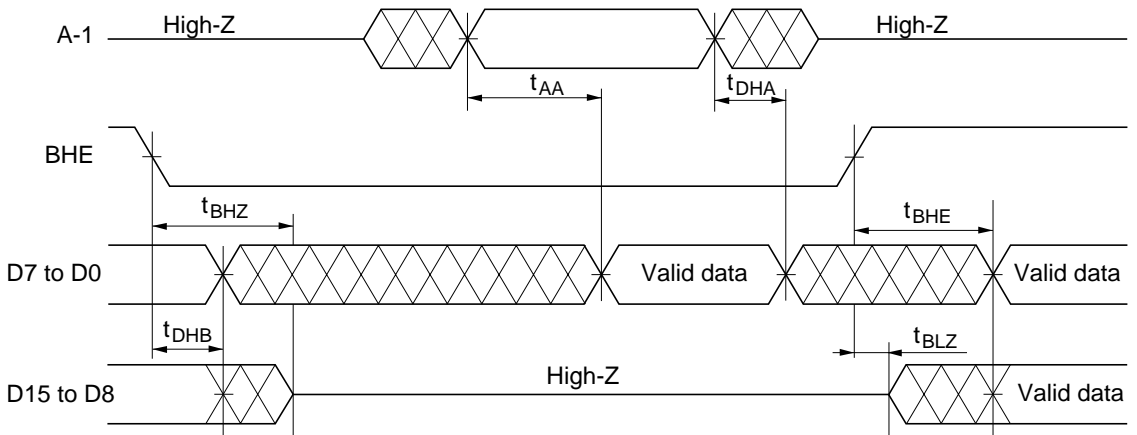
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



- Notes:
1. t_{DHA} , t_{DHC} , t_{DHO} : Determined by faster.
 2. t_{AA} , t_{ACE} , t_{OE} : Determined by slower.
 3. t_{CLZ} , t_{OLZ} : Determined by slower.

Word Mode, Byte Mode Switch



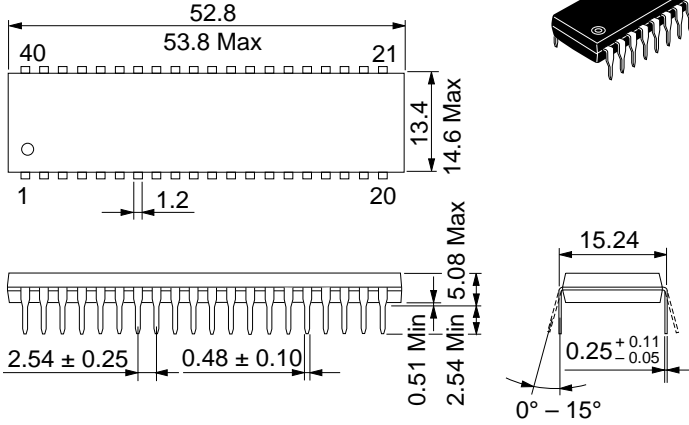
- Notes:
1. \overline{CE} and \overline{OE} are enable, A17 to A0 are valid.
 2. D15/A-1 pin is in the output state when BHE is high, \overline{CE} and \overline{OE} are enable. Therefore, the input signals of opposite phase to the output must not be applied to them.

HN62V454 Series

Package Dimensions

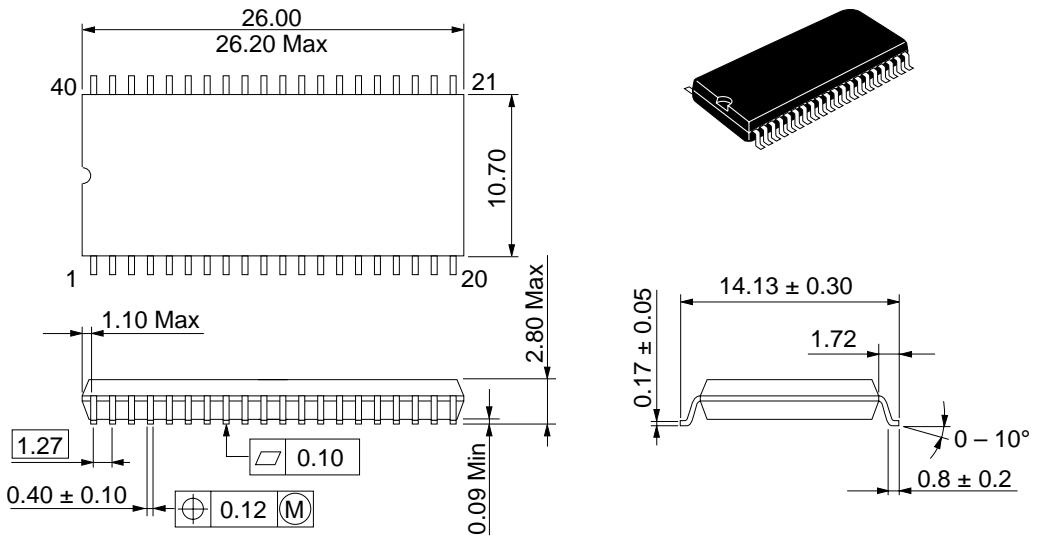
HN62V454P Series (DP-40)

Unit: mm



HN62V454FA Series (FP-40D)

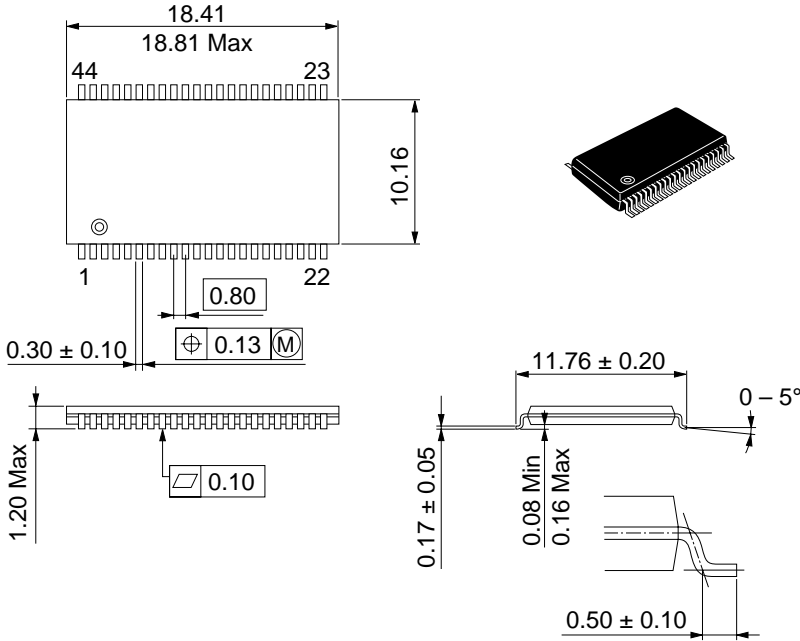
Unit: mm



Package Dimensions (cont.)

HN62V454TT Series (TTP-44D)

Unit: mm



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Revision Record

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1.0	Jul. 4, 1996	Initial issue		
