

PRELIMINARY
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 Some parametric limits are subject to change.

M62023L,P,FP

SYSTEM RESET IC WITH SWITCH FOR MEMORY BACK-UP

GENERAL DESCRIPTION

The M62023L/P/FP is a system reset IC that controls the memory backup function of an SRAM and an embedded RAM of a microcontroller.

The IC outputs reset signals ($\overline{\text{RES}}$ / $\overline{\text{RES}}$) to a microcontroller at power-down and power failure. It also shifts the power supply to RAMs from main to backup, outputs a signal ($\overline{\text{CS}}$) that invokes standby mode, and alters RAMs to backup circuit mode.

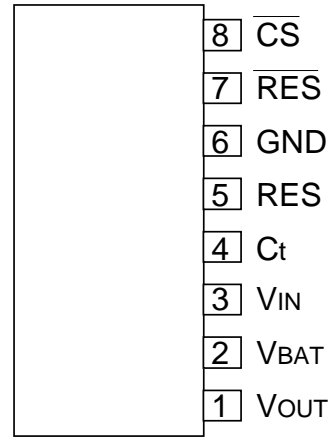
FEATURES

- Built-in switch for selection between main power supply and back-up power supply to RAMs
- Small difference between input and output voltages
 ($I_{\text{OUT}}=80\text{mA}$, $V_{\text{IN}}=3\text{V}$) : 0.15V typ
- Detection voltage (power supply monitor voltage) : 2.57V typ
- Chip select signal output ($\overline{\text{CS}}$)
- Two channels of reset outputs ($\overline{\text{RES}}$ / $\overline{\text{RES}}$)
- Power on reset circuit

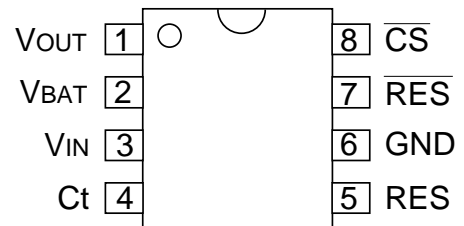
APPLICATION

Power supply control systems for memory of microcontroller systems in electronic equipment such as OA equipment, industrial equipment, and home-use electronic appliances and SRAM boards with built-in backup function that require switching between external power supply and battery.

PIN CONFIGURATION (TOP VIEW)

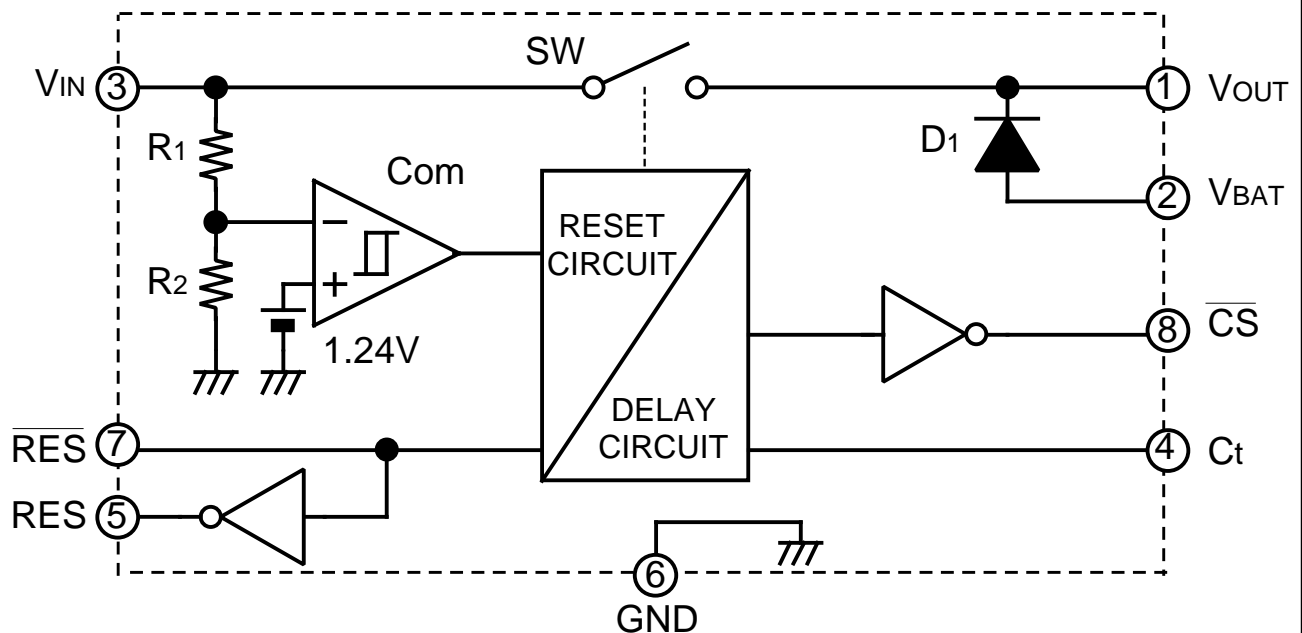


Outline 8P5 (L)



Outline 8P4 (P)
8P2S-A (FP)

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{IN}	Input voltage		7	V
I _{OUT}	Output current		100	mA
P _d	Power dissipation		800(L)/625(P)/440(FP)	mW
K _θ	Thermal derating	T _a 25°C	8(L)/6.25(P)/4.4(FP)	mW/°C
T _{opr}	Operating temperature		-20 to +75	°C
T _{stg}	Storage temperature		-40 to +125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
V _S	Detection voltage	V _{IN} (At charge from H → L)	2.44	2.57	2.70	V
V _S	Hysteresis voltage	V _S =V _{SH} -V _{SL}	50	100	200	mV
I _{CC}	Circuit current	I _{OUT} =0mA				mA
		V _{IN} =2V		1.5	3.0	
		V _{IN} =3V		6.5	10	
V _{DROP}	Difference between input and output voltages	V _{IN} =3V				V
		I _{OUT} =50mA		0.1	0.2	
		I _{OUT} =80mA		0.15	0.3	
V _{OH} (C _t)	C _t output voltage (high level)	V _{IN} =3V (Note 1)	2.0	2.4		V
V _{OL} (C _t)	C _t output voltage (low level)	V _{IN} =2V (Note 1)		0.02	0.1	V
V _{OH} (RES)	RES output voltage (high level)	V _{IN} =2V (Note 1)	1.5	2.0		V
V _{OL} (RES)	RES output voltage (low level)	V _{IN} =3V				V
		(Note 1)		0.02		
		I _{sink} =1mA		0.04	0.2	
V _{OH} (RES)	RES output voltage (high level)	V _{IN} =3V (Note 1)	2.5	3.0		V
V _{OL} (RES)	RES output voltage (low level)	V _{IN} =2V				V
		(Note 1)		0.02		
		I _{sink} =1mA		0.04	0.2	
V _{OH} (CS)	CS output voltage (high level)	V _{IN} =2V (Note 2)	1.3	1.6		V
		V _{IN} =0V, V _{BAT} =3V (Note 2)	2.40	2.47		
V _{OL} (CS)	CS output voltage (low level)	V _{IN} =3V				V
		(Note 1)		0.07		
		I _{sink} =1mA		0.08	0.3	
I _R	Backup Di leak current	V _{BAT} =3V				μA
		V _{IN} =3V			±0.5	
		V _{IN} =0V			±0.5	
V _F	Backup Di forward direction voltage	I _F =10μA		0.54	0.6	V
t _{pd}	Delay time	V _{IN} =0V → 3V, C _t =4.7μF	10	27	55	ms
t _d	Response time	V _{IN} =3V → 2V		5.0	25.0	μs
V _{OPL} (RES)	RES limit voltage of operation	(Note 3)		0.65		V

Note 1. Regarding conditions to measure V_{OH} and V_{OL}, voltage values are generated by internal resistance only and no external resistor is used.

2. These values are produced inserting an external resistor, R_{CS}=1M, between the CS pin and GND.

3. With no external resistor (10K internal resistance only)

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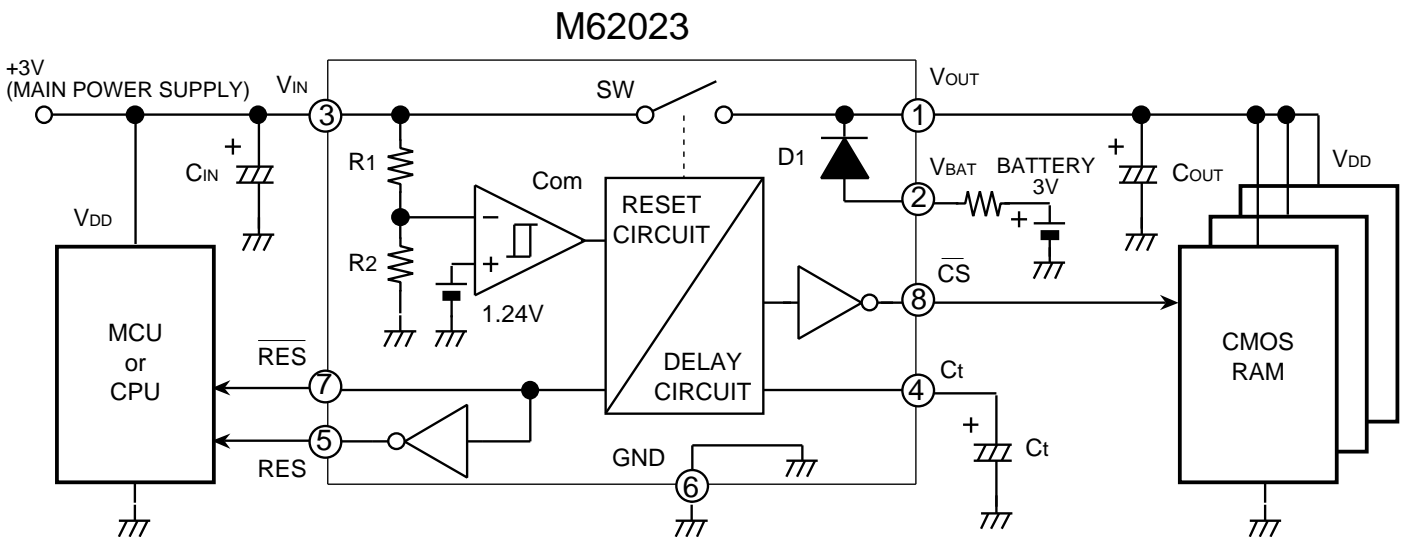
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EXPLANATION OF TERMINALS

Pin No.	Symbol	Name	Function
1	VOUT	Power supply output	V _{IN} and V _{BAT} are controlled by means of an internal switch and output through V _{OUT} . The pin is capable of outputting up to 100 mA. Use it as V _{DD} of CMOS RAM and the like.
2	V _{BAT}	Backup power supply input	Backup power supply is connected to this pin. If a lithium battery is used, insert a resistor in series for safety purposes.
3	V _{IN}	Power supply input	+3V input pin. Connect to a logic power supply.
4	C _t	Delay capacitor connection pin	A delay capacitor is connected to this pin. By connecting a capacitor, it is possible to delay each output.
5	RES	Positive reset output	Connect to the positive reset input of a microcontroller. The pin is capable of flowing 1mA sink current.
6	GND	Ground	Reference for all signals
7	$\overline{\text{RES}}$	Negative reset output	Connect to the negative reset input of a microcontroller. The pin is capable of flowing 1mA sink current.
8	$\overline{\text{CS}}$	Chip select output	Connect to the chip select of RAM. The CS output is at low level in normal state thereby letting RAM be active. Under failure or backup condition, the CS output is set to high level, then RAM enters standby state disabling read/write function. The pin is capable of flowing a 1mA sink current.

APPLICATION EXAMPLE



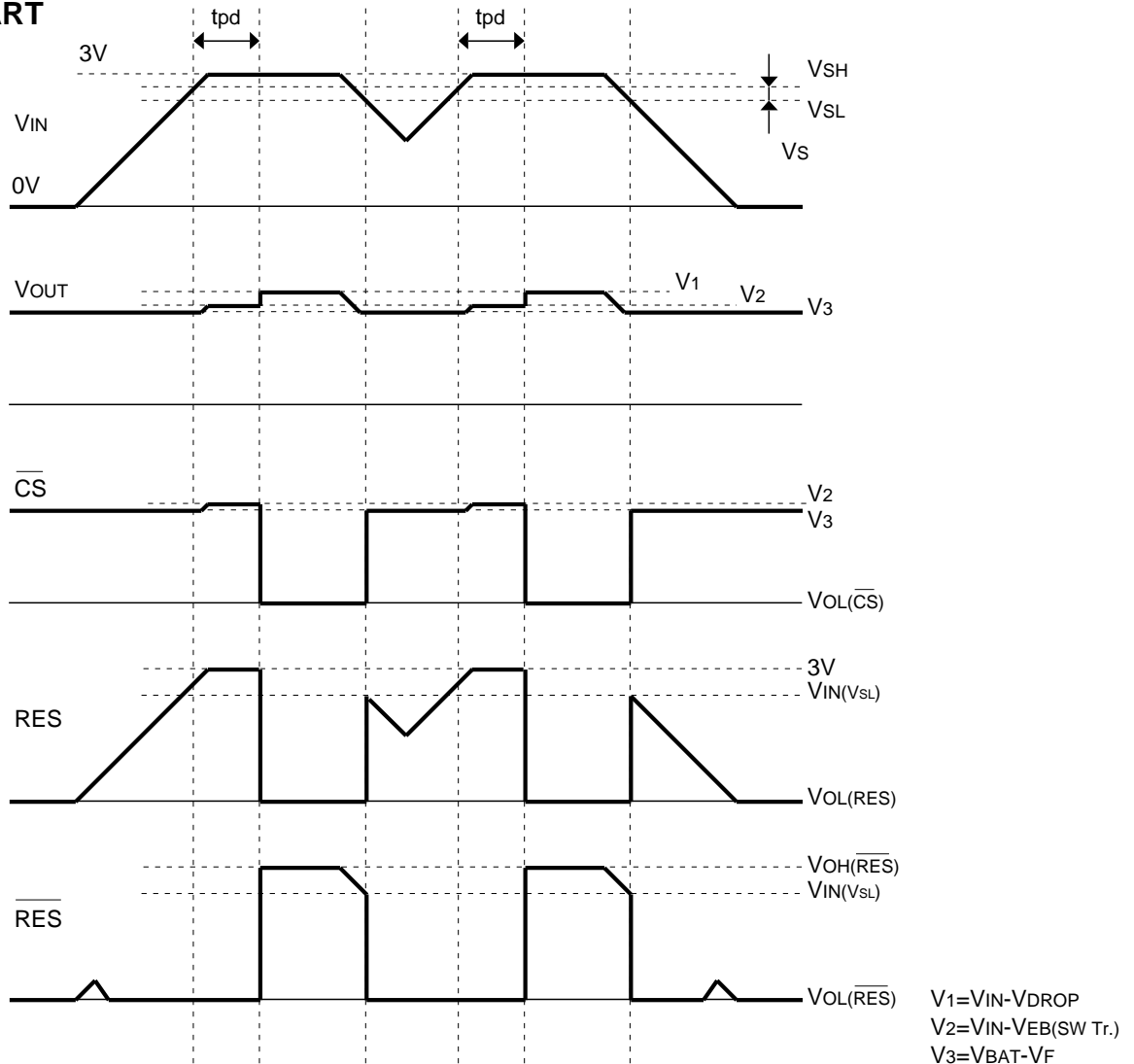
❖ Capacitance to be connected: C_{IN}: 10μF; C_{OUT}: 4.7μF; C_t: 4.7μF

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TIMING CHART



Input voltage	In normal operation	In failure (instantaneous drop)	Restoration from failure (instantaneous drop)	In backup state
Output pin	Input voltage : 3V	Input voltage : 3V → 2V Each output varies if the input voltage drops to V_{SL} or under	Input voltage : 2V → 3V If the input voltage goes higher than V_{SL} by 100mV, each output varies after delay produced by the delay circuit	Input voltage : 0V Backup voltage : 3V
V_{OUT}	With SW Tr. set to ON, a voltage ($V_{IN} - V_{DROP}$) is output	SW Tr. is turned OFF. A voltage ($V_{IN} - V_{EB}$) is output by the diode between E and B of SW Tr.	SW Tr. is turned ON after delay and a voltage ($V_{IN} - V_{DROP}$) is output	$V_{BAT} - V_F$
RES	The output level is $V_{OL}(RES)$ with a logic low	As the state shifts from a logic low to logic high, the output level becomes approximately equal to the input voltage	A logic high is maintained, and then shifts to a logic low	_____
\overline{RES}	The output level is $V_{OH}(\overline{RES})$ with a logic high	As the state shifts from a logic high to logic low, the output level becomes $V_{OL}(RES)$	A logic low is maintained, and then shifts to a logic high	_____
\overline{CS}	The output level is $V_{OL}(\overline{CS})$ with a logic low	As the state shifts from a logic low to logic high, the output level becomes the voltage $V_{IN} - V_{EB}$	A logic high is maintained, and then shifts to a logic low	The output is a logic high and the output level is $V_{BAT} - V_F$